A 2.6-GHz I/O Buffer for DDR4 & DDR5 SDRAMs in 16-nm FinFET CMOS Process

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***Abstract*—An input/output (I/O) buffer is developed to meet the specifications for DDR4 and DDR5 SDRAMs in terms of duty cycle, system voltage, and slew rate. As a means of reducing output current variations and increasing driving current, ultra-low threshold voltage (ULVT) transistors are opted for as output stage's driving devices. The gates of these transistors are stabilized thanks to the work of the novel VDDIO Detector circuit and an on-chip MIM capacitor that cancels out noise coupled from GND. Leakage currents are minimized by the modified Leakage Reduction and Floating N-well circuits. TSMC's 16-nm FinFET CMOS technology was used to realize the I/O buffer. The core area is 0.242×0.126 mm^2. It has operated reliably at a maximum worst case frequency of 2.6 GHz. At 2.2 GHz, it achieves a slew rate of 8.89 V/ns (0.8 V VDDIO) and 8.85 V/ns (1.2 V VDDIO), as well as a duty cycle of 48.0% (0.8 V VDDIO) to 48.2%. (1.2 V VDDIO). After auto-tuning the driving current, the slew rate (SR improvement) is increased by at least 28% at high voltage mode (VDDIO).**

***Index Terms*—I/O buffer, DDR4, DDR5, FinFET, slew rate.**

I. Introduction

The input/output driver interface's frequency is increasing, due to development of advanced high speed technologies especially in SDRAMs. Also, the standards for the quality of the output signals have been raised to a considerably higher level. I/O interfaces of SDRAMs, for instance, conform to DDR4DB02 (DDR4 Data Buffer Specification) that was established by JEDEC [1], [2]. DDR4 SDRAM requires specific parameters to operate correctly, including a slew rate (SR) standard that falls between 4-9 V/ns, a 1.2 V I/O voltage, an I/O pad load capacitance (C_L) ranging from 0.7-1.1 pF, and a 50±2% duty cycle ratio (DR) [1]. For DDR5 SDRAM standard, there is no established SR standard yet, but a VDDIO of 1.1 V, C_L of 0.4 to 0.9 pF, and a DRof 50±5% should be implemented [3].

Many electronic systems operated at 3.3 V or 1.8 V using legacy CMOS technologies like 180 nm. New nanoscale-based devices and systems operate at lower supplies like 0.9 V, making interfacing communication between legacy circuits and nano-CMOS-based FinFET chips difficult. Voltage level converters or translators can fix this problem, but they require more space and power. To communicate between these processes, FinFET CMOS mixed-voltage I/O buffers are preferred. Besides voltage level compatibility, SR must be considered while designing mixed-voltage I/O buffers. Interfacing legacy systems with new technologies like FinFETs is difficult because of SR variations. For example, PVT variations alter SR stability. Previous efforts on maintaining the slew rate of I/O buffers within a reasonable range were developed [4]–[8]. However, they cannot match the SR, I/O voltage, and DR criteria of the DDR4 standard. On the other hand, a prior output buffer complying with the slew rate requirements and operating with a higher frequency of 1.6 and 2.5 GHz was proposed [9]–[11]. The latest 2.5-GHz buffer implemented Duty Cycle Correctors and Feedback Detector were used to identify and rectify DR and voltage SR, respectively, depending on the needed parameters [11], [12].

This research, therefore, proposes a design for a 2.6-GHz, digital I/O buffer that satisfies both the DDR4 and DDR5 specifications for FinFET CMOS buffers. The Feedback Detector and Duty Cycle Correctors were not used. Instead, ultra-low V_{th} transistors (ULVT) were employed in all transistors where the input Data signal passes (violet font in Fig. 1) through achieving 2.6 GHz higher than the prior buffer (only 2.5 GHz). They are used since V_{th} drop hampers digital circuits in modern low-tech nodes with ultra-low supply voltages. They are also utilized in the output stage to maintain the required range of SR and DR. They are also implemented in the input stage decreasing the transistor counts when standard V_{th} (SVT) and low V_{th} (LVT) transistors are realized; thus, removing the need of the keeper for the inverter used in the traditional input stage. The leakage currents brought upon by these ULVTs were minimized by the Leakage Detection and the Floating N-well circuits. Lastly, conventional PVT Detectors are used to detect the PVT corner to maintain the suitable SR accordingly.

II. System Architecture

The system block diagram of a DDR4-and-DDR5-compliant I/O buffer with self-adjusting slew rate is depicted in Fig. 1. VDDIO Detector, Voltage Level Converter (VLC), Non-overlap circuits, Digital Logic Control circuit, Pre-drivers, PVT Detector, Output Buffer Stage, Floating N-well circuit, Leakage Reduction circuit, and Input Buffer stage are its constituent parts.

[1]The first two authors contributed equally to this work.

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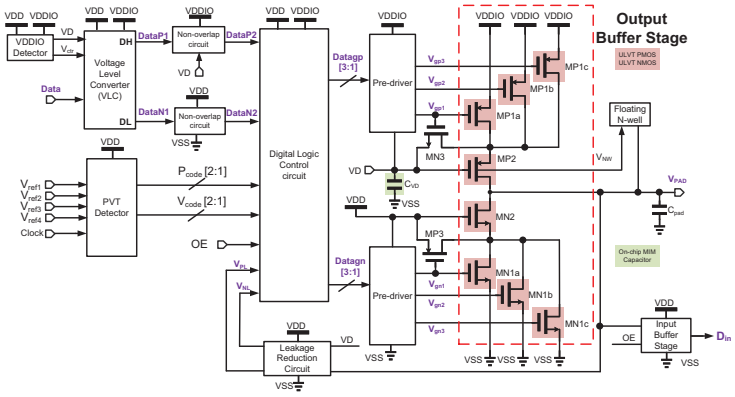


Fig. 1. Proposed I/O buffer for DDR4 & DDR5 SDRAMs.

Floating N-well circuits circumvent the channel of leakage current generated by mode switching at 1.2 V [13], [14]. Pre-charging control is implemented by SVT transistors, MP3 and MN3, to prevent immediate overstress on the Output Buffer Stage. The subsequent subsections will address the remaining blocks.

A. Output Stage

All transistors of Output Buffer Stage in Fig. 1 are all implemented using ULVT transistors. Compensating transistors MP1a, MP1b, and MP1c, are parallel stacked on top of MP2 to prevent transistor over-voltage at VDDIO of 1.2 V. The associated compensating transistor is activated when the PVT Detector detects a corner. When these compensating transistors are constantly on, the worst output current swings are prevented, resulting in a rise of the driving current and increase of SR. Meanwhile, MN1a, MN1b, and MN1c are compensating transistors that must sink the same magnitude of the driving current to increase the fall edge's SR.

B. VDDIO detector

Fig. 2 shows the novel VDDIO detector in Fig. 1. Mp5 is activated and Mp4 is deactivated due to the high voltage level at V3 when VDDIO is set to 1.2 V. Hence, V1 is equal to threshold voltage of Mp7 and V2 is pulled to 0. The clamper transistors, Mp8 and Mp9, generate a voltage of 0.4 V needed to supply Buffer Stage 2 which are implemented using ULVT devices. Thus, VD of 0.4 V is obtained. When VDDIO is equal to VDD, V3 becomes VDD - Vth, which causes Mp4 to turn on and pull V2 to VDD and V1 to 0 V. This generates a VD of 0 V. To ensure proper functionality across all simulated corners, cross-coupled transistors (Mn4 and Mn5) were added. The necessary driving current is supplied by Buffer Stage 2, as shown in Fig. 2.

C. Voltage Level Converter

Given that VDDIO can be any voltage between 0.8 V and 1.2 V, a Voltage Level Converter in Fig. 1 was required to safeguard against excessive voltage at Output stage [13], [14].

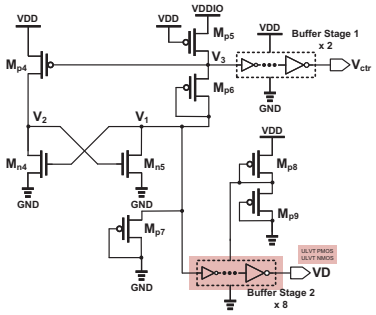


Fig. 2. VDDIO detector circuit diagram.

Depending on the VD value (0 or 0.4 V), it is utilized to decide if an increase in voltage for outputs, DH and DL, in Fig. 1 is necessary.

D. Non-overlap circuit

The Non-Overlap circuit in Fig. 1 generates two non-overlapping signals preventing compensating transistors MP1a, MP1b, MP1c and MN1a, MN1b, MN1c from turning on simultaneously during transitions. Transistors instead of logic gates as shown in Fig. 3 boost data rate [10]. VDD and VDDIO Non-overlap Circuits of the same size are needed, since VDDIO is either 0.8 V or 1.2 V. DataP2 and DataN2 have the same voltage levels as DataP1 and DataN1 in Fig. 1, respectively. All transistors are ULVTs for faster switching. Deep N-Well ULVTs are used for MN18, MN19, MN20, and MN21 for stable bias-to-source voltage in VDDIO Non-overlap circuit.

E. PVT detector

The number of compensating transistors activated by corresponding variations in processes, voltages, and temperatures is determined by the PVT Detector and then sent on to the Digital Logic Circuit for encoding. PVT detectors can be either P-type or N-type, reflecting the fact that there are five possible cases for process corners to be considered [2].

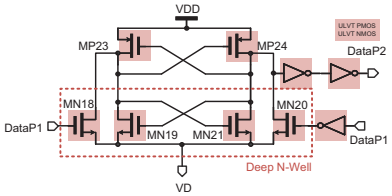


Fig. 3. VDDIO Non-overlap circuit.

F. Digital Logic Control

Digital Logic Control circuit is shown in Fig. 4. Referring to Fig. 1, Pcode[2:1] and Ncode[2:1] are encoded from the outputs of PVT Detector. Then, the said circuit's outputs, Vgp[3:1] and Vgn[3:1], are generated and fed through the Pre-Driver circuits in Fig. 4 to control the compensating transistors in the Output Stage. The Output Stage in Fig. 1 is deactivated by OE when Input Stage is activated. The signals VPL and VNL from the Leakage Reduction circuit will turn off transistors when VPAD = VDDIO.

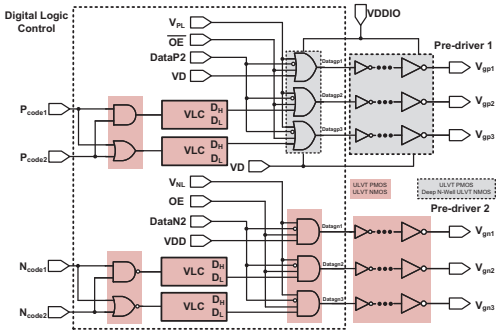


Fig. 4. Digital Logic Control and Pre-driver circuits.

G. Input Stage

Fig. 5 is the Input Stage's schematic where all devices are implemented using ULVTs for faster response. It is modified from the traditional design [13]. Notably, the keeper was not used, since the simple inverter can accept very high frequencies from the VPAD. Besides, when VDDIO is at 1.2 V, Mn19 creates the pre-charge route to operate V10 at VDD. When OE is low, the Input Stage is deactivated; thus, the Output Stage can perform its driving function. Otherwise, the Input Buffer is activated.

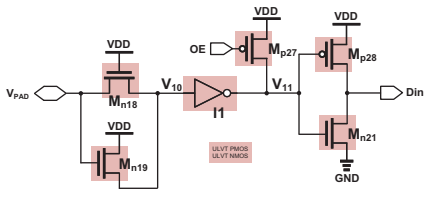


Fig. 5. Input Stage.

H. Leakage Reduction circuit

To overcome the leakage currents caused by over-voltage hazards when VPAD requals VDDIO, a modified Leakage Reduction circuit was used [15]. Unlike the report of [15], low-skew SVT-based inverters are implemented for INV51 and INV52, since VD is either 0 or 0.4 V.

III. All-PVT-Corner Post-Layout Simulation

TSMC 16-nm technology was used to design the I/O buffer. The buffer's whole chip layout is shown in Fig. 6. Its core and chip area are 0.242×0.126 mm^2 and $0.710\times0.0.452$ mm^2, respectively. Notably, C_{VD} overlaps with the VDDIO Detector since it is a MIM capacitor which uses higher layer levels of metals, thus, reducing chip area.

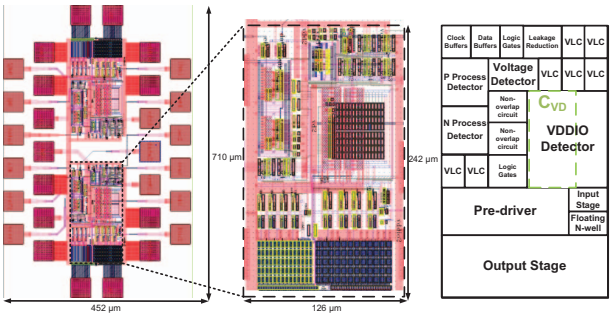


Fig. 6. Proposed I/O buffer's layout.

Our proposed I/O buffer exhibits two I/O voltages, such as VDDIO = 1.1/1.2 V and 0.8 V. The pad capacitance load (1.1 pF) represents C_L. At a frequency of 2.2 GHz, the all-PVT-corner post-layout simulation results for VDDIO = 0.8 V with and without PVT compensation are shown in Fig. 7. On the other hand, the results for maximum VDDIO = 1.2 V with and without PVT compensation are shown in Fig. 8. For the computation of Improvement in ΔSR, Eqn. (1) is used.

$$Improvement\ in\ \Delta SR\ (\%) = \frac{\Delta SR_{\text{NoPVT}} - \Delta SR_{\text{WithPVT}}}{\Delta SR_{\text{NoPVT}}} \quad (1)$$

where ΔSR_{NoPVT} and $\Delta SR_{\text{WithPVT}}$ is the difference between the worst-case slew rates without and with PVT compensation, respectively. Improvement in ΔSR for VDDIO of 0.8 V and 1.2 V is 10.7% and 28%, respectively. Fig. 9 shows the jitter simulations. The proposed I/O buffer is compared with prior works as summarized in Table I. Fig. 10 and 11 show the eye diagrams for VDDIO of 0.8 and 1.2 V, respectively. Fig. 12 shows the waveform at the highest frequency of the I/O buffer operating in the worst case.

IV. Conclusion

An I/O buffer is presented that meets the specifications for both DDR4 and DDR5. It operates at a worst case data rate of 2.6 GHz. Future work includes fabrication and testing of I/O buffer in silicon.

TABLE I
A COMPARISON OF THE PERFORMANCE OF THE PROPOSED APPROACH WITH EARLIER METHODS

	ICICDT [4]	MWSCAS [5]	APCCAS [9]	ISNE [10]	ISCAS [6]	APCCAS [8]	APCCAS [11]	This work
Year	2016	2018	2018	2019	2021	2021	2021	2023
Process (nm)	28	180	40	16	65	22	16	16
Verification	Simulation	Simulation	Simulation	Simulation	Simulation	Simulation	Simulation	Simulation
VDD (V)	1.05	1.8	0.9	0.8	1.8	1.8	0.8	0.8
VDDIO (V)	1.8/1.05	1.8	1.8/0.9	1.6/0.8	3.3/1.8/2.5	3.3/1.8	0.8/1.2	0.8/1.2/1.1
Max. Data Rate (GHz)	0.8	0.25	2.5/1.6	2.5	0.2	0.5	2.5	2.6
ΔSR (V/ns)	3.9/4.9	0.75/1.41	6.91/7.85	18/19.1	N/A	N/A	8.7/6.4	5.77/8.89
Improvement in ΔSR (%)	N/A	50	37	23.5/15.8	N/A	N/A	26/21	28/10.7
Duty Cycle (%)	N/A	N/A	N/A	N/A	N/A	N/A	49.2/48.3	48/48.2
Dynamic Power (mW)	N/A	N/A	33.71 (@500 MHz)	28 (@500 MHz)	29.8 (@200 MHz)	N/A	153 (@2.5 GHz)	143.5 (@2.6 GHz)

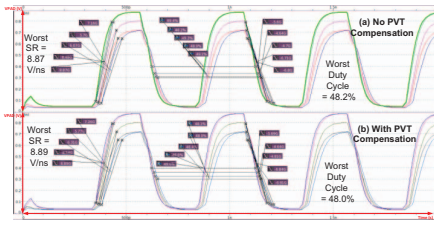


Fig. 7. A 0.8-V VDDIO's PAD output waveform (a) without PVT compensation (worst SR= 8.87 V/ns; best SR= 5.7 V/ns); (b) with PVT compensation (worst SR = 8.89 V/ns; best SR= 5.77 V/ns)

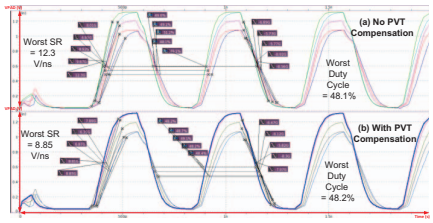
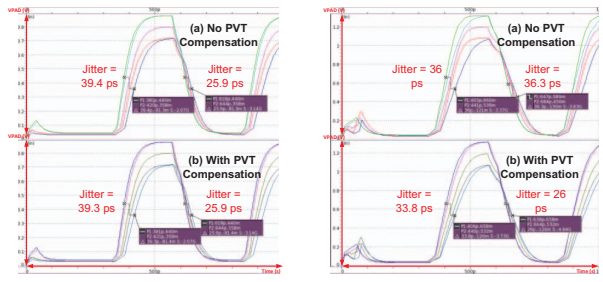
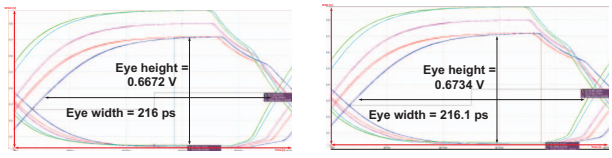


Fig. 8. A 1.2-V VDDIO's PAD output waveform (a) without PVT compensation (worst SR= 12.3 V/ns; best SR= 6.85 V/ns); (b) with PVT compensation (worst SR = 8.85 V/ns; best SR= 6.39 V/ns)



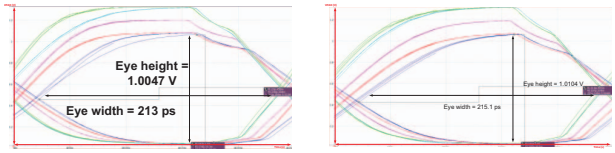
(a) (b)

Fig. 9. Jitter simulations. (a) VDDIO = 0.8 V; (b) VDDIO = 1.2 V.



(a) (b)

Fig. 10. 0.8-V VDDIO's eye diagram (a) without PVT compensation (height = 0.6672 V; width = 216 ps); (b) with PVT compensation (height = 0.6734 V; width = 216.1 ps).



(a) (b)

Fig. 11. A 1.2-V VDDIO's eye diagram (a) without PVT compensation (height = 1.0047 V; width = 213 ps); (b) with PVT compensation (height = 1.0104 V; width = 215.1 ps).

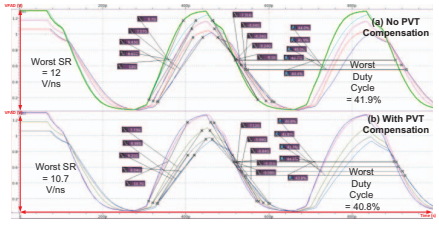


Fig. 12. A 1.2-V VDDIO's PAD output waveform at maximum frequency of 2.6 GHz (worst PVT corner), load capacitance of 20 pF, and laod resistance of 50 ohms (a) No PVT compensation (worst SR= 12 V/ns; best SR = 7.57 V/ns); (b) with PVT compensation (worst SR = 10.7 V/ns; best SR = 6.94 V/ns)

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