A 1-kb Sub-1 fJ/b per Access CAM Design Using 40-nm CMOS Process

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***Abstract*—This investigation presents a low-power content addressable memory (CAM) design using 10T single-ended cells. It uses the single-ended SRAM cell as a memory unit and a single-ended comparison circuit. By adopting this circuit, the proposed CAM cell is the first to have both the read/write and search operation to be in a single-ended mode. An energy reduction by power gating unused column is also presented in this investigation. The proposed CAM is implemented using the typical TSMC 40-nm CMOS logic process. It has an area of 1.4×1.4 mm^2 with a core of 0.89 mm^2. Simulation results show that the energy per bit per search is 0.938 fJ with a search time of 0.47 ns. An FOM comparison based on the search time, energy per bit per search, and supply voltage also showed that the proposed CAM is the best compared to prior designs.**

***Index Terms*—single-ended cell, content addressable memory, low-power, 10T cell, power gating**

I. Introduction

With the introduction of artificial intelligence (AI), its applications to manufacturing processes follow. Industry 4.0 has prepared the way for smart factories, autonomous systems, IoT (Internet of Things), machine learning, and artificial intelligence in the industrial environment [1], [2]. Electronic systems are the most important components of an AI system where storage or memory devices are highly demanded. In this regard, memories enable the system to "remember" information by storing it in a database for processing afterwards.

Common memories include random access memories (RAM) which are categorized into dynamic random-access memory (DRAM) and static random-access memory (SRAM) [3]. Other than RAM, there is another type of memory that is the actual opposite on how it accesses the data. It follows a similar concept in writing, but it differs in accessing the memory. A content addressable memory (CAM) is used in AI systems as a high-speed lookup table [4]. Furthermore, it is used for internet protocol (IP) routing, data management, data compression, image processing, multi-protocol label switching, reconfigurable computing systems, finite state machines (FSM), pattern matching and many more [5], [6]. Considering its computing capabilities, CAM designs have some issues: density scaling, power scaling, and time scaling [7]–[10]. Common implementation of CAMs is mainly in modern digital networking systems [5] and AI systems. Specifically, it is implemented in image processing, IP addressing, multi-protocol label switching (MPLS), data compression and encryption. CAM storages are also proposed as a foundation for a number of computational models such as reconfigurable computing systems and associative computing. It is also used on emerging drive mapping such as FSMs, traversed decision trees, pattern matching, arbitrary logic functions, etc.

This investigation proposes a new CAM cell that uses single-ended access lines, match lines, and search lines to reduce power consumption. A positive feedback amplifier between BLB and BL is used to minimize the delay during read operation. The same amplifier design is used as a match line amplifier to have a full scale match line output voltage. A supply voltage selection is also used to reduce power consumption during standby mode.

II. 1-kb Content Addressable Memory Architecture

The architecture of the proposed 1-kb content addressable memory (CAM) is shown in Fig. 1. The proposed design consists of the following blocks:

- CAM Array: composed of a 32×32 10T single-ended CAM cells
- Supply Voltage Control (SVC): it controls the supply voltage for the CAM array to reduce power consumption
- Control circuit: it is in charge of the timing operation of the system
- Row & Column Decoder: it selects the row/column to where the bits are access and/or searched
- Column Selector: this circuit selects which data bit to be presented at the output of the system
- Address Encoder-Multiplexer: this will show if the selected matched the search data
- Built-In Self-Test (BIST): a self test circuit to ensure that the chip is working through a given internally generated input pattern

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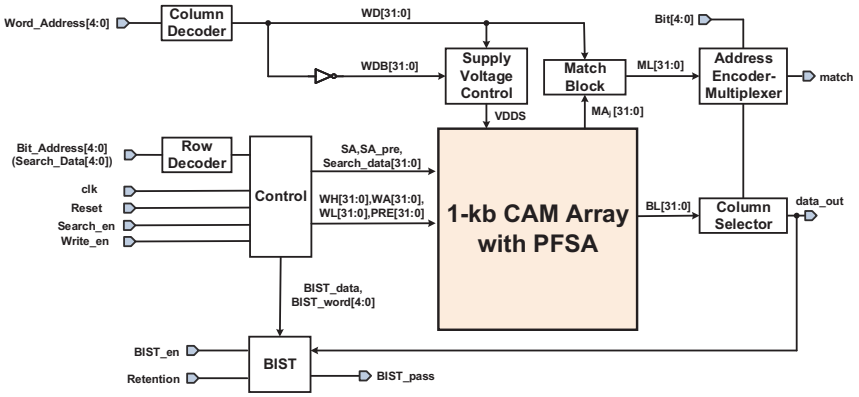

Fig. 1. Proposed 1-kb CAM architecture

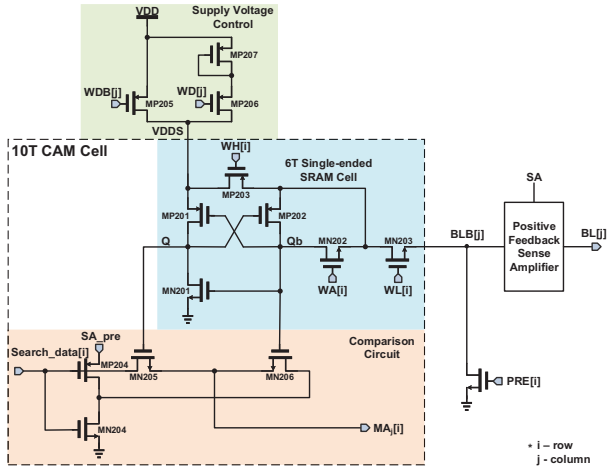

Fig. 2. 10T single-ended CAM cell with Supply Voltage Control (SVC) and positive feedback sense amplifier (PFSA)

TABLE I
6T SRAM CELL OPERATION

	Standby	Write-1	Read-1	Write-0	Read-0
WA[i]	0	1	1	1	1
WH[i]	1	1	1	0	0
WL[i]	0	1	1	0	1
PRE[i]	1	1	0	1	0

i- Row

A. 10T single-ended access and search CAM cell design

Referring to Fig. 2, the CAM cell is a 10T cell with a 6T single-ended SRAM cell together with a comparison circuit consisting of 4 transistors. The cell is based on the report in [11] which addresses the noise rejection performance of existing single-ended SRAM cells [5], [12]. The read and write operation of the single-ended cell is presented in Table I while the search operation is shown in Table II.

One problem of single-ended architectures is that the output lines (bitlines and matchlines) are almost difficult to have

TABLE II
WRITE AND SEARCH OPERATIONS OF CAM CELLS

	Write-0		Write-1	
	Search-0	Search-1	Search-0	Search-1
SA_pre	1	1	1	1
Q	0	0	1	1
Qb	1	1	0	0
Search_data	0	1	0	1
MA	1	0	0	1

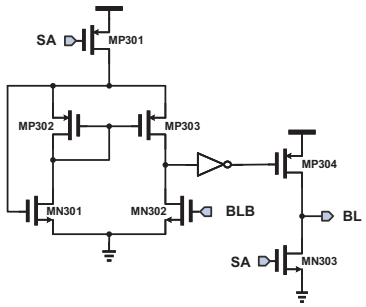

Fig. 3. Positive Feedback Sense Amplifier (PFSA))

a full-swing. A Positive Feedback Sense Amplifier (PFSA) is used to resolve this issue, which is shown in Fig. 3. The bitline (BLB) is fed through the amplifier to have a decoupled output bitline (BL) that can be accessed during read operation. Transistor MP301 acts as a gating transistor to enable the sense amplifier. When MP301 is turned on, MN301 and MN302 will have a large open-loop differential gain with MP302 and MP303 as its load. To further increase the gain, a positive feedback towards MN301 is used. This ensure that the amplifier reaches saturation faster compared to a typical op-amp.

B. Supply Voltage Control

In order to reduce power consumption, a Supply Voltage Control (SVC) is used for the entire column of CAM cells.

The SVC is a power gating strategy that is used when the corresponding column is in standby operation.

C. Timing operations: Read, Write, and Search Modes

Table II summarizes the conditions during read/write and search operations. A more detailed view of how the timing of the proposed design are presented in Fig. 4 and 5. For this example, the values 32'h2 and 32'h3 are saved in the word addresses 32'h25 and 32'h10, respectively. The operation for this example is as follows:

1) *Write Mode*: During write mode, Write_en is activated. Then the addresses are changed and the input data is saved. For this example, the data 32'h2 is written into address 32'h25. Then, after one clock cycle, 32'h3 is written into address 32'h10.
2) *Read Mode*: Once Write_en is deactivated, the system enters the read mode, if Search_en is not initiated as shown in Fig. 4. For this example, the first address selected during read mode is 32'h25 and Bit[1] (or 2nd LSB) is selected. Since address 32'h25 contains 32'h2, and the 2nd LSB of it is '1'. Hence, data_out will generate '1'. Then after one clock cycle, the same address (32'h25) and the 4th LSB (Bit[5]) is selected. The output '0' is then generated at data_out. For the following cycles, the address is changed from 32'h10 and select bits 0, 2, and 7 and data_out generates '1', '1', and '0', correspondingly.
3) *Search Mode*: Search mode is initiated when Write_en is deactivated and Search_en is activated as shown in Fig. 5. For instance, a data of 32'h4 is searched on address 32'h25 and gives a mismatch (match = 0), since that address contains a 32'h2. When 32'h2 is searched on address 32'h25, it will generate a match (match = 1) at the output. Correspondingly, when 32'h2, 32'h10 and 32'h3 is searched from address 32'h10, the output will generate 0, 0, and 1, respectively, since address 32'h10 contains a 32'h3.

III. Implementation and Simulation

The proposed CAM is implemented using TSMC 40-nm CMOS logic process. Fig. 6 shows the layout of the proposed CAM design. It has a chip size of 1.4×1.4 mm^2 and a core of 0.94×0.95 mm^2. Fig. 7 is the layout of the CAM cell.

In order to validate the functionality of the proposed design, an all-PVT-corner post-layout simulation is carried out: 5 process corners (TT, FF, FS, SF, SS), 3 voltage corners (0.9 V, 0.81 V, 0.99 V), and 3 temperature corners (25 °C, 0 °C, 75 °C). Fig. 8 shows the all-PVT-corner simulation results. The worst search delay is 0.47 ns at the SS corner, 0 °C, VDD of 0.81 V at a clock frequency of 100 MHz. The proposed CAM can also operate at a maximum frequency of 800 MHz at 60 pF load.

Table III shows the comparison with recent CAM designs published in the last decade. Ref. [13]–[16] used a predictive 45-nm technology while ours used a TSMC 40-nm CMOS technology. Our design offered the lowest energy bit per search

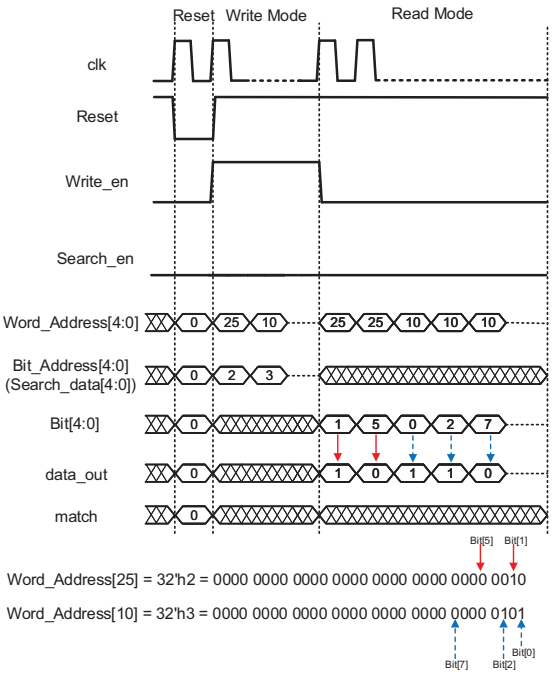

Fig. 4. Write and Read timing diagrams of the proposed CAM

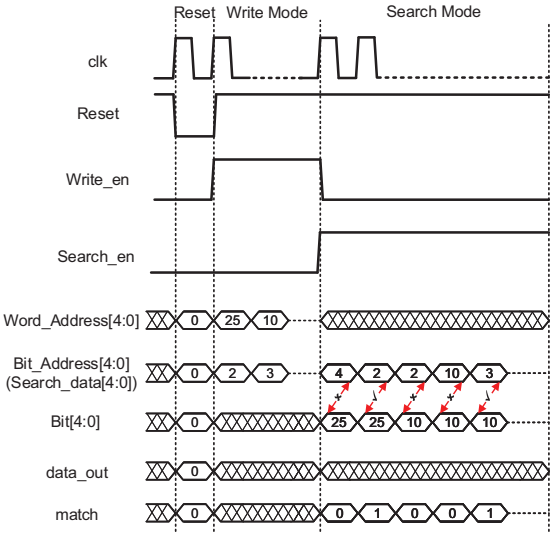

Fig. 5. Search mode timing diagram of the proposed CAM

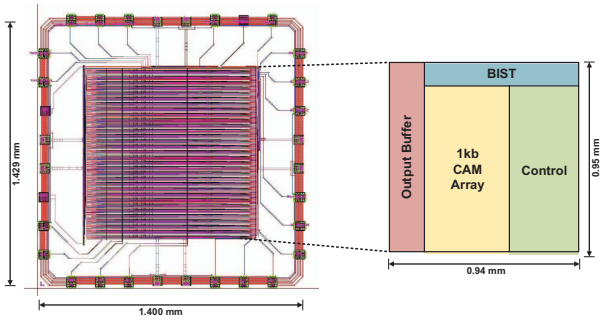

Fig. 6. Layout of the proposed 1-kb CAM

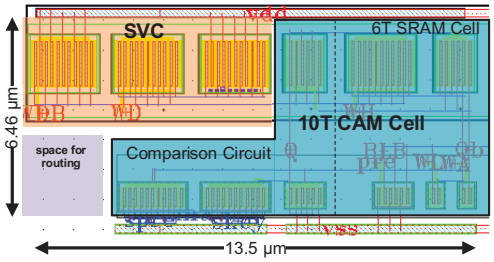

Fig. 7. Layout of a CAM cell

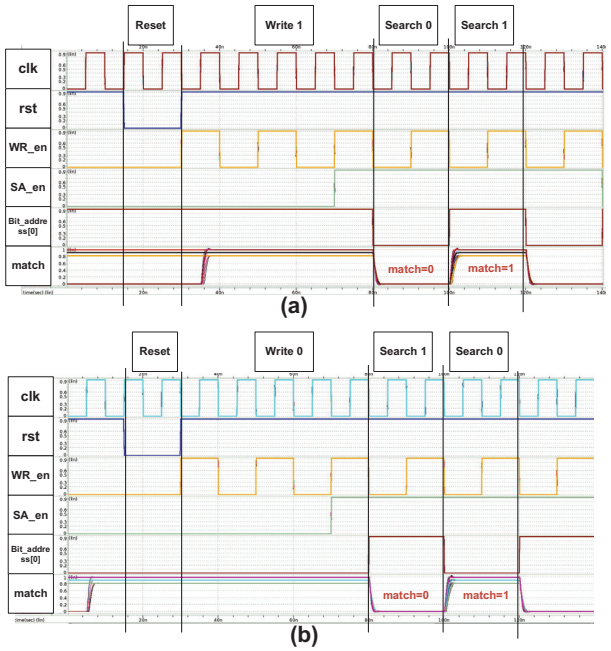

Fig. 8. All-corners post-layout simulation results (a) Write-1 then Search operation (b) Write-0 then Search operation

with a value of 0.938 fJ/bit/search. A Figure-of-Merit (FOM) is also derived to compare the different works. The FOM is based on the search time, energy per bit per search, and the supply voltage. The table shows that the proposed CAM has the lowest FOM so far. Fig. 9 shows the technology roadmap of the different CAMs.

IV. Conclusion

A 1-kb low power CAM is proposed in this investigation. It is composed of a single-ended 10T CAM cell for both access and search operations. A power gating technique is used for cells that are not being accessed or searched. To have a full swing when accessing the cells, a Positive Feedback Sense Amplifier is also proposed. An all-PVT-corner simulation shows that it uses 0.938 fJ energy per bit during search operation. An FOM is also proposed to compared the design with recent CAM designs. Our design offer the lowest FOM to date.

TABLE III
Comparison with prior CAM designs

	[13]	[14]	[15]	[16]	Ours
Year	2016	2017	2019	2020	2023
Publication	TCAS-I	TVLSI	iSES	ICECE	
Process (nm)	45	45	45	45	40
Cell	9T	13T	10T	12T	10T
Supply (V)	1.0	1.0	1.0	1.0	0.9
Capacity (kb)	4.0	4.0	2.0	4.0	1.0
Word size	128	128	64	128	32
Search time (ns)	0.43	1.25	0.56	3.58	0.47
[1]EbS (fJ/b)	1.72	2.1	0.83	0.17	0.938
[2]Normalized EbS	1.82	2.1	0.83	0.17	1.16
[3]FOM	0.74	2.625	0.465	0.609	**0.441**

[1]Energy per bit per search
[2]Normalized EbS = EbS / Supply Voltage [2]
[3] FOM = Search time × Normalized EbS

Fig. 9. CAM technology roadmap

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