2-Level Miller Detection-based High Side Gate Driver Design for Power MOSFETs

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***Abstract*—The gate driver design for power semiconductor devices affects overall efficiency and performance. This research presented an AGD (active gate driver) that detects the Miller plateau during the driving signal's turn-on and turn-off using a 2-level Miller detector. It has a power gating mechanism that reduces the power consumption of the AGD. Furthermore, the Equalizer in the AGD ensures that all MOS devices in the buffer arrays are utilized. The AGD design has been implemented in TSMC 0.18-μm HV CMOS (T18HVG2) process. The functionality of the AGD design was verified by the all-PVT-corner post-layout simulations with C_{load} = 2 nF and an operating frequency of 500 kHz. It has an average combined static and dynamic power dissipation of 288.8 mW. Finally, the power gating mechanism provides a 65.9 mW static power reduction based on two cycles comparison (with and without power gating).**

***Index Terms*—AGD, Miller plateau, power gating, equalizer, power MOSFET**

I. Introduction

Power semiconductor devices, such as SiC and GaN, play a vital role in the evolution of power electronics technology towards higher power density, better efficiency, and more integrated systems [1]. However, the design of power semiconductor gate drivers affects their performance and efficiency. It must be optimized to achieve its best switching performance. In addition, the gate driver must maintain low switching loss and can suppress oscillations.

A resistive gate driver (RGD) is a circuit that can reduce the surge voltage, surge current, and switching loss during the transition by adjusting the switching waveform through gate resistance (R_g) [2]. However, its waveform adjustment is limited. Active gate driver (AGD) was reported to suppress EMI and increase power efficiency for different power semiconductor devices [3].

The use of microcontrollers and FPGAs for AGD design efficient driving was reported [4] [5]. However, the models need to be reprogrammed based on the characteristics of different power devices and don't have real-time output data. It consists of multiple chips that make it bulky and requires expensive data processors for a heavy computational work load. A dynamic gate driver IC monitors the V_g of the SiC power MOSFET during switching transients to generate an optimized dynamic R_g pattern [6]. This system detects the end of the Miller plateau, providing a duration for the new gate driving pattern. The dynamic gate drive automatically suppresses ringing while maintaining a fast switching speed. The FPGA, however, processed the optimized timing configuration for the gate driver IC, increasing its complexity, costs, and area.

In this work, an AGD design uses 2-level Miller detection to detect the Miller plateau during power MOSFET on and off. The Miller plateau is observed based on the V_{gs} and V_{ds} of the power MOSFET, improving the detection accuracy. The proposed AGD is implemented in 0.18-μm HV CMOS, eliminating the area limitation of the AGD that uses a microcontroller and FPGA. The driver's power gating approach reduced the power loss generated by Voltage level shifter.

II. 2-Level Miller Detection-based High Side Gate Driver Design

Fig. 1 illustrates the block diagram of the proposed AGD. The 2-level Miller detector identifies the Miller plateau through V_{gs} and V_{ds}. It has a power gating circuit that generates V_{PG}, turning off N-1 PMOS in the buffer array when $V_{gs} \geq 0.8\ V_{DD}$, reducing the power loss generated by Voltage level shifter. The Adaptive split-path feedback circuit generates two independent signals, V_{PWMP} and V_{PWMN}, to avoid a shoot-through between NMOS and PMOS buffer array during the transition. The Equalizer randomizes the selection of which position of N-1 PMOS to be turned off, ensuring the current is distributed equally among all the PMOS in the buffer array. The UDDSP (user-defined drive strength profile) selector determines the number of PMOS and NMOS devices in the buffer arrays that are off during the Miller plateau. The NMOS and PMOS switch selectors generate gate drive signals for the NMOS and PMOS buffer arrays, respectively. The Delay matching compensates for the delay caused by Voltage level shifter. Voltage level shifter adjusts PMOS voltage gate signal from $0 \sim 5$ V to $5 \sim 10$ V, since the PMOS in the T18HVG2 process requires a floating reference voltage. The "N" number of NMOS and PMOS in the buffer array produces different drive strengths in the Miller plateau. The PMOS buffer array and Voltage level shifter use V_{DD} = 10 V (V_{DDH}), and other sub-circuits use 5 V (V_{DDL}).

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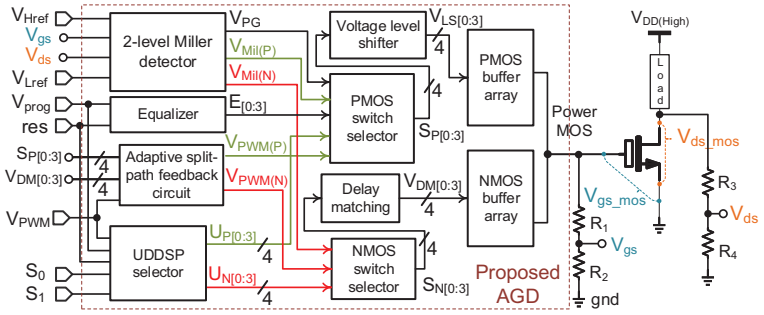

Fig. 1. Block diagram of the proposed AGD

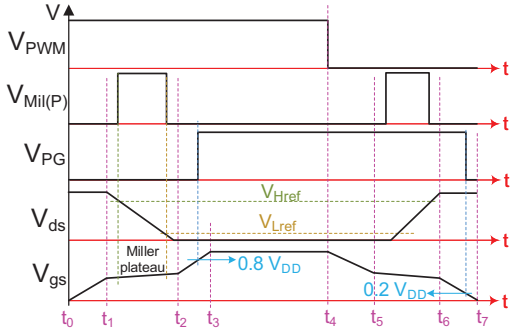

Fig. 2. Proposed AGD timing diagram

Fig. 2 shows the timing diagram for the proposed AGD. During turn-on, V_{gs} starts to rise when V_{PWM} is high. Ideally, when V_{ds} starts to drop, V_{gs} enters the Miller plateau until $V_{ds} = 0$. However, V_{Href} (0.8 V_{ds}) and V_{Lref} (0.2 V_{ds}) are used to detect the miller plateau from the V_{ds} signal. This will generate a smaller Miller plateau $V_{Mil(P)}$ to avoid the noisy regions above V_{Href} and below V_{Lref}, which results in a stable waveform. The same process happens during turn-off. When V_{ds} starts to rise above V_{Lref}, $V_{Mil(N)}$ is generated until $V_{ds} \geq V_{Href}$. V_{PG} turns off N-1 PMOS devices when $V_{gs} \geq 0.8\ V_{DD}$ and resets once if $V_{gs} \leq 0.2\ V_{DD}$ to reduce power loss.

A. 2-level Miller detector and Equalizer

The 2-level Miller detector shown in Fig. 3 detects the Miller plateau based on signals V_{gs}, V_{ds}, V_{Href}, and V_{Lref}. During turn-on, the Miller plateau is detected when both Q_{gs} and Q_{ds} are high through $V_{Mil(P)}$, which controls the PMOS buffer array. Miller plateau is detected during turn-off when both Q'_{gs} and Q'_{ds} are low through $V_{Mil(N)}$, which controls the NMOS buffer array. Summarized in Table I are the three cases for the 2-level Miller detector, where the Miller plateau occurs during case 2.

The power gating signal is generated from the V_{gs} window detector. It detects when $V_{gs} \geq 0.8\ V_{DD}$, generating a control signal to turn off N-1 PMOS devices for static power reduction. When $V_{gs} \leq 0.2\ V_{DD}$, the power gating resets

TABLE I
CASES FOR 2-LEVEL MILLER DETECTOR

Case	V_{ds}	Q_{gs}	Q_{ds}	$V_{Mil(P)}$,$V_{Mil(N)}$
1	$V_{ds} > V_{Href}$	0	0	0, 1
2	$V_{Lref} < V_{ds} < V_{Href}$	1	1	1, 0
3	$V_{ds} < V_{Lref}$	0	0	0, 1

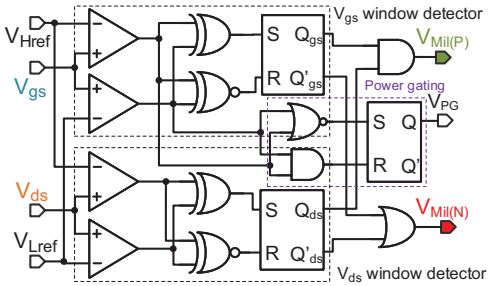

Fig. 3. 2-level Miller detector schematic

TABLE II
TIME CONSTANT VS $\%V_{max}$ AND $\%I_{max}$ IN RC CIRCUIT

τ ($R_g \cdot C_g$)	$\%V_{max}$	$\%I_{max}$
1.0	63.2	36.8
2.0	86.5	13.5
3.0	95.5	5.00
4.0	98.2	1.80
5.0	99.3	0.79

for the next cycle. Tabulated in Table II is the relationship of voltage, current, and time constant (τ) in an RC circuit, where R_g and C_g are the buffer resistance and capacitance of the power MOS, respectively. The required current to fully charge the capacitor decreases as the voltage across the capacitor increases. The proposed AGD uses N = 4 buffers in the PMOS buffer array. In this case, a single PMOS device can produce 25 % of I_{max}, enough to fully charge C_g when it reaches 0.8 V_{DD}. Thus, the power gating turns off N-1 PMOS devices in the buffer array when the voltage across C_g = 0.8 V_{DD} for power reduction.

The Equalizer consists of a programmable parallel-in-parallel-out (PIPO) shift register as illustrated in Fig. 4. It

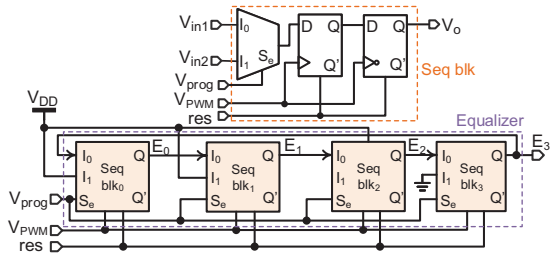

Fig. 4. Equalizer circuit

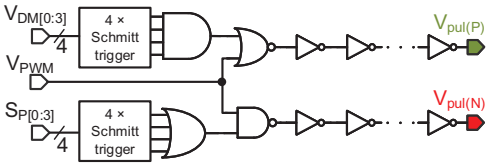

Fig. 5. Adaptive split-path feedback circuit

uses V_{PWM} as the clock signal to generate different switch selection sequences every cycle for both NMOS and PMOS buffer arrays. This makes sure that all the MOS devices in the arrays are equally utilized, avoiding any mismatch due to the overuse of one specific MOS. V_{prog} signals load the sequence data into the DFF array. The "res" signal reset the DFFs in the equalizer to the default state ($E_{[3:0]}$=0000) during the initial turn-on.

B. Adaptive split-path feedback circuit and UDDSP selector

The Adaptive split-path feedback circuit shown in Fig. 5 produces the dead time between NMOS and PMOS buffer arrays during transitions. It detects the buffer with the slowest rise-time/ fall-time amongst the buffer arrays. Once it detects the slowest buffer, the CMOS Schmitt trigger compensates it by producing an extra delay for the other buffers. The threshold values for the Schmitt trigger are 0.7 V_{DD} (V_{TON}) and 0.3 V_{DD} (V_{TOFF}). The PMOS buffer array will turn on once if the NMOS buffer array is turned off, and vice-versa. The dead time for the rising edge ($t_{dt(r)}$) and falling edge ($t_{dt(f)}$) based on Table II can be determined using Eqn. (1).

$$\begin{aligned} t_{dt(r)} &= T_{d\_cell} + 1.5 \cdot R_g \cdot C_g \\ t_{dt(f)} &= T_{d\_cell} + R_g \cdot C_g \end{aligned} \tag{1}$$

where $T_{(d\_cell)}$ is the delay produced by the inverter chain.

UDDSP ensures that the PMOS and NMOS buffers has a proper drive strength during the Miller plateau. Fig. 6 shows the UDDSP circuit which includes an equalizer and mode decoder that converts $S_{[0:1]}$ into sequence data. Table III summarizes the list of sequence data for the buffer arrays.

During turn-on, when $U_{P[0:3]}$ = 0000, all the PMOS devices in the buffer array is on. A non-zero value in $U_{P[0:3]}$ turns off a corresponding PMOS device in the buffer array. $U_{N[0:3]}$ follows the same concepts with inverted logic during turn-off. The Equalizer performs a right shift operation on the sequence data at the negative edge of the V_{PWM}.

TABLE III
UDDSP SEQUENCE DATA FOR THE PMOS/NMOS BUFFER ARRAY

	$U_{P[0:3]}$, $U_{N[0:3]}$			
Mode	Cycle 1	Cycle 2	Cycle 3	Cycle 4
0	0000, 1111	0000, 1111	0000, 1111	0000, 1111
1	1000, 0111	0100, 1011	0010, 1101	0001, 1110
2	1100, 0011	0110, 1001	0011, 1100	1001, 0110
3	1110, 0001	0111, 1000	1011, 0100	1101, 0010

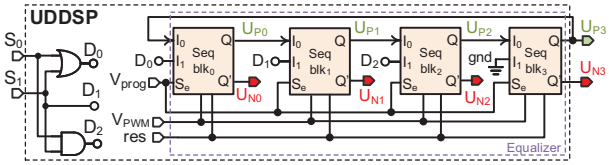

Fig. 6. UDDSP schematic

C. Other auxiliary circuits

The NMOS and PMOS switch selector illustrated in Fig. 7 (a) and (b), respectively, identify which NMOS and PMOS from the buffer arrays are turned on/off during the Miller plateau (NMOS and PMOS switch selectors) and power gating (PMOS switch selector). Signal $U_{N[0:3]}$ for the NMOS switch selector determines the position and number of NMOS active in the buffer array during the Miller plateau. If $U_{N[0:3]}$ = 0000, $V_{DM[0:3]}$ equals $V_{pul(N)}$. In the PMOS switch selector, $U_{P[0:3]}$ has the same function as $U_{N[0:3]}$. $E_{[0:3]}$ determines the position of PMOS in the array buffer in the power gating (V_{PG}) region. Dummy logic matches the transmission delay in each switch selector. To properly drive the PMOS buffer array, the Voltage level shifter adjusts $S_{P[0:3]}$ from 0 $\sim$ 5 V to 5 $\sim$ 10 V [7]. Referring to Fig. 1, Delay matching uses a series of inverters to compensate for the delay generated by Voltage level shifter.

III. SIMULATION AND ANALYSIS

Fig. 8 shows the proposed AGD circuit layout implemented using TSMC 0.18 μm HV CMOS process. It has an overall chip area of 5.26 $\times$ 1.05 mm^2 and a 4.79 $\times$ 0.83 mm^2 core area. Fig. 9 shows the all-PVT-corner post-layout simulation output waveforms. The V_{gs} from Infineon IRF130 100 V MOSFET was introduced into the AGD to verify Miller plateau detection [8]. Furthermore, a C_{load} = 2 nF during the simulation is used at an operating frequency of 500 kHz. The V_{PWM} switches from 0 $\sim$ 5 V, while V_{LS0} and V_{LS01} are shifted to 5 $\sim$ 10 V. Both V_{gs} and V_{ds} varied from 0 to 5

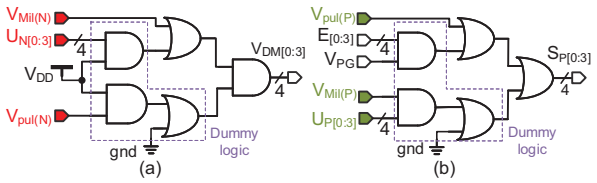

Fig. 7. (a) NMOS and; (b) PMOS switch selector

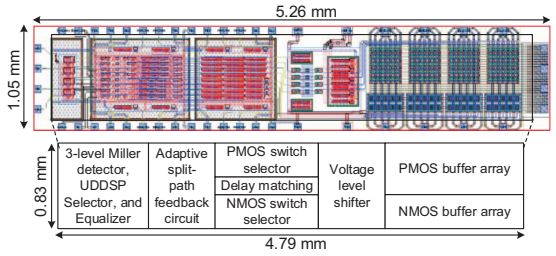

Fig. 8. Layout of the proposed AGD

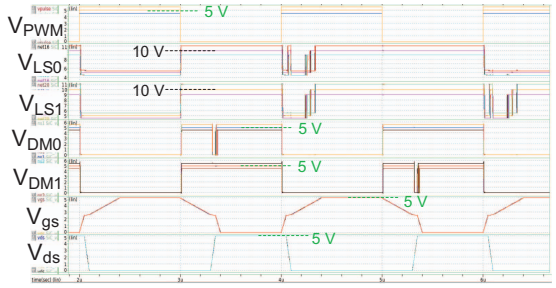

Fig. 9. Proposed AGD All-PVT-corner post-layout simulation

V because the comparators and other circuits work faster at lower node voltages.

The detailed operation of the proposed AGD is shown in Fig. 10 at $S_{[01]}$ = 01 (mode 01). In this mode, only a single MOS in either buffer array responds to $V_{Mil(N)}$ and $V_{Mil(P)}$. Notably, the Equalizer selects different MOS device for each cycle. For the PMOS buffer array, V_{LS0} = 1 at cycle 2, and V_{LS1} = 1 during cycle 3. The selection also occurs in the NMOS buffer array. Miller plateau is detected when both V_{gs} and V_{ds} are in transition between V_{Href} and V_{Lref}, resulting in 2-level detection. Using two variables, V_{gs} and V_{ds}, improves the accuracy of Miller plateau detection. Also, during the Miller plateau, V_{LS} = 0 and V_{DM} = 1 because of the complementing control logic of PMOS and NMOS.

Fig. 11 shows the effect of power gating in the AGD. The first cycle doesn't have power gating detection having higher static power dissipation P_{dis} of 202 mW because all the MOS devices in the PMOS buffer array is on for $T_{PWM(on)}$ = 1 μs.

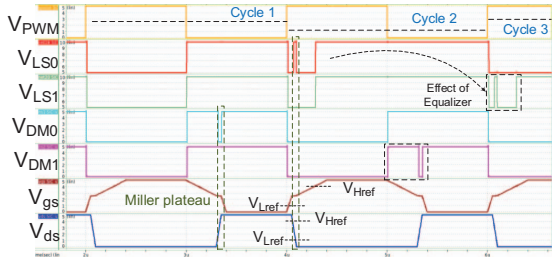

Fig. 10. TT, V_{DDH} = 10 V, and V_{DDL} = 5 V, at 25°C post-layout simulation

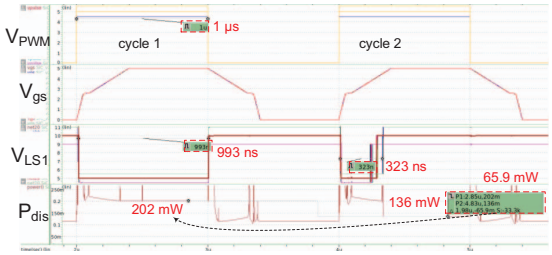

Fig. 11. Effect of power gating at FF, 1.1· $V_{(DDH,L)}$, and 0°C

TABLE IV
PERFORMANCE COMPARISON

	[9]	[6]	This work
Year	2018	2022	2023
Publication	JSSC	ISPSD	
Technology (μm)	0.18 BCD	0.18 BCD + FPGA	0.18 T18HVG2
Driver type	Passive	Active	Active
Verification	Meas.	Meas.	Post-sim.
V_{DD} (V)	15	1.8, 3.3 & 20	5 & 10
f_{PWM} (MHz)	1	0.1	0.5
t_{rise} (ns)	5.6 at 5 V	—	28.4 at 10 V
t_{fall} (ns)	—	—	36.1 at 10 V
C_{load} (nF)	2.7	2	2
Chip area (mm^2)	4.9 x 2.3	2.5 x 2.5	5.26 × 1.05
P_{dis_total} (mW)	—	79.51*	288.8

*not including FPGA power

The effect of power gating in cycle 2 reduced the $T_{PWM(on)}$ to 323 ns and P_{dis} to 136 mW. The reduced static power caused by power gating is 65.9 mW (36.2%).

Table IV summarizes the literature comparison for power MOS driver design. Compared to [6], our AGD doesn't use FPGA for optimal driving. It has a t_{rise} and t_{fall} of 28.4 ns and 36.1 ns, respectively. The total average power dissipation (P_{dis_total}) of 288.8 mW is the combined static and dynamic power during the complete six cycles; 4 different sequences for mode, 1 for mode data loading, and 1 for without the power gating.

IV. Conclusion

This paper demonstrates an AGD design for power MOSFET devices implemented in the 0.18-μm CMOS (T18HVG2) process. The 2-level Miller detection accurately detects the Miller plateau through V_{gs} and V_{ds} of the power MOSFET devices. It has a power gating mechanism that improves the power loss generated by the voltage level shifter. The performance of the proposed AGD is verified through all-PVT-corner post-layout simulation with the worst corner values of t_{rise} = 28.4 ns, t_{fall} = 36.1 ns, and an overall six cycles average power dissipation of 288.8 mW at an operating frequency of 500 kHz.

Acknowledgment

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