Passiveless Digitally Controlled Oscillator With Embedded PVT Detector Using 40-nm CMOS

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***Abstract*—This paper presents a design of a digitally controlled oscillator (DCO) with a build-in PVT (process, voltage, temperature) variation sensor using a 40-nm CMOS process. The DCO is designed using a 128-stage differential ring oscillator wherein the number of stages is being controlled by an input of 7-bit digital code. It is further realized using serpentine style arrangement to minimize variation on wafer. A multiplexed PVT sensor is integrated to provide a way to feedback for output correction using any auto-calibration strategy, e.g., PID control or artificial intelligent control. A linearized model of the DCO is presented based on the results of the post-layout simulations. The DCO has a dynamic range of 9.9 MHz to 527.43 MHz. The DCO is designed to operate at the frequencies –20 °C to 75 °C. The overall chip consumes 0.235 mW from a 0.9 V supply. The overall chip area is 0.67 mm^2 with a core area of 0.05 mm^2. The all-PVT-corner post-layout simulations show a highly linear fit for the period vs. input code with the worst R^2 of 0.992 in the SS corner at 0.99 V supply and 25 °C.**

***Index Terms*—DCO, PVT detector, feedback, delay element, CMOS**

I. Introduction

An oscillator is an electronic circuit that generates a periodic signal, usually in a form of sinusoidal wave or pulse train. For instance, those periodic signals generated by oscillators are widely used in broadcast radio & TV stations transmitters, local oscillators (LO) in receivers, energy harvesting circuits, and digital clock signals for computers. It is particularly important in the design of low power transceivers such as in handheld and IoT devices. The oscillator of timing circuits are considered to be a limiting factor both for spectrum efficiency and power consumption [1].

Modern semiconductor manufacturing processes are much more complex, where any variation in the process may cause corresponding variations in components on an integrated circuit. When transistors become smaller, the impact of any variation can be a cause of major failures. More specifically, the performance of an integrated circuit will be heavily affected by process (P), voltage (V), and temperature (T) variations. For processes more advanced than 90-nm process, the leakage becomes a major problem especially in low power applications [2], [3]. Device leakage is directly affected by the aforementioned parameters. This problem is even worse when there are passive devices included in a clock generator circuit. Hence, using a fully digital architecture may improve the overall performance.

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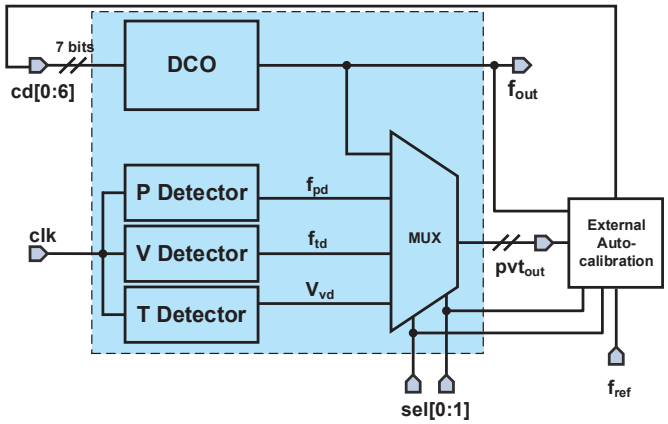

Fig. 1. DCO with an embedded PVT detector

TABLE I
System Operation

Select (sel[0:1])	Operation
0 0	DCO
0 1	Process Detector
1 0	Voltage Detector
1 1	Temp. Detector

Fig. 1 shows the overall architecture of the DCO with the embedded PVT detectors. The four circuits are multiplexed providing for the information of the output frequency of the DCO and the detected PVT corners. The output generates 6-bit code as well as analog frequency and voltage according to the selection codes, sel[0:1]. Table I summarizes the operations of the system.

The rest of the paper is organized as follows: Section II details the design of the digitally control oscillator free of passive devices. Section III discusses the process, voltage, and

temperature (PVT) sensors used. Simulation results are presented in Section IV, the external auto-calibration is discussed in Section V, and a conclusion is given in Section VI.

II. Passiveless DCO Design

The DCO schematic details in Fig. 1 are presented in Fig. 2. It is composed of a differential ring oscillator that uses transmission gate switches to create a feedback controlled by a digital signal. The number of delay stages determines the output frequency of the DCO. The larger the decimal equivalent of the selection code, the more delay stages are being fed back to the first stage of the circuit, thus making the output frequency slower. Differential delay cells are chosen for the design taking into account because of the advantages in frequency stability, common-mode noise reduction, even-order distortion rejection, and high phase noise immunity [4]. Referring to Fig. 3, the differential delay cell used in the DCO is shown. It is composed of a differential current-starved inverters, where the outputs are attached to cross-coupled inverters INV0 and INV1. These inverters are included to provide a full swing output of the delay cells. MP0 and MN0 are the current source of the differential inverters. All delay cells have their own bias circuit to provide for V_{b1} and V_{b2} for each cell.

III. PVT Detectors

Referring to Fig. 4, the detectors embedded in the chip are shown. A process dependent detector, as shown in Fig. 4 (a) is used as a process variation detector based on the report [5]. Fig. 4 (b) shows a time-digital converter used as a voltage detector and Fig. 4 (c) shows a temperature detector based on a temperature to frequency converter reported in [6].

A. Process Detector

Fig. 4 (a) shows the process detector used in the system. It is composed of a 6-stage ring oscillator with alternating stages of delay cells composed of NMOS-based inverter and a typical CMOS inverter. The NMOS-based inverters provide different delays to sense N-process variations. The typical CMOS inverters include PMOS devices with forward-body bias to detect the P-process variations. The output oscillation is then fed to a counter to convert the oscillation count into a 6-bit digital code.

B. Voltage Detector

Fig. 4 (b) presents the block diagram of the voltage detector, composed of three parts: buffer delay line, delay element, and delay decoder. The delay element will have shorter or longer delay depending on the variation of VDD. A current starved delay element is used in this design, since it has symmetric load to provide a good linearity [7]. The delay decoder is designed to detect voltage variation from VDD, and VDD $\pm$10% VDD. The generated codes represents a 3-bit code output.

C. Temperature Detector

The schematic diagram of the temperature detector is shown in Fig. 4(c) based on the report in [6]. It consists of a current generation circuit, a charge/discharge circuit, and a voltage window comparator. The temperature dependence of the current generation circuit output on MN406 is given by Eqn. (1).

$$\frac{\partial I_{out}}{\partial T} = -\frac{V_{GS(MN405)} - V_{GS(MN406)}}{R} \cdot \frac{\partial R}{\partial T} + \frac{1}{R}\left(\frac{\partial V_{GS(MN405)}}{\partial T} - \frac{\partial V_{GS(MN406)}}{\partial T}\right) \quad (1)$$

where R is the current generation resistance, and I_{out} is the current along R and MN406.

IV. Implementation and Simulation

The proposed system is implemented using a typical 40-nm CMOS process. The overall layout is 817$\times$817 μm^2 with a core of 221.13$\times$217.36 μm^2. The DCO covers a 100$\times$100 μm^2, as shown in Fig. 5, which is realized using serpentine configuration to minimize layout variation as claimed in [8].

Table II summarizes the decimal equivalent of the output of the process detector. It is the number of pulses produced by the process dependent oscillator. Fig. 6 shows the all-PVT-corner post-layout simulations showing the output frequency from the process detector. The effects of temperature and voltage variations are also shown in the graph. It can be inferred from the plots that the output frequency is increasing as VDD increases. Fig. 7 shows the all-process simulation results for the voltage detector. It shows that the designed voltage detector can distinguish VDD, and VDD $\pm$10% VDD. Fig. 8 shows the post-layout simulations of the frequency output of the temperature detector vs. temperature in the different corners. It shows a linear relationship to which the fitted curves of each corner as presented in Table III. Referring to Fig. 9, the 45 corners simulation is shown to discriminate the 5 different corners. It is consistent with Fig. 8.

Fig. 10 shows the 45 all-PVT-corner simulations of the output period of the DCO. It can be seen that the period is linear in reference of the input code. Modeling the DCO output in the form of Eqn. (2), where x is the input code, it can be summarized that the slope, k_1, highly depends on the process corners. The slopes of all the process corner lines are as follows: SS = 0.0007, FS = 0.0005, TT = 0.0004, SF = 0.0003, and FF = 0.0002. This means that voltage and temperature variation mainly affects the y-intercept of a linear model. The worst curve fit from the 45 corners is an R^2 of 0.992 at the SS process, VDD of 0.99 V, and 25°C corner.

$$T = k_1 \cdot x + k_2 \quad (2)$$

Fig. 11 shows the simulated phase noise of the DCO in the range of 100 Hz to 30 MHz. The computed phase jitter is 1.98 ps by the simulation results.

The proposed design consumes an overall power of 0.235 mW at 100 MHz from a 0.9 V supply voltage.

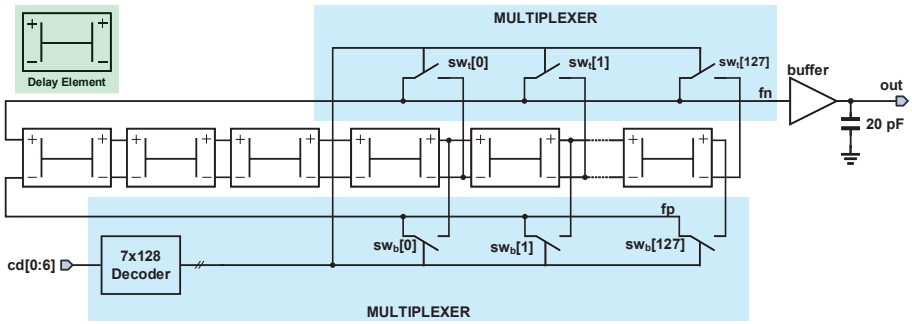

Fig. 2. Differential oscillator architecture

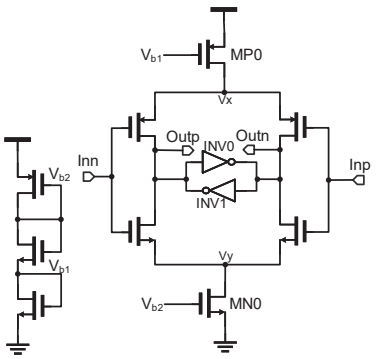

Fig. 3. Differential delay cell of the DCO

TABLE II
ALL-PVT-CORNER SIMULATIONS OF THE PROCESS DETECTOR (ALL ENTRIES ARE DENOTED BY DECIMAL EQUIVALENT)

	VDD = 0.81 V			VDD = 0.9 V			VDD = 0.99 V		
	T_1	T_2	T_3	T_1	T_2	T_3	T_1	T_2	T_3
FF	13	13	13	14	14	15	19	19	17
TT	5	6	7	8	9	9	10	10	10
FS	5	5	5	7	7	6	11	11	10
SF	2	3	5	5	5	7	4	9	10
SS	1	1	3	3	3	5	5	6	7

Note: $T_1 = 0°C$, $T_2 = 25°C$, $T_3 = 75°C$

V. FUZZY LOGIC EXTERNAL AUTO-CALIBRATION

Fuzzy logic is an artificial intelligence method to predict system output by imitating human reasoning. Instead of using a binary system which only have 2 cases of truth (1's or 0's), fuzzy logic uses intermediate degrees of truth. Referring to Fig. 12, it shows the block diagram of the fuzzy logic systems to be used for auto-calibration. There are two fuzzy systems in placed for this setup. First, a fuzzy system to predict the input to be fed to the DCO. It will accept the frequency output coming from the process and temperature sensor as well as the detected voltage. The output from the PVT sensors (pvt_{out}) are demultiplexed to be match with the individual sensors in Fig. 1. Fig. 13 shows the surface plots based on the rules of the system. Once the input code is predicted, the DCO will oscillate based on the input codes to the DCO. Another fuzzy

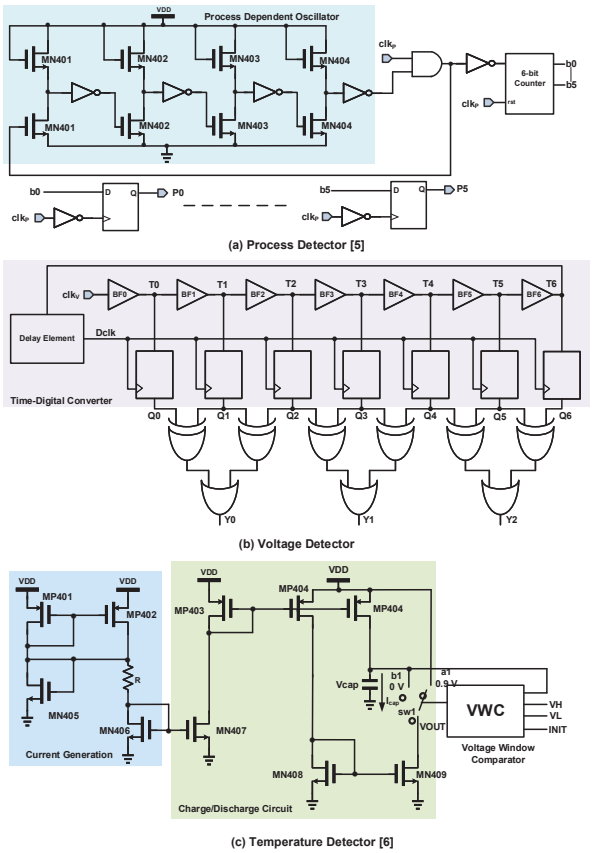

Fig. 4. Embedded Detectors: (a) Process Detector; (b) Voltage Detector; (c) Temperature Detector

system is then used at the feedback to correct the codes when the frequency is different from the reference frequency.

VI. CONCLUSION

A digitally controlled oscillator (DCO) implemented in 40-nm CMOS process is presented in this study. A build-in process, voltage, and temperature detector is included on chip for auto-calibration purposes. The proposed design shows a very small jitter of 1.98 ps with phase noise of -132 dBc/Hz at 1 MHz with a carrier frequency of 100 MHz. The DCO is

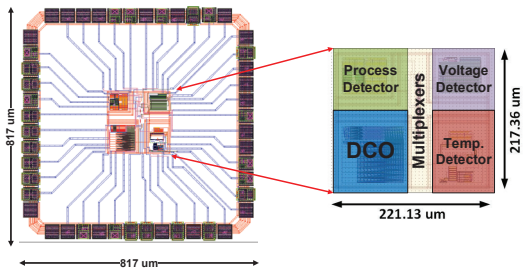

Fig. 5. Chip layout

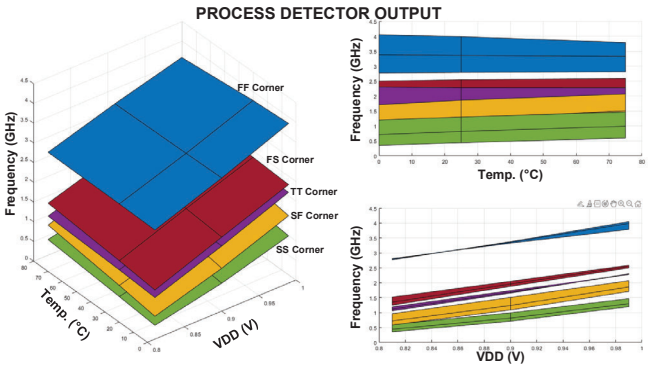

Fig. 6. Post-layout simulations of Process detector (Output frequency)

highly linear and the inclusion of the PVT detectors increase its controlability. The proposed design shows the lowest power and jitter compared with several prior fully digital designs in Table IV.

TABLE III
CURVE FIT FOR THE TEMPERATURE DETECTOR OUTPUT

Corner	Equation	R^2
TT 0.90	$f = 0.4509 \cdot T + 1.6576$	0.9939
TT 0.99	$f = 0.4528 \cdot T + 1.6476$	0.9934
TT 0.81	$f = 0.4345 \cdot T + 1.6017$	0.9940
FF 0.90	$f = 0.6176 \cdot T + 3.0967$	0.9971
FF 0.99	$f = 0.6231 \cdot T + 3.0347$	0.9965
FF 0.81	$f = 0.6099 \cdot T + 3.0335$	0.9971
SS 0.90	$f = 0.2851 \cdot T + 0.2804$	0.9837
SS 0.99	$f = 0.2905 \cdot T + 0.2714$	0.9827
SS 0.81	$f = 0.2751 \cdot T + 0.1645$	0.9894

TABLE IV
COMPARISON OF PERFORMANCE

	[9]	[10]	[1]	This Work
Year	2016	2015	2018	2023
Tech. (nm)	180	180	28	40
Supply (V)	1.8	1.8	0.8	0.9
Control bits	6+1	6+1	8	7
PVT Detectors	none	none	none	45 corners
Bands	dual	dual	single	single
Stages	4/8	10/11	255	132
Jitter (ps)	3.48	14.8	∼	**1.98**
max. Power (mW)	1.98	1.37	2.5	**0.235**

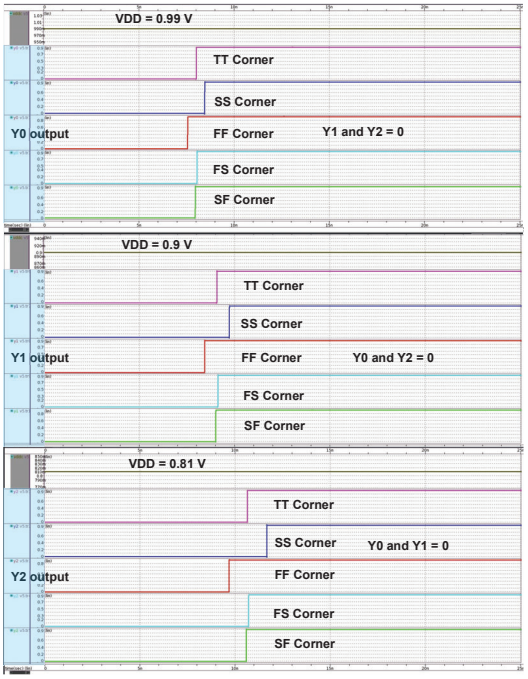

Fig. 7. Post-layout simulations of Voltage detector

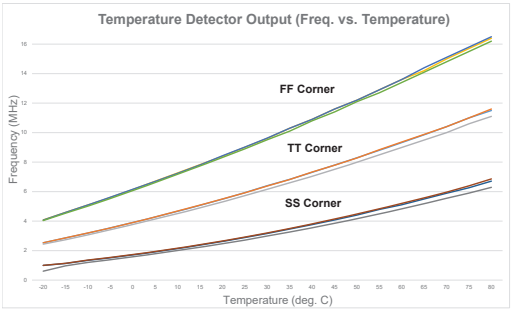

Fig. 8. Post-layout simulation of Temperature detector

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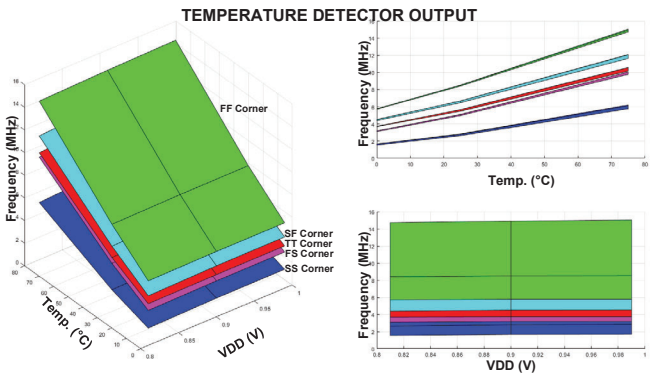

Fig. 9. Post-layout simulation of Temperature detector (45 corners)

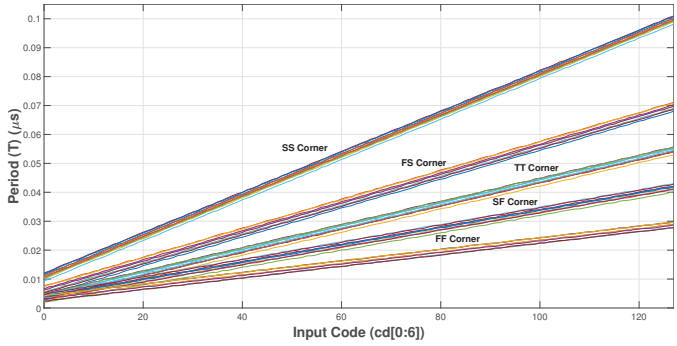

Fig. 10. DCO post-layout simulations

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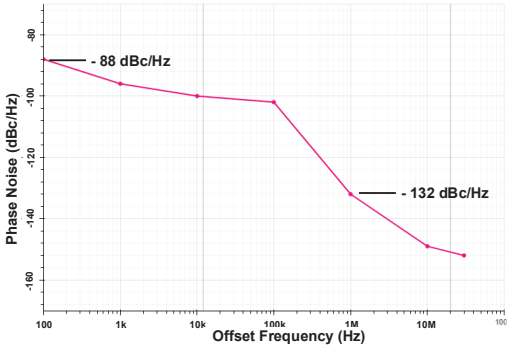

Fig. 11. DCO phase noise by post-layout simulations

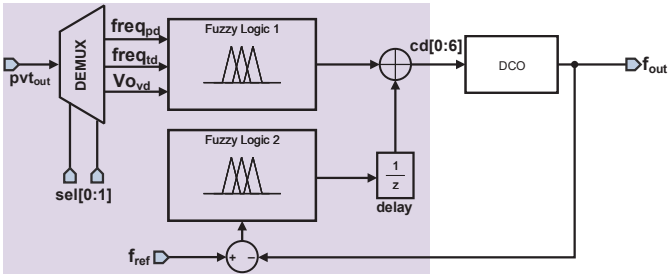

Fig. 12. Block diagram of external auto-calibration which used fuzzy logic control

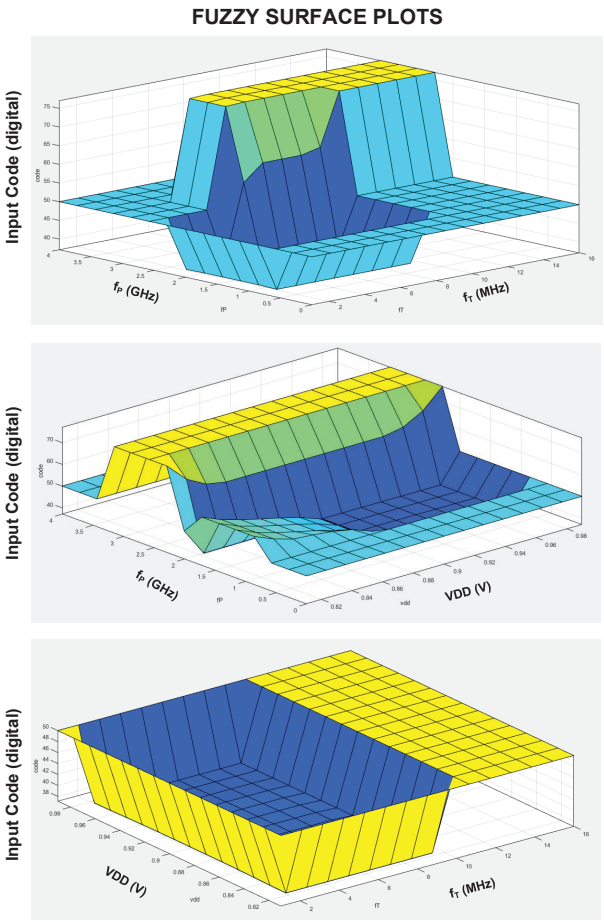

Fig. 13. Fuzzy logic surface plot

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