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SiC MOSFET High Side Gate Driver Design Using HV CMOS Process

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***Abstract*—High side driver is one of major factors determines the performance of SiC MOSFETs. This research proposed an AGD (active gate driver) design that uses a window comparator circuit, feedback-controlled split-path circuit, and tri-state inverting buffer to generate weak and strong driving signals. The proposed AGD has been implemented in TSMC 0.18-μm HV CMOS (T18HVG2) technology, which has a core area of 3200 x 2632 μm^2 and an overall chip area of 4515 x 3260 μm^2. The HV MOS and diode model of Infineon IMW65R048M1H are used as the power MOSFETs in all-PVT corner post-layout simulations. The peak gate current ($I_{g(pk)}$), rise time (t_{rise}), fall time (t_{fall}), and average power consumption (P_{ave}) for the worst corner are 4.15 A, 153 ns, 187 ns, and 32.7 W, respectively, at f_{PWM} = 500 kHz.**

***Index Terms*—AGD, Miller plateau, SiC MOSFET, weak and strong driving signals**

I. Introduction

Silicon based power semiconductors carved its name for most power electronics applications because of its design compatibility, advanced manufacturing process techniques, and quality of material over the years [1]. In line with silicon device advancements, wide band-gap (WBG) semiconductor such as Silicon Carbide (SiC) and Galium Nitride (GaN) offer unipolar power diodes and transistors with low on resistance and switching loss, high blocking voltage, and the ability to withstand high junction temperature because of its material superiority compared to unipolar silicon (Si) devices [2].

Designing a high side gate driver appropriate for SiC MOSFET performance is critical [3]. The SiC MOSFET driver circuit must maintain its usual driving voltage under high dv/dt and di/dt. The high dv/dt may interact with SiC C_{gd}, causing a shoot-through event, false turn-on, and crosstalk noise [4]. A low dv/dt and di/dt may be obtained by reducing the driving frequency, which reduces the power device's switching speed. The conventional architecture of gate drivers gives a trade-off between switching loss of the SiC power devices and current/voltage overshoot [5].

An Active Gate Driver (AGD) is an effective method that resolves the trade-off between current/voltage overshoot and switching loss by dynamically adjusting the driving capability in the process of switching the power SiC MOSFET. A prediction method based on MEA-BP neural network (NN) in driving IGBT module was reported to predict the turn-on and turn-off of variable gate resistance active gate driver [6]. A BP (backpropagation) neural network was employed, and the prediction technique made the overshoot and switching loss smaller without varying the switching time to adjust the weights and biases of the NN. The prediction method and the algorithm are complex, and the driver requires positive and negative voltage supplies which are rarely appreciated. Many other researches use FPGA, or microcontroller in the design of AGD for optimal driving capability [7] [8] [9]. However, all the models don't have real-time output data and each so-called optimal driving voltage is specific only to one specific power device and topology. It needs to be retuned or reprogrammed based on the characteristics of each power device to acquire their optimal driving voltage, which is not efficient. Each driver consists of different chips that makes them bulky. The heavy computational workload requires expensive data processors, FPGAs, etc., which will increase the number of the critical components in the system to cause more downtime.

The proposed AGD method has been implemented in TSMC 0.18-μm HV CMOS (T18HVG2) technology which overcomes the area limitation of the module-based AGD driver. The reference voltages, $V_{ref(th)}$ and $V_{ref(m)}$, in the driver reduce the complexity of the computational or tuning methods that the prior works employ.

II. High side driver design based on Miller plateau detector

Fig. 1 shows the block diagram for the proposed AGD. The 2-level Miller plateau detector compares the gate voltage (V_g) to both $V_{ref(th)}$ and $V_{ref(m)}$. It generates two signals that indicate when the gate voltage enters and leaves the Miller region. The output of the detector circuit is coupled to the Logic circuit, which drives the Strong Inverter (M_{PS}, M_{NS}, both HV MOS) through V_{PS}, and V_{NS}. The Standard and Strong Inverters in the Two-stage tri-state inverting buffer generate strong and weak driving signals depending on the output of Logic circuit. To prevent overshoot, the PWM input signal is fed to the Feedback-controlled split-path circuit, which produces a delay between the signals, V_{PW} and V_{NW}. The split-path circuit drives Standard Inverter (M_{PW}, M_{NW}, both HV MOS).

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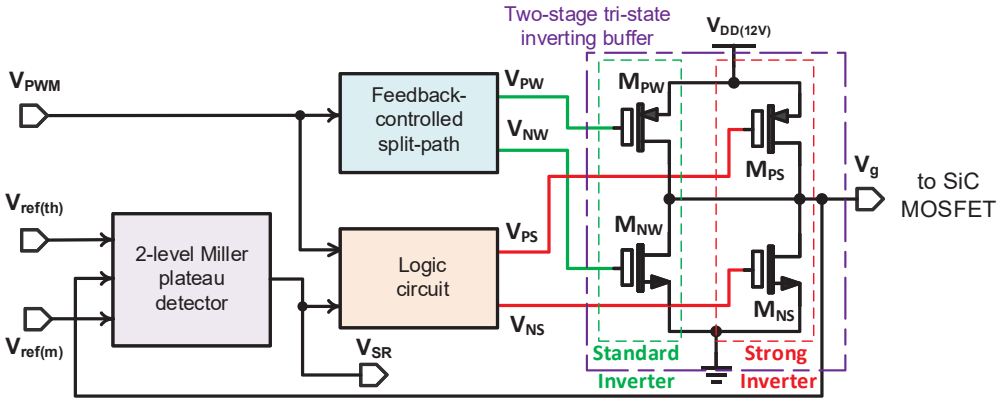

Fig. 1. Proposed SiC MOSFET AGD block diagram

TABLE I
SUMMARY OF AGD OPERATION

Case	V_{PS}	V_{NS}	V_{PW}	V_{NW}	V_g	Driving Signal Strength
1	L	L	L	L	$V_g \leq V_{ref(th)}$	Strong
2	H	L	L	L	$V_{ref(m)} \geq V_g > V_{ref(th)}$	Weak
3	L	L	L	L	$V_g > V_{ref(m)}$	Strong
4	H	H	H	H	$V_g > V_{ref(m)}$	Strong
5	H	L	H	H	$V_{ref(m)} \geq V_g > V_{ref(th)}$	Weak
6	H	H	H	H	$V_g \leq V_{ref(th)}$	Strong

The timing diagram for the proposed AGD is illustrated in Fig. 2. It consists of 6 cases; 1 to 3 for on state and 4 to 6 for off state. The different cases are detailed as follows:

Case 1: All the HV MOS driving signals are logic low. In this state, the output V_g goes up until it reaches $V_{ref(th)}$.

Case 2: In this state, when V_g exceeds $V_{ref(th)}$, it enters the Miller plateau. The driving level of V_{PS} will be pulled high. The strong driving signal of the gate voltage will be relaxed or weakened until V_g=$V_{ref(m)}$.

Case 3: When V_g is greater than $V_{ref(m)}$, the level of V_{PS} will go low. V_g will leave the Miller plateau to rise to full opening and will be revived as a strong driving signal.

Case 4: The level of the PWM signal will change from low to high, and all of the HV MOS driving signals will become high. V_g will leave from fully turned on until it goes down to the Miller plateau.

Case 5: Once it enters the Miller plateau, V_{NS} will shift from low to high. V_g at this point will become a weak driving signal until its value reach $V_{ref(th)}$.

Case 6: When the value of V_g is smaller than $V_{ref(th)}$, it will revert to a strong driving signal. V_{NS} at this point will return to a high-level signal.

Table I summarizes the outcomes of V_g based on the driving signals of HV MOS for the proposed AGD.

A. 2-level Miller plateau detector

To determine the voltage levels where AGD generates strong and weak driving signals, a 2-level Miller plateau detector is used. Fig. 3 shows the detection circuit based on the window detector, which utilizes two comparators in parallel. The circuit realizes a window based on $V_{ref(th)}$ and $V_{ref(m)}$. When V_g is within the window, Two-stage tri-state inverting buffer generates a strong driving signal; outside the window, it generates a weak driving signal. Voltage references $V_{ref(th)}$ and $V_{ref(m)}$ can be reconfigured depending on the actual $V_{ref(th)\_actual}$ and $V_{ref(m)\_actual}$ of a given power MOSFET. The initial calibration and configuration of $V_{ref(th)}$ and $V_{ref(m)}$ can be done by referring to the datasheet of the MOSFET and conducting a double pulse test. A $V_{ref(th)}$ and $V_{ref(m)}$ in Eqn. (1) are used, since it is the most probable region during the double pulse test.

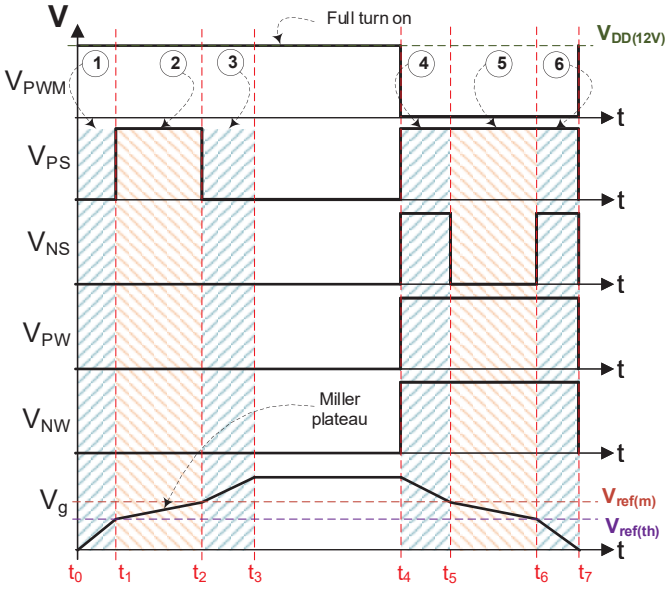

Fig. 2. Proposed AGD timing diagram

$$V_{ref(th)} = 0.3 \cdot V_{DD}; \quad V_{ref(m)} = 0.5 \cdot V_{DD} \qquad (1)$$

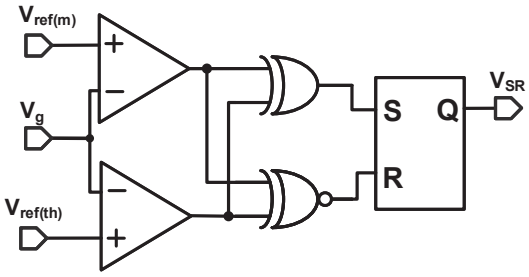

Fig. 3. 2-level Miller plateau detector circuit

TABLE II
STATE OF V_g IN EACH CASE.

V_{PWM}	V_{SR}	V_{PS}	V_{NS}
0	0	H	H
0	1	H	L
1	0	L	L
1	1	H	L

B. Logic circuit

Referring to Fig. 1, Logic circuit generates two independent non-overlapping signals to strong HV MOS, M_{PS} and M_{NS}. Logic circuit's input is coupled to the output of the 2-level Miller plateau detector and the input signal V_{PWM}. In Miller plateau's region, Logic circuit tri-states the Strong Inverter, while only Standard Inverter is on. During this time, Two-stage tri-state inverting buffer will generate a weak driving signal to V_g. Tabulated in Table II is the truth table for the logic circuit.

C. Feedback-controlled split-path circuit

Fig. 4 shows the schematic for the feedback-controlled split-path circuit [10]. Its primary function is to provide a dead zone that eliminates the shoot-through when driving Strong Inverter during transitions. The split-path circuit takes the input signal from the PWM and generates two complementary signals with a dead zone so that M_{PW} and M_{NW} are ensured to be non-overlapping.

D. Two-stage tri-state inverting buffer

Referring to Fig. 1, Two-stage tri-state inverting buffer consists of 2 sets of HV MOS Inverters connected in parallel, namely Standard Inverter and Strong Inverter. They are driven by the split-path circuit and Logic circuit, respectively. During the non-Miller region, the operations of both Standard Inverter and Strong Inverter are the same, which generate a strong driving signal (low output impedance) to drive SiC MOSFET. In the Miller plateau region, however, the PMOS and NMOS of Strong Inverter vary depending on the output of Logic circuit, resulting in a weak driving signal. The width of the PMOS and NMOS of the two inverters is given by Eqn. (2).

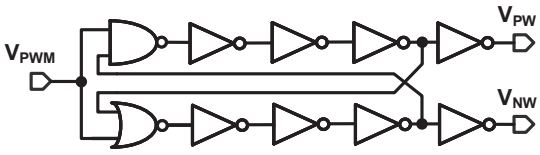

Fig. 4. Feedback-controlled split-path schematic [10]

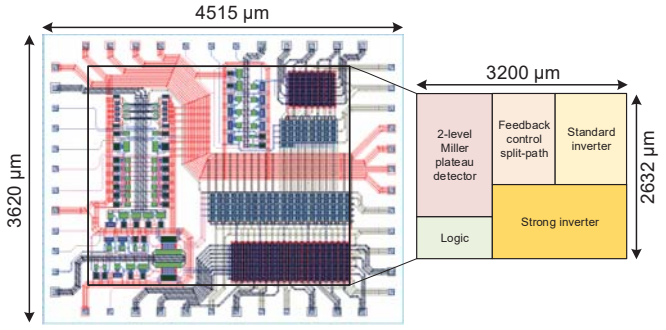

Fig. 5. Layout of the proposed AGD

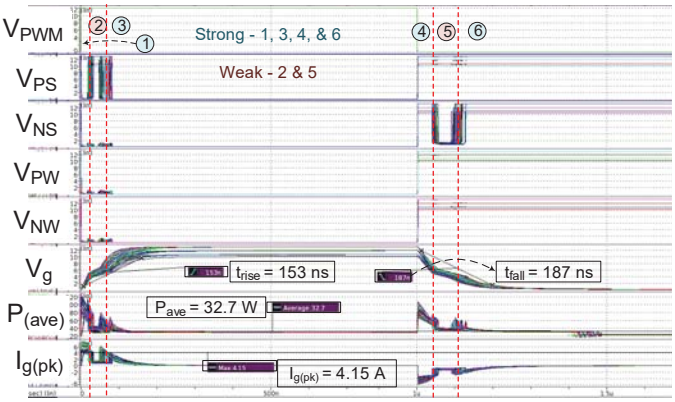

Fig. 6. All-PVT corners post-layout simulation of the proposed design

$$W_{M_{PW}} = \frac{W_{M_{PS}}}{3}; \quad W_{M_{NW}} = \frac{W_{M_{NS}}}{3} \tag{2}$$

III. SIMULATION AND ANALYSIS

The proposed AGD is implemented in TSMC 0.18 μm HV CMOS technology. Fig. 5 shows the design layout with a core area of 3200 x 2632 μm^2 and an overall chip area of 4515 x 3260 μm^2. Fig. 6 illustrates the all-PVT post-layout simulation output waveforms. It is evaluated in five process corners (FF, FS, TT, SF, and SS), three V_{DD} voltages (10.8, 12, and 13.2 V), and 0, 25, and 75^{o}C. The load used during simulation is the equivalent model for Infineon IMW65R048M1H using HV MOS with parasite, diode, where c_{iss} = 13 pF, and R_g = 6 ohms. Furthermore, a c_{rss} = 2 nF compared to the device data sheet is employed to compensate for all the parasitic capacitance at PWM_{freq_max} = 500 kHz. Referring again to Fig. 6, significant parameters such as $I_{g(pk)}$, t_{rise}, t_{fall}, and P_{ave} can be observed with values of 4.15 A, 153 ns, 187 ns, and 32.7 W, respectively. These are from the worst corner that provides the highest value of t_{rise}, t_{fall}, P_{ave}, and the lowest $I_{g(pk)}$.

TABLE III
POWER MOSFET GATE DRIVER COMPARISON

	[11]	[12]	[7]	[13]	This work
Year	2017	2018	2019	2022	2023
Publication	ECCE	JSSC	TPE	ISPSD	
Process (μm)	0.18 AMS HVCMOS	0.18 BCD	CPLD	0.18 BCD + FPGA	0.18 18HVG2
Type	Active	Passive	Active	Active	Active
Verification	Meas.	Meas.	Meas.	Meas.	Post-sim.
V_{DD}	-4 & 15 V	15 V	20 & -5 V	1.8, 3.3 & 20 V	12 V
$f_{operating}$	100 kHz	1 MHz	9.2 MHz	0.1 MHz	0.5 MHz
t_{rise}	140 ns @ 15 V	5.6 ns @ 5 V	—	—	153 ns @ 12 V
t_{fall}	—	—	—	—	187 ns @ 12 V
C_{load}	260 pF	2.7 nF	—	2 nF	2 nF
Chip area	5.00 mm^2	11.27 mm^2	—	6.25 mm^2	16.32 mm^2
$P_{(ave)}$	—	—	—	0.079 W (chip only)	32.7 W

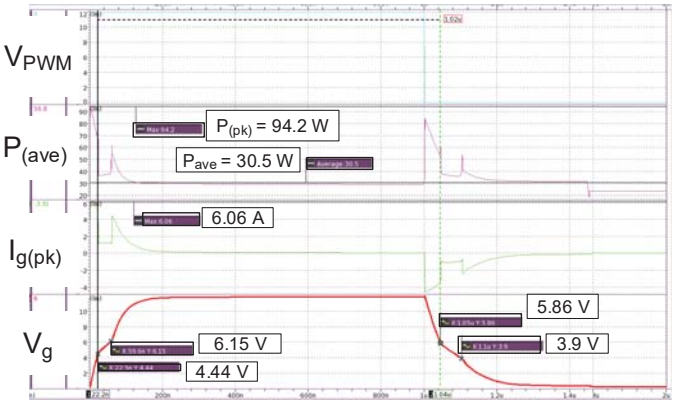

Fig. 7. TT, V_{DD} = 12V, 25°C post-layout simulation

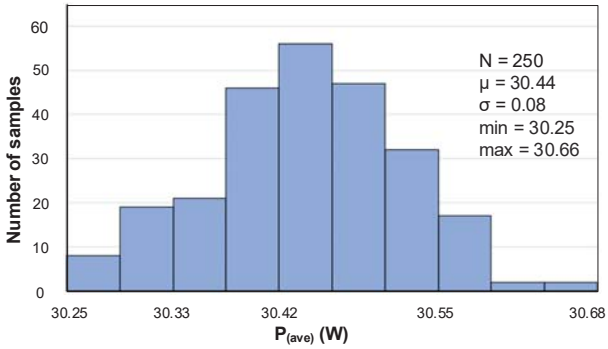

Fig. 8. Monte Carlo simulation for $P_{(ave)}$

Fig. 7 shows a detailed transition of the power consumption (P_{cons}), I_g, and V_g of the proposed AGD at a typical-typical corner, V_{DD} = 12 V, and T = 25 ^{o}C. During turn-on, V_g starts to rise (producing a strong driving signal while the P_{cons} and I_g have peak values of 94.2 W and 6.06 A, respectively, until it reaches V_g = 4.44 V. By then, V_g will enter the Miller plateau generating a weak driving signal. Furthermore, the values of the power and I_g dramatically decrease until V_g hits 6.15 V. Beyond this, the driving signal shifts again to a strong driving signal with a sudden spike of I_g and P_{cons}. When V_g = 12 V, I_g will be approximately equal to 0 while P_{cons} is close to P_{ave}. During turn-off, the process follows the same sequence with different values of $V_{ref(th)}$ and $V_{ref(m)}$ while V_g decreases from 12 V to 0. The direction of the current at this point is also reversed. Notably, $V_{ref(th)}$ and $V_{ref(m)}$ from the simulations are not the same as the voltage references used in the Miller plateau detector because those values changes during operation. Nevertheless, since the error margin $|(V_{ref(th)} - V_{ref(m)})|$ range is large enough to compensate the actual SiC MOSFET V_{th} and V_m variations, the changes will not affect the functionality of the proposed AGD.

Monte Carlo simulations of AGD $P_{(ave)}$ are carried out to evaluate the design's robustness, as shown in Fig 8. The design achieved a minimum of 30.25 W and a maximum of 30.66 W $P_{(ave)}$ for 250 samples. It has an average gain (μ) of 30.44 with a deviation (σ) of 0.08, demonstrating the reliability of the design.

The literature comparison for power MOSFET driver designs is tabulated in Table III. The proposed AGD is the only design implemented on silicon using HV CMOS technology that doesn't rely on programming and thorough tuning. In other words, our AGD driver design is the most cost-effective solution without the loss of robustness by far.

IV. CONCLUSION

This research exhibit an active gate driver design for SiC power devices implemented in 0.18-μm CMOS (T18HVG2) technology. The driver is a closed-loop system that uses a 2-stage Tri-state inverting buffer that generates two distinct driving signals based on the window detection circuit's reference voltages. The performance of the proposed design is confirmed through all-PVT post-layout simulations with worse corner values of $I_{g(pk)}$ = 4.15 A, t_{rise} = 153 ns, t_{fall} = 187 ns, and P_{ave} = 32.7 W at test frequency of 500 kHz.

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