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A 99.6 % Duty Cycle High-Resolution DPWM Using Reconfiguring Decoder

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***Abstract*—Recent DPWM (digital PWM) researches utilize long DFF arrays and multiple clock inputs resulting in serious clock skew at high-accuracy and high-resolution applications. This paper proposed a DPWM using Reconfiguring decoder that only requires a small number of DFF for high-resolution applications. The DPWM design reduces the redundant DFF array clock activity to prevent long clock skew. The single clock input eliminates the need for an additional synchronization signal in the DPWM. In addition, it has a Non-overlapping circuit to prevent shoot-through. The proposed DPWM design is implemented using UMC 180-nm CMOS process. It has an overall chip area of 1469.08 x 1469.08 μm^2 and a core area of 658.93 x 493.79 μm^2. The functionality of the design was validated through all-PVT corner post-layout simulation to demonstrate 99.6 % maximum duty cycle, 96.69 % peak efficiency at C_{load} = 10 μF, L_{load} = 8 μH, and operating frequency of 200 MHz.**

***Index Terms*—DPWM, Reconfiguring detector, single clock, high resolution, high duty cycle**

I. Introduction

Integrated dc-dc converters, as one crucial component in power management, must be highly efficient, easily adjustable, and controllable [1]. Compared to analog systems, digital control offers significant advantages for power dc-dc control [2]. Digital PWM (DPWM), as one type of digital controllers, can work at a low voltage supply with a low quiescent current, which makes it ideal for low-power applications [3]. However, DPWM is inaccurate and uses a wide bit-width and high-speed shift register to increase the resolution, which increases clock power dissipation [4].

An FPGA-based DPWM control circuit was reported to improve the resolution [5]. It implements DCM (digital clock manager) and LUT (look-up-table) approach in two FPGAs to realize the DPWM. Though the control circuit achieves a high resolution of 625 and 500 ps, the FPGA-based DPWM is costly and uses a large area.

A low-power, low-voltage digital buck converter using a DPWM controller for wireless sensor network systems was reported [6]. The automatic selection of DCM or CCM by the DPWM controller increases the buck converter's power efficiency. However, to increase its resolution, the long chain of DFFs in the DPWM is also increased exponentially. Furthermore, it requires three input clock signals, which makes operating at different frequencies very difficult.

A paper that also used a long chain of DFF with a clock gating signal is proposed for a low-power application PWM buck converter [4]. It uses two clock input signals, a fast shift register, and a slow bidirectional shift register in adjusting the DPWM duty ratio. Despite having two clock inputs only, the long DFF chain required for high resolution may cause significant clock skew. Its clock gating architecture adds more propagation delay, which limits the performance of DPWM at higher clock frequencies.

In this study, a DPWM design utilizes a single clock input and Reconfiguring decoder, which is not based on long-chain DFF arrays. The Reconfiguring decoder only requires a small number of DFFs, minimizing the effect of clock skew. The 8-bit resolution is used in the DPWM design to show the functionality scalable to a higher resolution. The dual-clock edge clocking technique reduces glitches during shift register operation. It has a Non-overlapping circuit to prevent shoot-through with a 99.6 % and 96.69 % maximum duty cycle and peak efficiency, respectively.

II. Reconfiguring decoder-based DPWM

Fig. 1 shows the block diagram of the proposed DPWM topology. It consists of 3 main components; Input detection and synchronization, PWM controller, and Output buffer. Input detection and synchronization will determine the % duty cycle of the proposed DPWM. The PWM controller generates SOE (start of sequence) and EOS (end of sequence) signals that set the start and end points of the V_{OPWM}, respectively. The output buffer prevents shoot-through during transitions and achieve impedance matching at large loads. Fig. 2 shows the timing diagram for the proposed Reconfiguring decoder-based DPWM. The length of the V_{OPWM} pulse depends on the input code $D_{O[0:7]}$. Sequence generator counts the clk cycle based on the N resolution, which defines the V_{OPWM} period (T_{DPWM}). When the Sequence generator completes a 2^N clk cycle ($S_{G[0:7]}$ = 00000000), Input sync will produce V_{sync} = 1. V_{sync} and $S_{G[0:7]}$ are updated at the negative and positive edges, respectively, which will reduce glitches during the transitions. SOE signal is generated by the Zero input detector when the output of the DFF input array is not 00000000. The start point of the SOE signal is the reference

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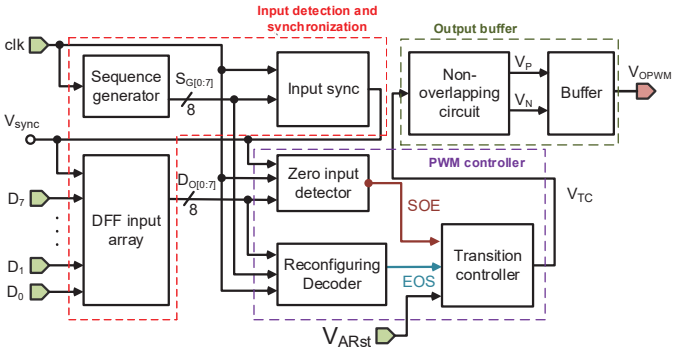

Fig. 1. Proposed DPWM block diagram

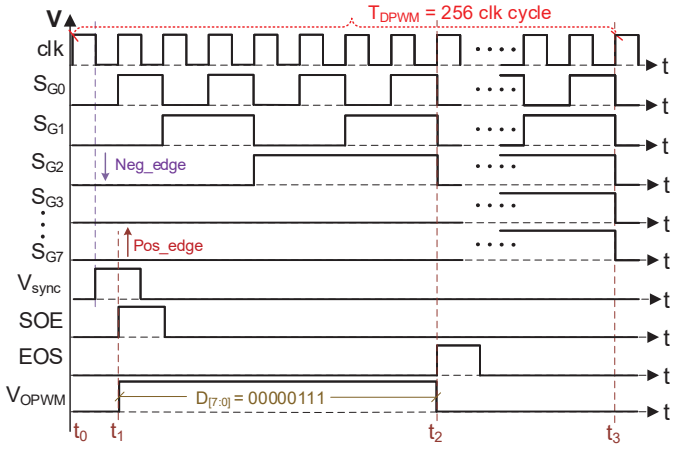

Fig. 2. Timing diagram of the proposed DPWM

for the start point of the V_{OPWM}. The EOS signal marks the end point of the V_{OPWM} generated by Reconfiguring decoder, when the $S_{G[0:7]} = D_{O[0:7]}$.

A. Input detection and synchronization

Input detection and synchronization block in Fig. 1 determines the % duty cycle of the proposed DPWM. It consists of a Sequence generator, Input sync, and DFF input array. Fig. 3 shows the schematic of Sequence generator that converts clk pulses into N-bit binary sequences (S_{G0} to S_{G7}), which represent the input pulse position. The dual-edge-triggering technique utilizes the positive and negative edges in updating the present and next state of the DPWM. This provides enough margin for "read" and "write" for DFF strings, improving the proposed DPWM reliability at higher resolutions.

The Input sync shown in Fig. 4 updates the duty cycle selection inputs and synchronizes Sequence generator and DFF input array. The V_{sync} signal is generated every 2^N clk cycle and updated at the negative edge of the clk, improving the stability. Lastly, the DFF input array determines the resolution of the DPWM. The "N" resolution of the DPWM is equal to the number of DFFs in the DFF input array.

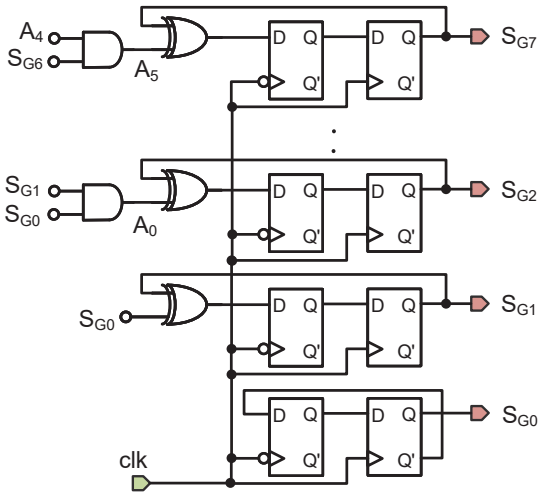

Fig. 3. Sequence generator schematic

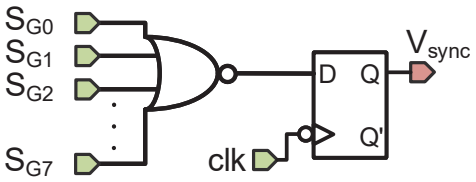

Fig. 4. Input sync schematic

B. PWM controller

The PWM controller consists of a Zero input detector, Reconfiguring decoder, and Transition controller that determines the start (SEO) and end (EOS) points of the proposed DPWM output voltage. When $D_0 \sim D_7$ of the DFF input array is 00000000, Zero input detector (shown in Fig. 5) prevents the SOE signal from being generated, since no PWM signal must be generated under this condition. In any other input of the DFF input array, Zero input detector will generate the SOE. The SOE is delayed by half clk duty cycle, which provides enough margin for Zero input detector to accurately detect if inputs $D_0 \sim D_7$ is 00000000 or not, which are updated at the positive edge of clk.

Since the prior DPWM topologies used a long chain of DFF (equal to 2^N) [4] [6], the Reconfiguring decoder lessens the number of DFFs in the proposed DPWM. Fig. 6 shows the Reconfiguring decoder, which generates the EOS to determine the pulse width of the DPWM output. From V_{sync}, the Input detection produced another half clk cycle to SOE (one clk

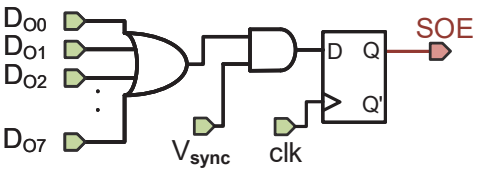

Fig. 5. Zero input detector circuit

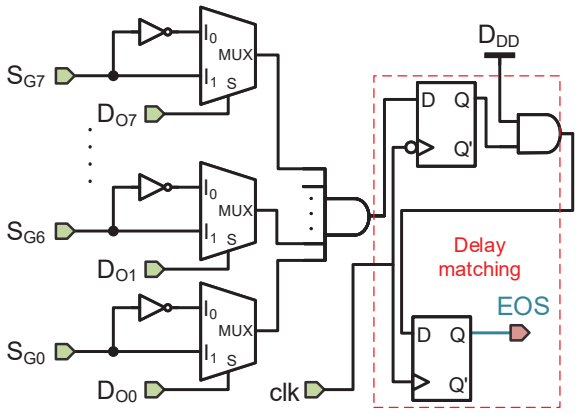

Fig. 6. Reconfiguring decoder schematic

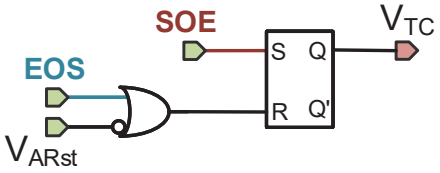

Fig. 7. Transition controller circuit

cycle delay from t_0). Thus, EOS is also delayed by one clk cycle from t_0 to ensure that the total period of the output signal (T_{PWM}) is addressed the same as Eqn. (1).

$$T_{PMW} = 2^N \cdot T_{clk} \tag{1}$$

where T_{clk} is the clock period. The maximum duty cycle (dc_{MAX}) can be determined using Eqn. (2).

$$dc_{MAX} = \frac{2^N - 1}{2^N} \cdot 100\% \tag{2}$$

The schematic of Transition controller, which is driven by SOE and EOS signals, is shown in Fig. 7. The output pulse width of the DPWM is based on its Transition controller output V_{TC}. During the initial operation of the DPWM, V_{ARst} resets the SR latch to its default state and will be disabled after.

C. Output buffer

The Output buffer uses a Non-overlapping circuit based on a feedback-controlled split-path topology [7]. Illustrated in Fig. 8 is the Non-overlapping circuit that provides a dead time that eliminates shoot-through when driving the buffer during transitions.

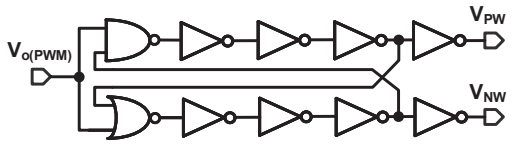

Fig. 8. Feedback-controlled split-path

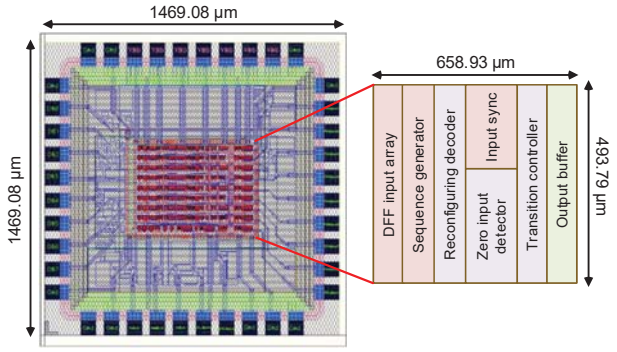

Fig. 9. Layout of the proposed DPWM

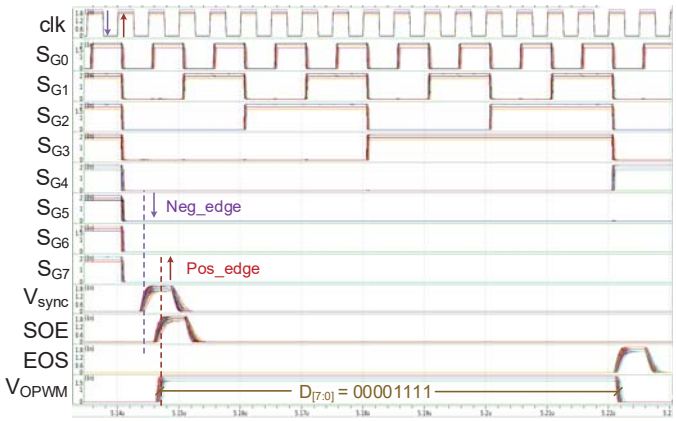

Fig. 10. All-PVT corners post-layout simulations of $D_{[7:0]}$ = 00001111 of the proposed DPWM

III. Simulation and Analysis

The layout of the proposed DPWM circuit is illustrated in Fig. 9. It is implemented using 180-nm CMOS technology with an overall chip area of 1469.08 x 1469.08 μm^2 and 658.93 x 493.79 μm^2 core area.

The all-PVT corner post-layout simulations of the Reconfiguring decoder-based DPWM design is illustrated in Fig. 10. The DPWM design is evaluated in five process corners (FF, FS, TT, FS, and SF), three voltage supply (1.98, 1.8, and 1.62 V), and temperatures of 0, 25, and 75°C. C_{load} = 10 μF, L_{load} = 8 μH are used during the simulations at a clk frequency of 200 MHz, and $D_{[7:0]}$ = 00001111. Referring to Fig. 10, V_{sync} is generated in the clk's negative edge (represented by a downward arrow) after a half clock cycle. After another half clock cycle, an SOE signal is generated at the positive edge of the clk input (represented by an upward arrow), which marks the start of the V_{OPWM} to go high. For 15 clock cycles (the binary equivalent of the D inputs = 1111), V_{OPWM} will remain at a high state. After this, the EOS is generated at the positive edge of the clk input, pulling V_{OPWM} from high to low until $T_{PWM} = 2^N$ clk clycles.

Fig. 11 (a) shows the all-PVT corner post-layout simulation of the DPWM using Johnson counter. This provides a different % duty cycle of the V_{OPWM} to check the correctness of the design. It attains a maximum duty cycle of 99.6 % and

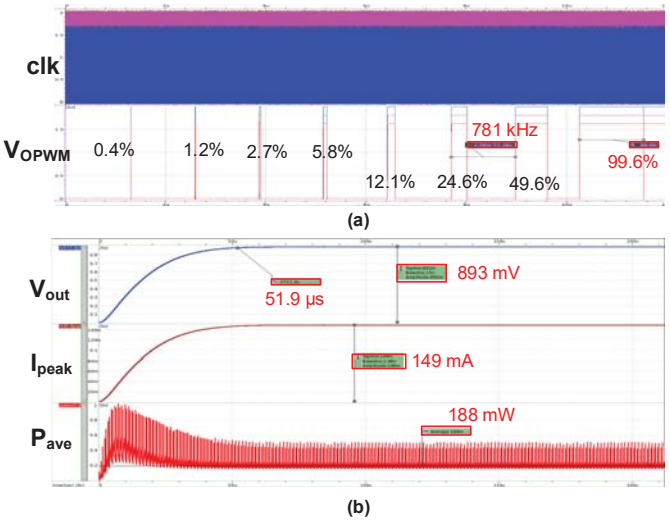

Fig. 11. Proposed DPWM: (a) all-PVT corners post-layout simulations driven by Johnson counter, (b) P_{ave} consumption

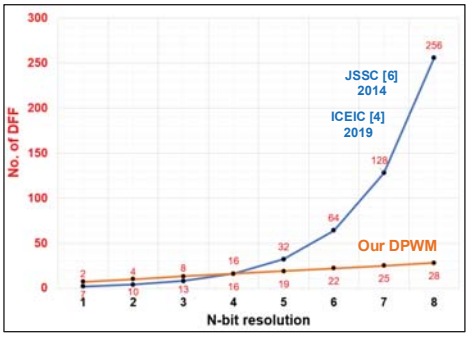

Fig. 12. No. of DFFs comparison between [4], [6] and proposed DPWM

f_{DPWM} = 781.2 kHz. At a 50 % duty cycle, our design achieves I_{peak} = 142 mA, V_{out} = 0.85 V, and P_{ave} = 188 mW, as shown in Fig. 11 (b).

The number of DFFs used between our DPWM design and [4] [6] is illustrated in Fig. 12. Our DPWM design requires (3 × N) + 4 numbers of DFFs to have an N-bit resolution. The number of DFFs of our DPWM is significantly lesser compared to the prior DPWMs as resolution increases.

The performance comparison with prior DPWM architectures is tabulated in Table I. The efficiency of our design is not affected by the legacy process that we used compared to [4] and [6], since it is a function of P_{out} and P_{in} (η_{eff} = P_{out}/P_{in}). In addition, the lower values of passive components are required to filter output voltage ripple at higher switching frequencies. The proposed DPWM Reconfiguring decoder significantly reduces the number of DFF as the resolution increases, which reduces the effect of clock skew. The single clock in our DPWM design reduces design complexity and makes it scalable across a wide frequency range. Notably, compared to other DPWMs topologies in Table I, our DPWM design has the highest maximum duty cycle of 99.6 %, which improves the load and line regulations. Compared to other

TABLE I
PERFORMANCE COMPARISON OF SEVERAL DPWM

	[6]	[4]	this work
Year	2014	2019	2023
Publication	JSSC	ICEIC	
Technology	40-nm	65-nm	180-nm
Verification	Meas.	Meas.	Post-layout sim.
V_{DD} (V)	0.6 - 1.1	0.6	1.8
V_{out} (V)	0.3 - 0.55	0.1 - 0.5	0 - 1.79
Clk frequency (MHz)	64	64	200
Resolution (bits)	6	6	8
Load	1 μF & 220 μH	4.7 μH	10 μF & 8 μH
Duty cycle$_{(Max)}$ (ideal)	98.44 %	98.44 %	99.6 %
Core area (mm^2)	31.4	31.73	0.325
P_{out} (mW)	N/A	N/A	188
Peak efficiency	94 %	94 %	96.69 %

DPWM designs, our design has the highest peak efficiency of 96.69 % and the highest resolution of 8 bits, making it more practical.

IV. Conclusion

This paper presents a DPWM design using Reconfiguring decoder implemented in UMC 180-nm CMOS process. The Reconfiguring decoder significantly reduces the number of DFFs compared to prior DPWMs to reduce clock skew. The use of a single clock makes the design easier. Additional Non-overlapping circuit prevents shoot-through during operations. The functionality of the DPWM design is validated through all-PVT corner post-layout simulation with a maximum duty cycle of 99.6 % and peak efficiency of 96.69 % at C_{load} = 10 μF, L_{load} = 8 μH, and 200 MHz clock frequency.

Acknowledgment

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