Three-level DC-DC Buck Converter Architecture Using Digital Pulse Width Modulation

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***Abstract*—This study demonstrates a high efficiency 3-level DC-DC buck converter using DPWM (digital pulse width modulation). It is mainly featured with the replacement of traditional flying capacitor with a capacitive voltage divider, which will constantly maintain the half of the supply input voltage. Consequently, one of the power MOSFETs in the output stage will be removed to reduce conversion loss. The duty cycle is found to be as high as 93.75% and the peak efficiency is 98% at 6.25 MHz switching clock rate by all-PVT-corner simulation.**

Keywords—DC-DC converter, 3-level topology, DPWM, duty cycle, high efficiency

I. Introduction

The fast evolution of semiconductor technologies results in that transistors as well as devices are downsized constantly and rapidly. The operation voltage of these devices are also dropped from 5 V to 3.3, 1.8 , or even lower voltage levels. Nevertheless, the operation voltage of prior or existing systems might be still 5 V, 12 V or higher, particularly those in EV or PEV electronics. Therefore, DC-DC converters are demaned in many applications to support lower voltage operations for devices fabricated by advanced processes. There are two popular types of converters, namely "Low Drop-Out Linear Regulator (LDO)" [1] and the "Switching Mode Power Supply (SMPS)" [2], where the latter is recognized to possess wider range for many applications. Traditionally, two major SMPS methods have been reported to implement the controller mechanism, i.e., ``Pulse-Width Modulator (PWM)" and ``Pulse-Frequency Modulator (PFM)". Each has its own features and problems [3] [4] [5] [11].

One of the prior approaches to elevate the efficiency of the regulated voltage output is the increase of switching speed regardless of the load variation. These converters are mainly focused on high-frequency power conversion circuits that use high-frequency switching and inductors, transformers, and capacitors to smooth out switching noise into regulated DC voltages. However, this approach is hard to be adopted in battery-powered portable devices, since prior synchronous buck-based battery chargers cannot take full advantage of high input power because of their maximum efficiency limitations. The challenge for portable electronics designers is how to fit a high-efficiency battery charging solution in a small footprint that fully utilizes high input power to achieve fast and cool charging.

In this work, a three-level converter topology that includes added capacitive storage elements and power switches can increase the equivalent switching frequency, f_{sw}, and generate a lower voltage across the inductor, which enables the use of a smaller inductor. This improves total system efficiency, with lower power losses and cooler operating temperatures in a smaller footprint when compared to traditional synchronous buck converters. Besides theoretical analysis, thorough all-PVT-corner (process, voltage, temperature variation) simulations are conducted to justify the performance of the proposed architecture.

II. Proposed 3-level DC-DC Architecture

A. Prior 3-level DC-DC topology

Referring to Fig. 1, a total of 4 power MOSTFETs are needed in the output stage to carry out the required duck conversion. Not only these MOSFETS occupy a meaningful area on a silicon die or a PCB board, they also consume a great portion of power no matter which mode they are. A typical mode for D (duty cycle) > 50% is illustrated in Fig. 2. Notably, the scenario of D < 50% will be similar to that of D > 50%, as shown in Fig. 3. However, the details thereof will not be addressed here due to page limitation of the conference.

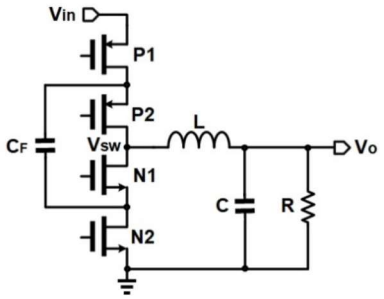

Fig. 1 : Conventional 3-level buck converter

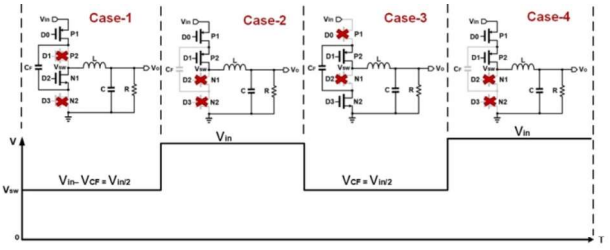

Fig. 2 : Operation of conventional 3-level cuck converter (D>50%)

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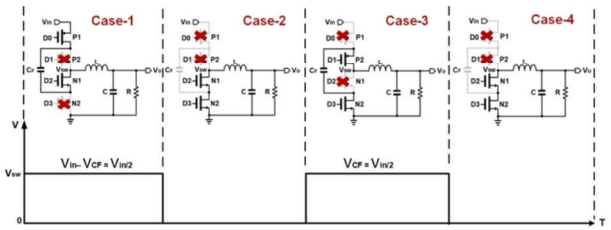

Fig. 3 : Operation of conventional 3-level cuck converter (D<50%)

Apparently, 2 of the 4 power MOSFETs shall be activated in any time. Besides, the generation of the 4 gate drive signals, D1, D2, D3, and D4, is considered quite complicated.

B. Proposed 3-level DC-DC converter

The proposed 3-level DC-DC converter is disclosed in Fig. 4, where the conventional flying capacitor is replaced by the capacitive voltage divider which will constantly maintain the half of the supply input voltage. Notably, the prior flying capacitor is balanced by power MOSFETs in the conventional designs, which may not be balanced accurately at Vin/2. Not only the proposed design resolves this issue, it also use 3 MOSFETs only to achieve better power-saving performance.

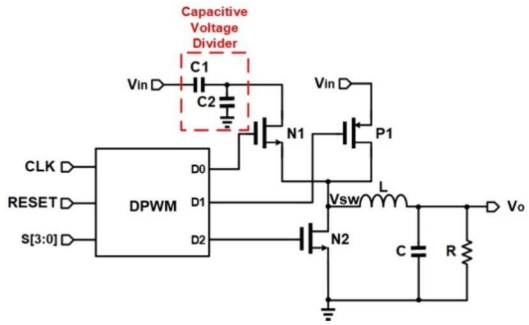

Fig. 4 : Proposed 3-level DC-DC buck converter

C. Estimation of off-chip passive discretes

Referring to Fig. 3, the passive (off-chip) discretes are estimated as follows.

$$L = \frac{(V_{in}-V_o)\times D}{I_{ripple}\times I_{o,max}\times f_s} \quad (1)$$

$$C = \frac{I_{ripple}}{8\times V_{o,ripple}\times f_s} \quad (2)$$

where Vin and Vo are input and output voltage, respectively, D is the dusty cycle, Iripple is the ripple current, Io,max stands for the largest load current, fs is the switching frequency, and Vo,ripple is the ripple of the output voltage. What is even more important is that the output voltage is predictable as follows.

$$V_0 = \frac{C1}{C2 \times C1} \times V_{in} \quad (3)$$

D. Operation modes

The operation mode of the proposed three-level buck converter when the duty cycle is greater than 50% is shown as in Fig. 5. There are a total of 4 cases described as follows.

- Case 1 : P1 and N2 power MOSFETs are off. N1 is turned on to pass down the output voltage of capacitive voltage divider which is Vin/2. Thus, the switching volage is Vin/2 as shown in the Fig. 4.
- Case 2 : N1 and N2 both are turned off, while P1 is turned on. Hence, Vsw is equal to Vin.
- Case 3 and 4 : They are repeated as Case 1 and 2, respectively.

The operation mode of the proposed three-level buck converter when the duty cycle is less than 50% is similar to that of D > 50%, as shown in Fig. 6. Compared the cases in Fig. 5 with those in Fig. 2, the proposed design obviously attains the following advantages: easy to generate gate drive control signals for MOSFETs, accurate Vin/2, less Vth drop loss caused by stacked MOSFETS. The proposed design, then, is expected to have better performance.

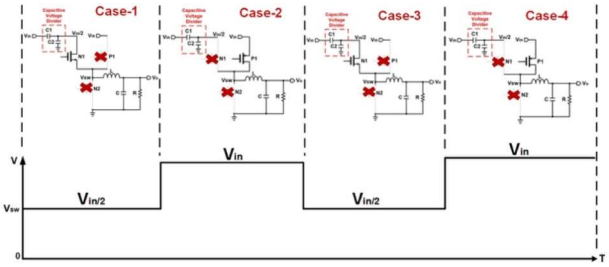

Fig. 5 : Operation of the proposed 3-level cuck converter (D>50%)

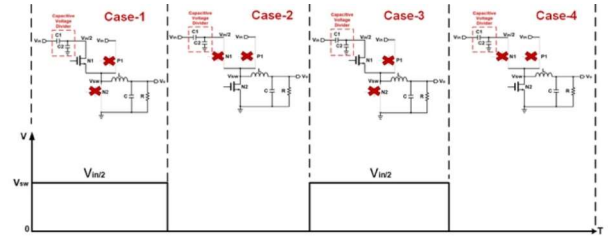

Fig. 6 : Operation of the proposed 3-level cuck converter (D<50%)

E. Digital Pulse Width Modulation (DPWM)

Referring to Fig. 4, the operation mode control depends on DPWM, which is in charge of the generation of the gate drive control signals, D0, D1, D2. It consists of 3 major blocks, i.e., 4-bit counter, Sequence Decoder, and MUX besides SR latch, as shown in Fig. 7.

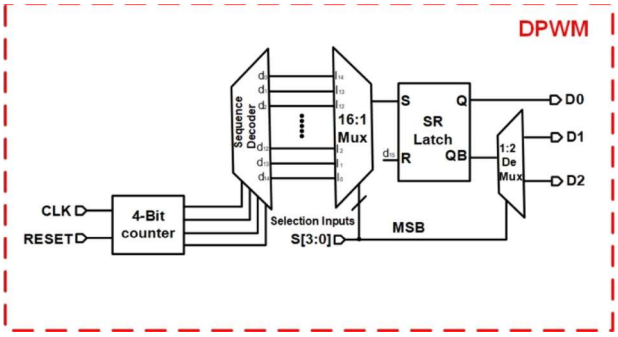

Fig. 7 : Block diagram of Digital Pulse Width Modulation

- **4-bit synchronous counter**: It counts the number of CLK pulses and produces the count in a binary format.

Hence, this binary count can also be seen as the CLK position, which can be decoded with the help of sequence decoder. This forms the basic timing synchronization block of the architecture. The resolution of the counter also determines the resolution of this DPWM.

- **Sequence Decoder**: The sequence decoder converts the binary equivalent of clock position into a unique time domain equivalent signal. Each decoded pulse is shifted by 1 CLK period. Hence, for 4-bit resolution counter, 16 total positions are possible to be detected from D0 to D15.

  Two types of PWM control are possible to be used, namely trailing edge control or leading edge control. This design chooses the latter one. Therefore, the end of PWM sequence (EOS) is fixed as D15. These leaves 15 possible positions (D0 to D14) for Start of the PWM sequence (SOE). The SOE positions can be selected with the help of MUX.

  The proposed design uses a 16x1 MUX with 16 input channels (I0 - I15). The sequence of connections between the sequence decoder should be reversed that means, for example, D14 is connected to I1 and D0 is connected to I14. But I0 will be left as D15 so that it cannot be used as SOE position. Hence, it is simply grounded, as I0 corresponds to 0% duty cycle.

- **SR Latch**: The SR Latch generates the PWM signal based on the SOE pulse (D0 - D14) and EOS signal (D15). The resolution of output PWM signal is CLK time period. The PWM frequency is given by the equation fclk/2^n. Maximum duty cycle is given by the equation (2^n-1/2^n) %.

III. Simulation And Performance Comparison

The proposed 3-level DC-DC buck converter was realized using typical 0.18 um HV CMOS process offered by TSMC. All-PVT-corner simulations, namely 5 process corners (TT, FF, SS, SF, FS), 3 voltage corners (VDD, 0.9xVDD, 1.1xVDD), 3 temperature corners (0, 25, 75)ºC, are conducted to ensure the robustness. Fig. 8 demonstrates the transient waveform of DPWM to prove that the gate drive control signals indeed are pulse modulated as expected.

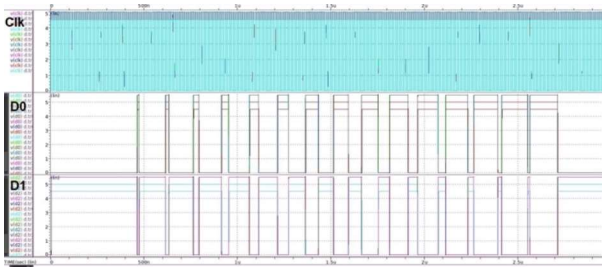

Fig. 8 : Simulation waveforms of Digital Pulse Width Modulation (partial)

A. Operation verification with various dusty cycles

Referring to Fig. 9, 10, and 11, the Vo timing responses for D = 25%, 50%, and 75 % are disclosed, respectively, at CLK = 6.25 MHz. The settling time is 289 us at max. load current = 6.25 mA, 284 us at max. load current = 37 mA, and 242 us at max. current = 43.75 mA.

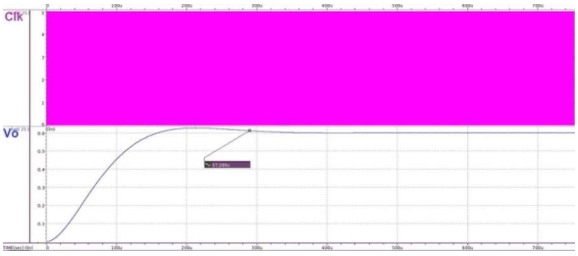

Fig. 9 : Vo waveform of the proposed DC-DC given D = 25%

Fig. 10 : Vo waveform of the proposed DC-DC given D = 50%

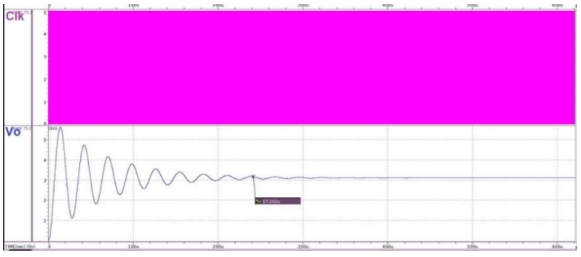

Fig. 11 : Vo waveform of the proposed DC-DC given D = 75%

All the simulation results are summarized in TABLE I. where Io is the load current and t_{settle} means the settling time. Apparently, the proposed 3-level DC-DC buck converter featured with DPWM and the capacitive voltage divider is proved to be fully functional given various dusty cycle conditions. Notably, as tabulated in Table I, the efficiency as well the output current both increases as duty cycle goes up, while the settling time decreases in this manner. This phenomena indeed proves the functionality of DPWM in our design.

TABLE I. SIMULATIONS OF VARIOUS DUTY CYCLES

	Duty Cycle	Efficiency	Io (mA)	t_{settle} (us)
D>50% (5V-2.5V)	**93.5**	**98.0**	**48.0**	**258**
	75.0	97.6	43.8	242
	62.5	97.2	40.6	271
	50.0	96.7	37.0	284
D<50% (2.5V-0V)	37.5	40.8	9.0	288
	25.0	36.67	6.25	289
	18.8	34.1	4.68	309
	6.25	32.2	1.56	312

B. *Peformance comparison*

Compared with recent mutil-level DC-DC converters as shown in TABLE II, the proposed design attains the second best of duty cycle and switching frequency, and more importantly the best 98% in terms of efficiency. Notably, the technology used in the realization of this study is not state of the art. On the contrary, what we used in this report is a legacy process, i.e., 180 nm CMOS. Apparently, the proposed 3-level DC-DC buck converter featured with DPWM and the capacitive voltage divider is proved to be fully functional given various dusty cycle conditions.

TABLE II. PERFORMANCE COMPARISON

	[6]	[7]	[8]	[12]	[9]	[11]	Ours
Year	2016	2018	2019	2019	2020	2022	2023
Pub.	JSSC	ISCAS	CICC	APC	APEC	TCAS1	
Tech. (nm)	500	130	65	180	65	65	180
Vin (V)	12	1.4 ~ 3.6	2.8 ~ 4.2	0.1 ~ 1.7	12	2.4	5
fsw	2.0	NA	NA	30	0.4	25	6.25
Duty cycle	83.0	NA	NA	94.8	NA	NA	93.75
#level	3	2	2	2	2	3	3
Peak Eff. (%)	90.0	90.2	86.6	94.5	86.7	92.8	**98.0**

C. *Techonoloy Review*

To graphically illustrate the superiority of the proposed DC-DC converter featured with DPWM and the capacitive voltage divider, the efficiency performance of all of the related multi-level DC-DC buck converters is drawn in Fig. 12. Certainly, it is well known that a single KPI (key performance index) is not enough to judge of the overall performance of a design. However, the efficiency is considered as the top KPI of converters. Thus, the proposed buck convert attains the edge in this regard.

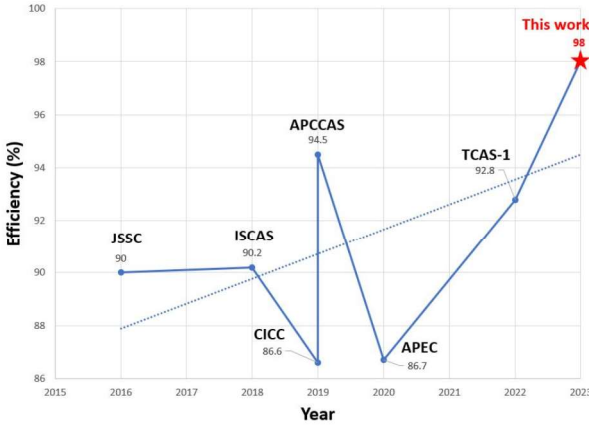

Fig. 12 : Technology roadmap of multi-level DC-DC buck converters

IV. CONCLUSION

Referring to TABLE II and Fig. 12, the proposed DC-DC converter featured with DPWM and the three-level switching technique is proved to attain the best efficiency and the second best of switching speed. Also, the capacitive voltage divider topology is much easier to implement compared to conventional architecture. More importantly, the duty cycle of the proposed design is digitally selectable to meet various demands, which also shows the flexibility as well. The peak efficiency is 98% achieved at load current of 48 mA.

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