A Novel Constant-pulse Scheme for Synchronous Half-bridge Converter Module

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***Abstract*—Half-bridge topology converters are favored over full-bridge topologies due to their lower cost, circuit simplicity, and benefits for high-power applications. This study demonstrates a new pulse width modulation (PWM) control strategy for a half-bridge converter implemented with two TL494 IC. It is featured a maximum turn-on time for high-side MOSFETs in a half-bridge converter to reduce overall power loss. The proposed PWM generator is proven to work at a switching frequency of 35 kHz with a load of 0.4 mH using Infineon SiC MOSFETs at 10%, 25%, and 40% duty cycles. The high-side power loss is reduced by up to 45% by the proposed PWM scheme.**

***Index Terms*—half-bridge converter, low power loss, synchronous switching, high-side MOSFET, PWM.**

I. Introduction

DC motors are employed in a wide range of industrial applications, from small equipment to large industrial machinery [1]. Generally, the efficiency of DC motors can be affected by the speed controller. Power MOSFETs are used as switches to control the voltage across the motor armature coils which in turn control the speed. Half-bridge and full-bridge are basic topologies that can be used to achieve the proper speed control of DC motors. However, the half-bridge is preferred because of its design simplicity and low cost. A half-bridge converter's typical power stage was proved to attain a reduced overall dimension, which is advantageous for high-power applications [2].

Power conversion circuits required low-on state voltage drop and fast switching to decrease the power loss [3]. The fast switching creates voltage spikes that may destroy the power transistor if the voltage exceeds its rated breakdown voltage. The use of free wheeling diode (FWD) prevents the destruction of power electronics to decrease the switching power loss [4]. The FWD conducts during the kick-back phase and clips the voltage below the V_{TH} of the power transistor. This method is considerably simple. However, it is only efficient during lower loads operations, since the constant voltage drop across the diode during forward-bias increases the power loss at higher loads. A synchronous switching method was used to address the issue of the FWD [5]. A transistor replaces the diode, resulting in a reduced power loss during conduction. However, the PWM must be modified to avoid high-side transistor (Q_{high}) and the associated driver transistor to be turned on simultaneously, which can lead to shoot-through. This shoot-through causes a significant current flow from V_{supply} to the ground, causing a large short circuit and destroying the transistor on the path. The low-to-high transitions in the gating signal of the Q_{high} and driver transistor are delayed by a dead-time circuit to prevent this shoot-through [6]. The implementation of the dead-time circuit will provide a small interval between signals where both Q_{high} and the driver transistor are off. However, when an application requires a lower pulse width, the power loss increases at the Q_{high}.

The use of DSP and FPGA in the implementation of PWM generates more accurate pulse control [7] [8]. However, they are not practical compared to analog chips because it occupies space and high cost. Also, most FPGAs operate at a 2.5 V to 5V power supply [9] [10]. Since power MOSFET required a high driving voltage, FPGA based pulse generator cannot be directly interfaced with it.

This paper proposed a new PWM control scheme for the half-bridge power MOSFET control using TL494. The input pulse for the high-side transistors is always set in maximum turn-on time that will decrease the power loss during low duty-cycle applications. The two TL494 will reduce the overall operating temperature of the power transistor, which will increase its lifetime, and requires a smaller heat sink and board that will lower the overall cost of the module. It uses Infineon IMW65R107M1H SiC MOSFET for 10% and 25% duty cycles and IMW65R048M1H for 40% duty cycle at 35 kHz switching frequency. Measurement results show a 51.2 W high-side transistor power loss (P_{Hloss}) reduction for a 10% duty cycle at I_O = 5A and 75W and 20.3W for a 25% and 40% duty cycle, respectively, at I_O = 8A.

II. Principle of Independent Constant Pulse PWM Scheme

A. Current fixed-frequency PWM scheme

Fig. 1 and 2 shows the schematic diagram and modulation technique of TL494 for the conventional fixed-frequency PWM control circuit [11]. The modulation of the output waveforms V_{PWM_01} and V_{PWM_02} is accomplished by comparing the sawtooth waveform V_{ramp} to either of two

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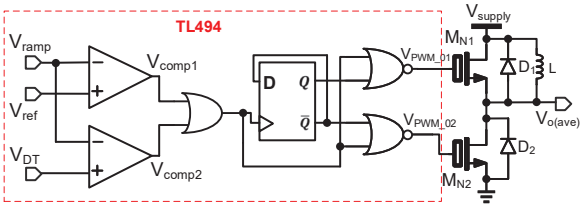

Fig. 1. TL494 PWM generator schematic diagram [11]

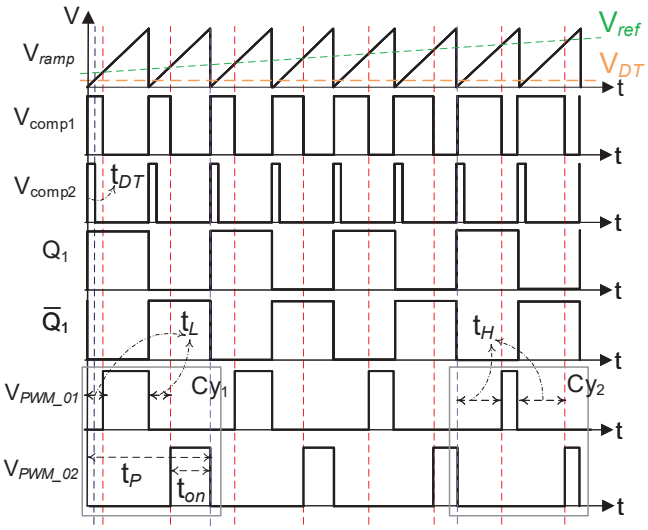

Fig. 2. Conventional PWM timing diagram [11]

control signals, V_{ref} and V_{DT} (dead time). When V_{ramp} is higher than V_{ref}, V_{PWM_02} is high, and V_{PWM_01} is low. In this state, M_{N1} is off while M_{N2} is on. V_{PWM_02} is responsible for controlling the output voltage $V_{o(ave)}$ to the load through M_{N2}. The $V_{o(ave)}$ can be calculated using Eqn. (1),

$$V_{o(ave)} = V_{supply} \cdot \frac{t_{on}}{t_P} \tag{1}$$

where t_{on} is the control pulse on time and t_P is the duty cycle. The function of M_{N1} is to act as a free-wheeling switch that will provide a low-resistance path for the current. The purpose of V_{DT} is to avoid shoot-through in M_{N1} and M_{N2} during the transition of signals V_{PWM_01} and V_{PWM_02} . Therefore, there are instances when both V_{PWM_01} and V_{PWM_02} are off at certain period. Referring to Fig. 2, V_{PWM_01} and V_{PWM_02} are identical and 180 degrees out of phase with each other. When M_{N2} is on, the inductive load L will charge energy. Once if M_{N2} is off and M_{N1} is on, L is discharged through the low-resistance path. For the high value of $V_{o(ave)}$ applications, t_{on} must be also high while the time where both transistors are off is low (t_L). This will allow M_{N1} more time to discharge the energy stored through L. Notably, the high-side transistor will contributes major power loss to the whole system. The total power loss at the high-side transistor can be calculated

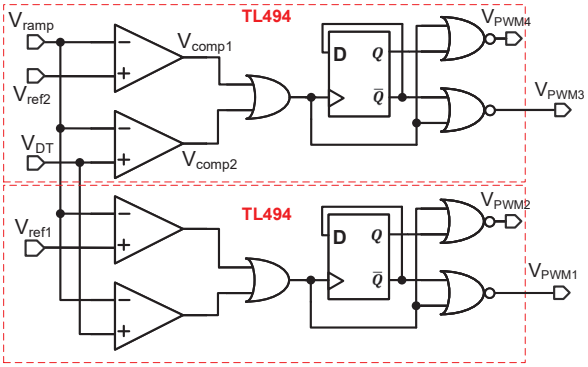

Fig. 3. Proposed PWM generator using two TL494.

using Eqn. (2),

$$P_{Hloss} = P_{ONH} + P_{DTtot} \tag{2}$$

$$P_{ONH} = I_O^2 \cdot R_{ONH} \cdot \frac{V_o}{V_{in}} \tag{3}$$

$$P_{DTtot} = V_{diode} \cdot I_O \cdot (t_{Dtrise} + t_{Dtfall}) \cdot f_{sw} \tag{4}$$

where P_{Hloss} and P_{ONH} [12] is the high-side transistors power loss and conduction loss, respectively, P_{DTtot} is overall dead time loss [12], and f_{sw} is the switching frequency. However, during a low duty cycle application, t_{on} of V_{PWM_01} is low. The time when M_{N1} and M_{N2} are off in this state is high (t_H). This will result in a limited time to discharge the energy stored in L. Also, D_1 conducts most of the time which will cause a higher voltage drop compared to the scenario that M_{N1} is on, and high power loss.

B. Proposed PWM approach

The proposed pulse generation scheme consists of two TL494s connected in synchronous mode sharing the same ramp signal as shown in Fig. 3. As mentioned, the conventional produced identical PWMs with 180 degrees out of phase with each other. In the proposed circuit, the signal that will go to the high-side transistor is independent of the signal that will drive the load.

Fig. 4 shows the timing diagram for the proposed circuit. The circuit generates 2 sets of outputs, namely V_{PWM1} and V_{PWM2}, and V_{PWM3} and V_{PWM4}. V_{PWM3} in the proposed circuit will deliver maximum time for M_{N1} to turn on and independent to the pulse coupled to M_{N2}. This can be calculated using Eqn. (5),

$$t_{on(prop)} = t_{HC} - t_{DT} \tag{5}$$

where t_{HC} is 50% of the total cycle time. The V_{PWM3} provides a long time to discharge the energy stored by L. The on-state time of D_1 is also limited by t_{DT} (minimum) which lessens the power loss. The long turn-on time of the V_{PWM3} will reduce the diode power loss, which improves switching efficiency during the re-circulating current phase.

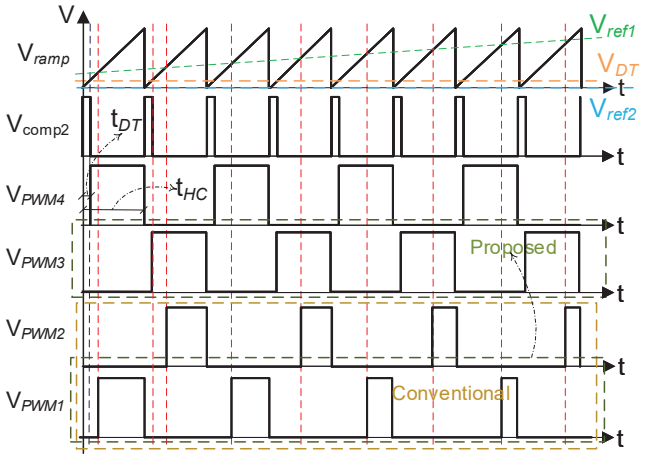

Fig. 4. Proposed PWM scheme.

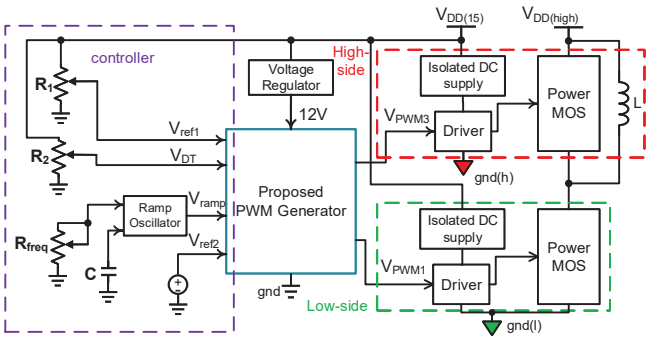

Fig. 5. Synchronous half-bridge converter module block diagram.

TL494 PWM generator has an internal offset of 110 mV that when V_{ramp} = 0 as same as V_{ref2}, it will not require the comparator more transition time [11]. When V_{ref2} is set to 0 V, internally it is biased at 110 mV, and the minimum dead-time, in this case, is approximately equal to $0.03/f_{sw}$.

C. Circuit implementation

Fig. 5 shows the block diagram for the half-bridge converter implementing the proposed pulse scheme. The controller block consists of three potentiometers that will control the oscillation frequency, ramp generator reference voltage, and dead time. The PWM generator composed of two TL494 ICs coupled in the synchronization mode generating the proposed scheme signals that may drive the power MOSFETs. The gate driver provides isolation and impedance matching to the signals from the PWM block. Two sets of 650V SiC power MOSFET are used (Infineon IMW65R107M1H and IMW65R048M1H) for different duty cycles during measurement.

III. Measurement and Analysis

Fig. 6 shows the measurement setup for the half-bridge converter module. The Keithley 2230-30-1 and Chroma 62012P-600-8 are used as power supplies for circuit board (15V) and SiC MOSFET (0 to 100V), respectively. LeCron Wavesurfer

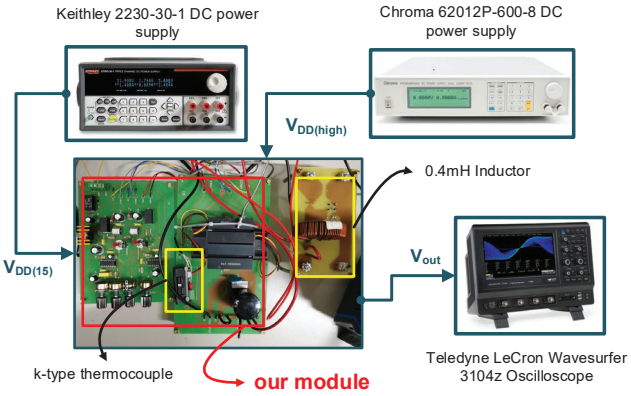

Fig. 6. Constant-pulse scheme half-bridge converter module measurement setup.

3104z is used to monitor output waveforms, including V_{diode}, and V_{RONH}. The SiC MOSFET used in the module is Infineon IMW65R048M1H and IMW65R107M1H with 650V rating and load inductance of 0.4 mH. Fig. 7 shows the waveform comparison for the conventional and proposed circuit with an output current of 0.5 A at f_{sw} = 35kHz and 25% duty cycle using Infineon IMW65R107M1H. The measured V_{diode} for conventional is greater than that of the proposed scheme with the value of 3.6 V and 3.2 V. In contrast to the conventional approach, the proposed approach has a larger V_{RONH}. Referring to Eqn. (2), the calculated $P_{Hloss(conv)}$ = 8.9 W and $P_{Hloss(prop)}$ = 5.1 W resulting in decrease of P_{Hloss} = 3.8 W given same value of V_{out} approximately equal to 7 V. The comparison table between the proposed technique and conventional pulse scheme is tabulated in Table I. The Infineon IMW65R107M1H is used during the 40% duty cycle, while IMW65R048M1H is for both 25% and 10%. The output current is set from 0 to 8A with 0.5 A increment during the 25% and 40% duty cycle. However, because of the high temperature generated by the power MOSFET during the low duty cycle, the output current is limited to 5A at a 10% duty cycle. The highest value P_{Hloss} of 51 W, 75 W, and 20 W, for 10%, 25%, and 40% duty cycle, respectively, occurs when the value of I_O is equal to the maximum. For every duty cycle with a 5 A output current, the 10% duty cycle produces the highest P_{Hloss} reduction.

Fig. 8 (a), (b), and (c) shows the graphical relationship of I_O and P_{Hloss} for each duty cycle. As output current increases, the P_{Hloss} also increases, resulting in higher power loss reduction. Referring to Table I, the maximum P_{Hloss} can be reduced as much as 45%. This proves that the proposed PWM scheme has low power loss compared to the conventional half-bridge control scheme.

IV. Conclusion

This study demonstrates a novel PWM scheme that produces a maximum turn-on time for high-side MOSFET in a half-bridge converter. This feature reduced the high-side MOSFET

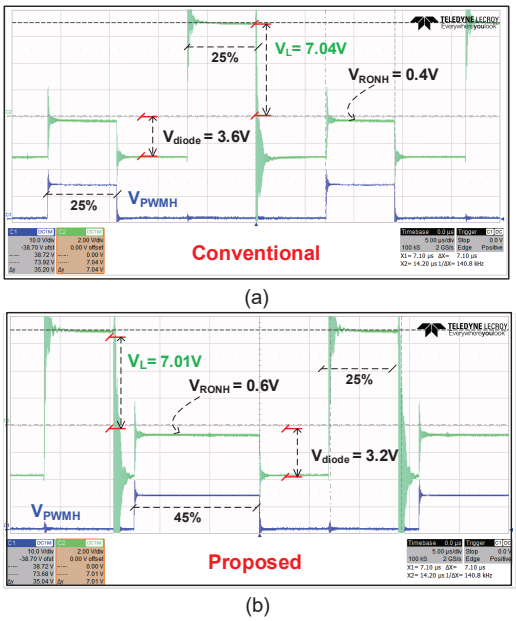

Fig. 7. Output waveform comparison at 25% duty cycle, f_{sw} = 35 kHz and I_O = 0.5 A (a) conventional PWM; (b) the proposed method.

TABLE I
COMPARISON OF POWER LOSS FOR CONVENTIONAL AND PROPOSED HALF-BRIDGE CONVERTERS.

	Power loss (W)					
	40% duty cycle		25% duty cycle		10% duty cycle	
I_O (A)	conv	prop	conv	prop	conv	prop
0.0	0.0	0.0	0.0	0.0	0.0	0.0
0.5	2.87	2.02	6.67	3.96	12.17	8.71
1.0	6.51	4.74	15.63	8.49	28.37	21.21
1.5	10.49	7.97	24.83	14.98	46.27	33.88
2.0	15.20	12.16	35.76	21.26	68.16	48.42
2.5	19.96	15.58	45.25	27.49	87.43	65.36
3.0	25.56	19.45	58.31	35.21	109.7	81.91
3.5	30.78	23.52	68.06	42.70	133.9	101.5
4.0	37.16	27.93	82.64	49.91	160.9	120.9
4.5	42.75	32.81	92.11	58.98	185.5	140.1
5.0	48.89	37.78	107.7	67.39	211.9	160.8
5.5	54.64	43.04	123.8	76.26		
6.0	62.24	48.91	135.1	85.41		
6.5	69.06	53.64	150.32	96.52		
7.0	75.65	59.61	169.3	105.1		
7.5	82.94	64.89	185.1	115.4		
8.0	90.22	69.96	200.3	125.3		

power loss, which enhanced the overall efficiency of the half-bridge converter compared to the conventional PWM signal. Most of all, during the low duty cycle applications, the power loss reduction is higher as the output current increases. The two TL494 reduce the overall operating temperature of the power transistors, which increases its lifetime and requires a small heat sink on board, lowering the module's cost.

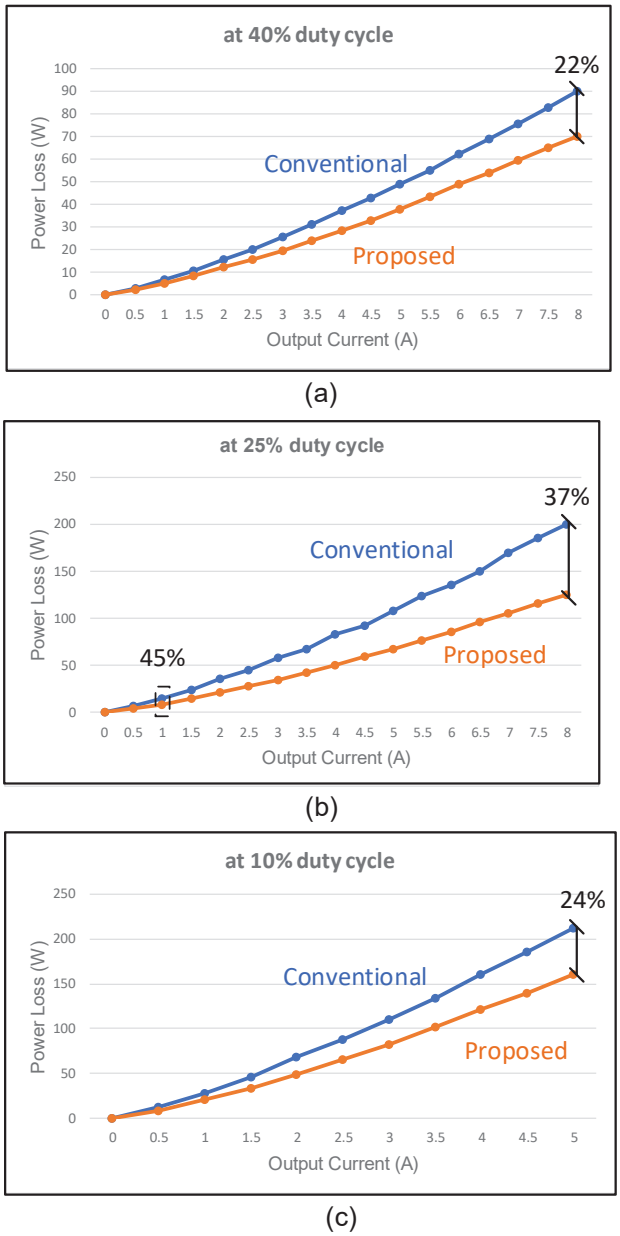

Fig. 8. Power loss comparison of conventional vs proposed at (a) 40%, (b) 25%, and (c) 10% duty cycle.

ACKNOWLEDGMENT

Taiwan's Ministry of Science and Technology (MOST) provided partial support for this research under MOST 110-2623-E-110 -001-, MOST 110-2224-E-110 -004-, and MOST 110-2221-E-110 -063 -MY2.

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