Sub-0.2 pJ/Access Schmitt Trigger Based 1-kb 8T SRAM Implemented Using 40-nm CMOS Process

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***Abstract*—This investigation presents a low-power 1-kb SRAM, where memory cells are based on skewed inverter design. More specifically, Schmitt trigger inverters are utilized in the cell to enhance read, write, and hold capabilities. To minimize power usage, a supply voltage selection circuit is included to the proposed cell, where the supply voltage of the cells is selected in different nodes. The 1-kb SRAM is designed using a typical 40-nm CMOS. The post-layout simulation is presented to verify the low power consumption. The design is operated at 100 MHz clock with an energy per bit simulated to be 5.968 fJ given VDD=0.8 V. The energy/access is simulated to be 0.191 pJ in the same condition.**

***Index Terms*—static RAM, Schmitt trigger, SNM, DNM, stability, low power**

I. Introduction

In computing devices, memory usage time is second to that of the central processing unit. If memory power consumption is reduced, the life cycle of any electronic device can be effectively extended. The battery life of portable devices has been known as a major issue given the rapid development of these devices like smart phones, smart watches, biomedical instruments etc. In digital systems, static random-access memory (SRAM) has been widely used as cache devices. Therefore, the research community has paid considerable attention to the low-power and cost-effective SRAMs.

SRAMs are widely used because it is fast if activated and it is low power if idle. SRAM cells, in comparison to DRAM cells, do not need to be refreshed constantly while it retains the stored value as long as the power is supplied. As CMOS scaling has been applied to deep sub-micron levels, there are problems with threshold leakage, short channel effects, gate dielectric leakage, and others. Power dissipation in this scale is mainly attributed to leakage power. As per the ITRS statement, the bulk of the logic chip area is occupied by the SRAM. Thus, power reduction in SRAM cells will have a major impact on overall power consumption.

Several strategies for reducing SRAM power consumption have been developed. An effective technique to reduce power consumption of SRAMs is through the use of only a single bit-line. Wang *et al.* used different voltage supply to obtain lower power consumption [1]. However, the single-ended cell design results in an asymmetrical static noise margin (SNM), which might affect the stability of the cell during read, write, and hold operations. Besides, with the scaling of VDD, the standard 6T SRAM cell suffers read current disturbance caused due to low supply voltage, the read and write stability of the SRAM is degraded. To counter these challenges, various SRAM topologies were proposed e.g., 7T, 8T, 9T, 10T, and many others [2] [3] [4] [5]. Read decoupling and feedback cutting schemes were proposed in [3]. Read isolation is presented in [2], [4] to reduce read delay and enhance the data stability. Adding another control signal can also improve SRAM performance as reported in [5].

In this report, we proposed a Schmitt trigger based 8T SRAM cell with a better read and write ability while incorporation the subsequent features: (1) low energy consumption by voltage selection, (2) fast access speed by employing a selective power gating technique, and (3) high noise immunity by using Schmitt trigger based inverter configuration.

II. Proposed 1-kb SRAM using Schmitt Trigger based cells

A. 1-kb SRAM Architecture

Fig. 1 shows the architecture of the proposed SRAM. It is composed of the following blocks:

1) 1-kb array with Schmitt trigger based cells
2) Supply (VDD) selection circuit
3) Controller
4) Row and Column Decoders
5) Built-In Self-Test Circuit
6) Energy Reduction
7) Sense Amplifiers
8) Column Multiplexer of the output

B. Schmitt trigger based SRAM Cell

SRAM cell circuits are designed to store one bit of data, and the memory cells contain two stable nodes, namely Q and QB. Through the word lines, the complementary bit lines can be used to access the data bit stored in the memory cell.

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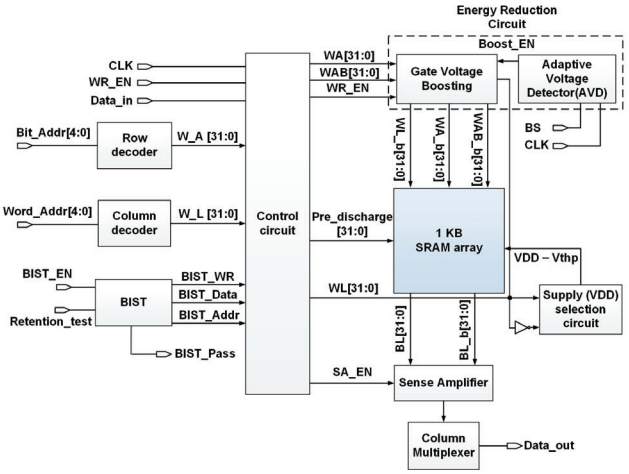

Fig. 1. Proposed 1-kb SRAM architecture

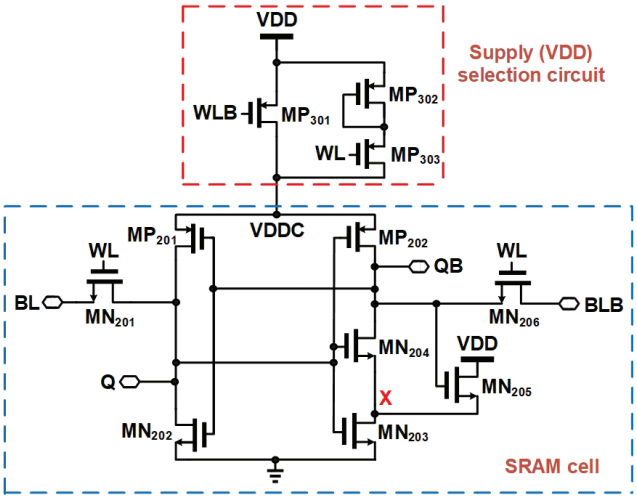

Fig. 2. Proposed SRAM cell with voltage select mode

A Schmitt trigger inverter consisting of MP_{202}, MN_{203}, MN_{204} and MN_{205} are used within the proposed SRAM cell, as shown in Fig. 2, to change the inverter transfer function. The Schmitt trigger inverter acts as a comparator with positive feedback. The feedback transistor, MN_{205}, maintains the output level of the inverter logic '1'. It will raise the voltage of node 'x' to VDD-Vth which will increase the minimum input voltage needed at the input of the Schmitt trigger for raising higher than Vth. Fig. 3 shows the transfer curve of the Schmitt trigger inverter are sharper in comparison with that of the traditional CMOS inverter. Thus, we can use the Schmitt trigger inverter to improve the noise margin of the SRAM cell.

The transistors of those in the Schmitt trigger are sized based on Eqns. (1), (2), and (3) [6]. The pull-up ratio (PR) and cell ratio (CR) of the access transistors MN_{201} and MN_{206} are assigned to be $CR = PR = 1$ to minimize the effect of the negative-bias temperature instability (NBTI) [7]. The

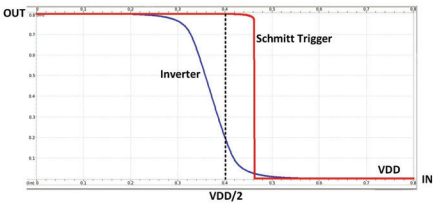

Fig. 3. Voltage transfer curves of Schmitt trigger vs traditional inverter

upper trip-point, V_{SPH} of the Schmitt-trigger is set to be 0.5 V, slightly above 0.5 V_{DD}, to have better hold characteristic for the logic '1' value.

$$PR = \frac{W_{MP202}/L_{MP202}}{W_{MN206}/L_{MN206}} \tag{1}$$

$$CR = \frac{W_{MN202}/L_{MN202}}{W_{MN201}/L_{MN201}} \tag{2}$$

$$\frac{\beta_1}{\beta_3} = \frac{W_{MN203} \cdot L_{MN205}}{L_{MN203} \cdot W_{MN205}} = \left(\frac{V_{DD} - V_{SPH}}{V_{SPH} - V_{THN}}\right)^2 \tag{3}$$

The operation of SRAM memory is classified into three operations: standby operation, write operation, and read operation.

1) Standby operation: MN_{201} and MN_{206} in Fig. 2, namely two access devices, are disconnected from the memory cell during this operation, when the word line is not active. If power is available, the memory cell will retain its previous state. As the column capacitance are charged to supply voltage through MP_{201}, MP_{202}, and MN_{205}. Thus, less energy is consumed by the memory cell.

2) Write operation: To perform the write '0' operation, assume that the data state in the memory cell was previously recorded as logic '1'. The voltage levels present at two of the nodes Q and QB, are VDD and 0 V, respectively. Therefore, the voltage levels present at the transistors MN_{202} and MP_{202} are cut-off, while the transistors MP_{201}, MN_{203}, MN_{204}, and MN_{205} are saturated. The column voltage of the bit line is now driven to logic low. Now the row decoder determines the address of the word line by which transistors are activated via MN_{201} and MN_{206}.

3) Read operation: If the initial state of the memory cell is logic low, when the cell needs to perform a read zero operation. When the operation begins, the storage node Q and the storage node QB are set to 0 V and VDD, respectively. Then, MP_{201}, MN_{203}, MN_{204}, and MN_{205} are cut-off, while MN_{202} and MP_{202} are in the saturation region. A row decoder circuit selects the word line to activate the access transistors MN_{201} and MN_{206}. There is now no current flowing through the transistors because there is virtually no voltage difference between node QB and the voltages at BLB. The transistors MN_{201} and MN_{202}, on the other hand, will drive the BL discharged to the ground from VDD by generating a nonzero current. Then, BL and BLB voltages are fed into the sense

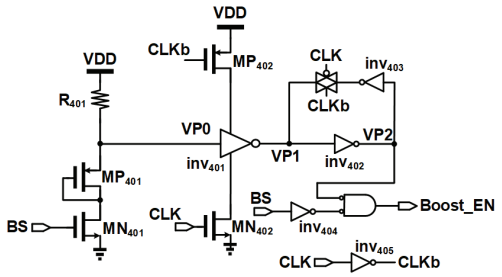

Fig. 4. AVD circuit [1]

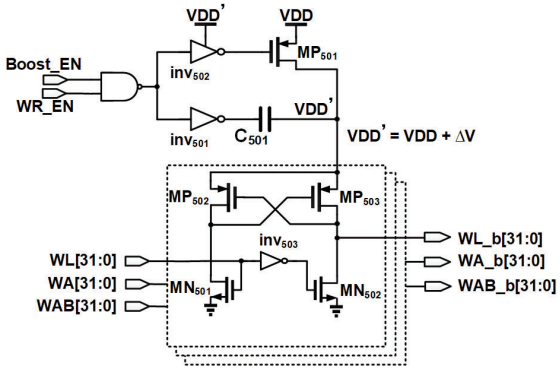

Fig. 5. Proposed gate voltage boosting circuit

amplifier's inputs, and then the sense amplifier outputs logic zero, because there is a voltage difference between BL and BLB.

C. Supply (VDD) selection circuit

Fig. 2 illustrates the proposed SRAM cell with a supply voltage selection circuit that employs three low-Vthp PMOS transistors per column of memory cells to reduce standby power when they are not being accessed.

1) In the standby operation, the supply voltage VDD - Vthp is selected so that WLB is high and WL is low. Since there are no cells being accessed, the power is saved by dropping the supply voltage by Vthp.

2) In Write/Read operations, the WL is high, which turns off MP_{303}. The WLB (low) turns on MP_{301} so that the normal VDD is supplied to the entire column of cells.

D. Energy Reduction

A refined Energy reduction circuit in Fig. 1 mostly consists of GVB (Gate Voltage Boosting) and AVD (Adaptive Voltage Detection), which is meant to save more energy for those cells not activated [1]. However, for those cells to be accessed, this circuit boosts the supply voltage for higher speed. Through the assertion of BS (Boost Select), the entire circuit is activated. To access cells from VDD to VDD', AVD generates Boost_EN to GVB, when BS is pulled high. The following text provides details about the circuit designs.

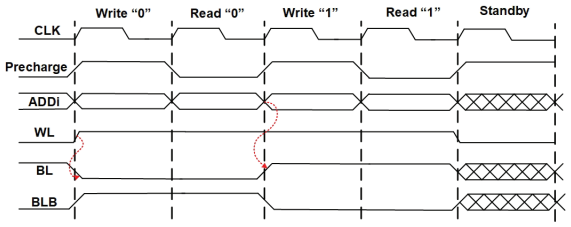

Fig. 6. Read and write cycle timing diagram

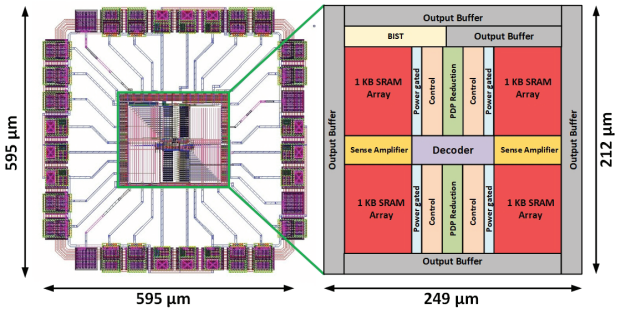

Fig. 7. Layout of the proposed 1-KB SRAM

1) Adaptive Voltage Detection: Fig. 4 shows the adaptive voltage detector in Energy reduction circuit. When the input BS signal reaches a high value bringing MN_{401} to ground, the AVD is triggered. VP0 will be grounded by MP_{401} and MN_{401}, and thus VP1 will have high value when clock is high. By means of a feedback loop composed of inv_{402}, inv_{403} and a transmission gate, the VPO and switching voltage is compared at VP1. To conclude, Boost_EN is generated when VP1 and BS are inversed, corresponding to VP2 and $\overline{BS}$.

2) Gate Voltage Boost Circuit: AVD is activated as described in the previous section once if BS is pulled up to logic 1. While AVD has not finished the system voltage detection, the Boost_EN of AVD remains 0. By pulling inv_{501} down to the ground, the top plate of the MP2 and MP3 will be lowered towards the ground, while MP_{502} and MP_{503} will pull up to the VDD. By pulling Boost_EN high in the presence of a higher system voltage than the switching voltage, AVD enhances the switching power. Consequently, it becomes inactive. After PVB enters the boost mode, which means MP_{502} and MP_{503} are turned off and the top plate of C_{501} is pulled higher than the original VDD, called VDD'=VDD+ΔV, when WR_EN pulls high, one of the SRAM cells will start a writing or reading operation. Thanks to the elevation of the supply voltage, the access operation of the activated cell will be fastened.

III. Simulations and Verification

The proposed SRAM is implemented using a typical 40-nm CMOS technology. The chip area is 595 × 595 μm^2 with a 249 × 212 μm^2 core as shown in Fig. 7. Referring to Fig. 8, all-PVT-corners post-layout simulation of the proposed design shows an SNM of 608.11 mV in the worst case. It also has

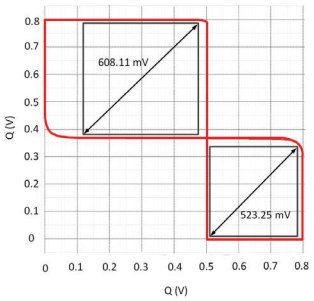

Fig. 8. SNM of the proposed SRAM cell

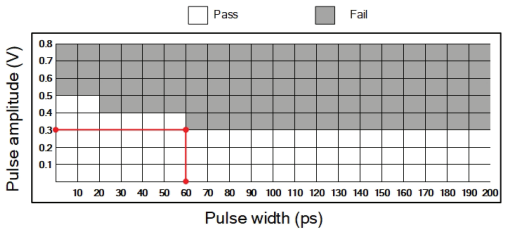

Fig. 9. DNM of the proposed SRAM cell

steeper response very close to ideal transfer curve due to the presence of the positive feedback transistor. The SRAM can will start to fail when there is a current disturbance on the cells equivalent to a pulse amplitude of 0.3 V and pulse width of 60 ps as shown by its dynamic noise margin (DNM) in Fig. 9. Fig. 10 is the post-layout simulation to show W1/R1/W0/R0 operation for all 45 PVT corners.

Table I shows the comparison with several previous SRAM designs in the last 5 years. The proposed SRAM achieved the lowest energy per access and energy per bit, 0.191 pJ and 5.968 fJ, respectively. It also offered the best SNM because of the added Schmitt trigger circuit at the expense of a larger cell area.

IV. Conclusion

A 1-kb low-power SRAM design using skewed cell is implemented using typical 40-nm CMOS technology. The cells are designed to utilize skewed inverters to improve on the static noise margin performance. A Schmitt trigger is paired with a regular inverter for the memory cell. A voltage supply selection circuit is presented to reduce power consumption of the memory array when in standby mode, while a voltage boost circuit is added to reduce the delay during read/write operations.

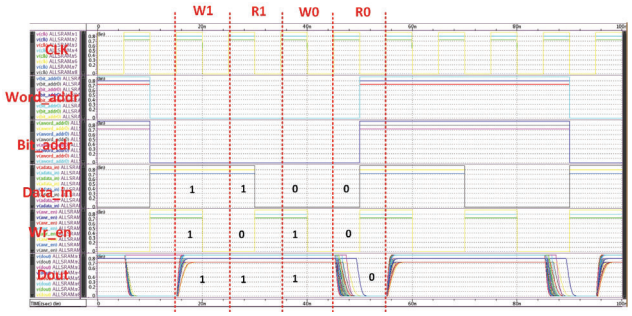

Fig. 10. All PVT corner post-layout simulation at 100 MHz clock rate

TABLE I
Comparison with previous works

	[8]	[9]	[10]	[1]	This Work
Year	2017	2018	2021	2021	2022
Tech. (nm)	65	65	40	16	40
Cell	6T	6T	6T	6T	8T
V_{DD}	1.2	1.2	0.9	0.8	0.8
SNM (mV)	N/A	N/A	377	504.76	608.11
Capacity (kb)	1	8	1	1	1
Word Length	32	32	32	32	32
Frequency (MHz)	100	20	200	500	100
Energy/access (pJ)	2.2	0.592	0.2313	0.219	0.191
Energy/bit (fJ)	68.75	18.5	7.23	6.8	5.968
Core Area (mm^2)	0.013	0.019	0.01	0.02	0.05

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References

[1] C.-C. Wang, R. G. B. Sangalang, and I.-T. Tseng, "A single-ended low power 16-nm FinFET 6T SRAM design with PDP reduction circuit," *IEEE Tran. Circuits Syst. II- Exp. Briefs*, vol. 68, no. 12, pp. 3478–3482, Dec. 2021.

[2] K. Mehrabi, B. Ebrahimi, and A. Afzali-Kusha, "A robust and low power 7T SRAM cell design," in *2015 18th CSI Int. Symp. Comput. Architecture Digital Syst. (CADS)*. IEEE, Oct. 2015, pp. 1–6.

[3] C. B. Kushwah and S. K. Vishvakarma, "A sub-threshold eight transistor (8T) SRAM cell design for stability improvement," in *2014 IEEE Int. Conf. IC Design Technol. (ICICDT)*, May 2014, pp. 1–4.

[4] A. S. Yadav and S. Nakhate, "Characterization of high speed 9T SRAM cell with enhanced data stability," *Mater. Today*, vol. 4, no. 9, pp. 10 356–10 361, 2017.

[5] M. Bansal, A. Kumar, P. Singh, and R. Nagaria, "A novel 10T SRAM cell for low power applications," in *2018 5th IEEE Uttar Pradesh Section Int. Conf. Elect. Electron. Comput. Eng. (UPCON)*, Nov. 2018, pp. 1–4.

[6] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed. John Wiley & Sons, Inc., Aug. 2010.

[7] A. Chenouf, B. Djezzar, H. Bentarzi, and A. Benabdelmoumene, "Sizing of the cmos 6T-SRAM cell for NBTI ageing mitigation," *IET Circ. Devices Syst.*, vol. 14, no. 4, pp. 555–561, 2020.

[8] J. Lee, D. Shin, Y. Kim, and H.-J. Yoo, "A 17.5-fJ/bit energy-efficient analog SRAM for mixed-signal processing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 10, pp. 2714–2723, Oct. 2017.

[9] N. Surana and J. Mekie, "Energy efficient single-ended 6-T SRAM for multimedia applications," *IEEE Tran. Circuits Syst. II- Exp. Briefs*, vol. 66, no. 6, pp. 1023–1027, Jun. 2019.

[10] C.-C. Wang and C.-P. Kuo, "200-MHz Single-Ended 6T 1-kb SRAM with 0.2313 pJ Energy/Access using 40-nm CMOS Logic Process," *IEEE Tran. Circuits Syst. II- Exp. Briefs*, vol. 68, no. 9, pp. 3163–3166, Sep. 2021.