A 40-nm CMOS Wide Input Range and Variable Gain Time-Difference Amplifier Based on Current Source Architecture

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***Abstract*—A time-difference amplifier (TDA) with a wide time-difference input range and variable gain is presented in this paper. Its time amplification is performed using novel current source architecture, phase detection, and variable delay circuits. After time amplification, to avoid the current sources for charging and discharging capacitors simultaneously, a reset circuit is added. To widen the input time-difference range, an adjustable current source control is added. The proposed TDA is implemented using TSMC 40-nm CMOS process. The core area is 209.42×84.775 μm^2. Though our design is driven by a lower supply voltage, it has the widest time-difference input range and the largest FOM among all existing TDAs.**

***Index Terms*—current source, delay, gain, phase detection, time amplifier.**

I. Introduction

The demand for high time precision in modern systems development is increasing. Both time-to-digital converters (TDC) and all-digital phase-locked loops (PLLs) have high-resolution requirements. As in general use, the time measurement to achieve a resolution of nanoseconds (ns) is usually based on the clock period generated by a quartz crystal. In special applications such as laser range-finder and logic analyzer, when it is necessary to conduct time measurement at a picosecond level resolution, TDC is commonly utilized. For a TDC circuit architecture, when its resolution is higher, its performance is better [1], [2]. To improve the precision of each bit conversion, the TDC can be further improved by using a time-difference amplifier (TDA) in its circuit besides using coarse-fine [3] or Vernier-Bias [4] TDCs. In coarse-fine TDC, the time-difference is sent to its TDA for amplification. The amplified sampling error is then sampled again in fine TDC architecture, thereby increasing the resolution of the entire TDC. Furthermore, a TDA with a wide linear input time difference and a stable gain is necessary.

Prior designs of TDAs, such as, SR-latch [5], closed-loop DLL [6], cross-coupled [7], and time latch [8] have both limited gain and input time difference. Meanwhile, TDAs that used feedback gain control [9] and modified SR latch [10] have only variable gain and variable input time difference, respectively. In this paper, to achieve both variable input time-difference range and gain, a novel TDA is proposed based on modified timing signal and redesigned current source architectures of the previous circuits [11], [12]. To achieve a wider time-difference input range, the current source control is adjusted. A Reset Circuit was added for discharging the capacitors at the output after time amplification is completed; thus, enabling the TDA to perform time amplification again (TDA is reused) for another input time difference. With this, the proposed TDA design has a variable gain, wider input time difference, and small gain error.

II. System Architecture of the Proposed Time-Difference Amplifier (TDA)

The block diagram of the proposed TDA is shown in Fig. 1 where all the blocks will be discussed in the succeeding subsections.

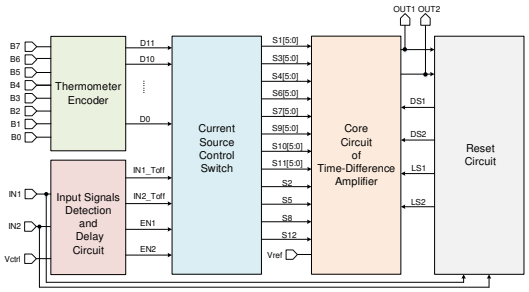

Fig. 1. Block diagram of the proposed time-difference amplifier (TDA).

A. Input Signals Detection and Delay Circuit

Referring to Fig. 2, two square wave input signals, namely, IN1 and IN2 pass through the Input Signals Detection and

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Delay circuit in Fig. 1. This circuit consists of 2 blocks: Detection Circuit and Delay Circuit. Detection Circuit in Fig. 3(a) is used to determine which input signal is earlier or leading. It generates EN1 and EN2 signals which enable Current Source Control Switch circuit. Referring to Fig. 2 again, if IN1 is earlier than IN2, EN1 is high and EN2 is low; thus, time amplification is finished in the first cycle. If IN2 is earlier than IN1, EN2 is high and EN1 is low; time amplification is finished in the second cycle. Meanwhile, the schematic of Phase Detector circuit in Fig. 3(a) is shown in Fig. 3(b). The said phase detector generates a 1-bit signal Detect_ which serves as selection signal of MUX to output EN1. The D flip-flop of Detection Circuit receives Detect_ and take the inverted phase of the input signal IN1 as a clock to generate EN2. To resolve the large leakage current during the switch-off intervals of current sources, I_{B1} and I_{B3} of the proposed TDA as shown in Fig. 4, Delay Circuit as shown in Fig. 5(a) is designed to generate same time delays (T_{off}) at different corners. Every input signal (IN1 and IN2) are respectively delayed by a value of T_{off} in picoseconds through the Delay Circuit to generate outputs, IN1_Toff and IN2_Toff. The external bias voltage is Vctrl, and the Pctrl is generated internally to adjust the delay time of the input signal.

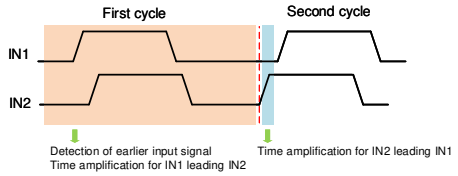


Fig. 2. Timing diagram showing detection of earlier input signal.

B. Thermometer Encoder and Current Source Control Switch

The 8-bit Thermometer Encoder (TE) shown in Fig. 5(b), which uses four 2-bit binary-to-thermometer decoders [13] converts the input into 12-bit thermometer code (D[11:0]).

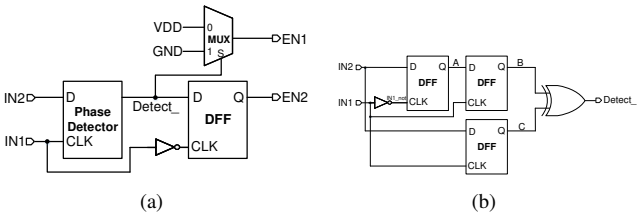


Fig. 3. (a) Input Signals Detection circuit; (b) Phase Detector circuit.

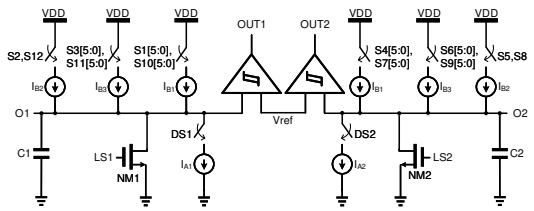


Fig. 4. Core Circuit of the Time-Difference Amplifier.

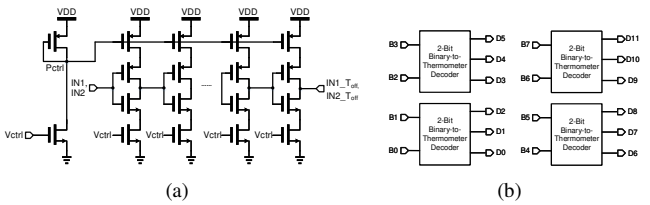


Fig. 5. (a) Delay Circuit; (b) Thermometer Encoder circuit.

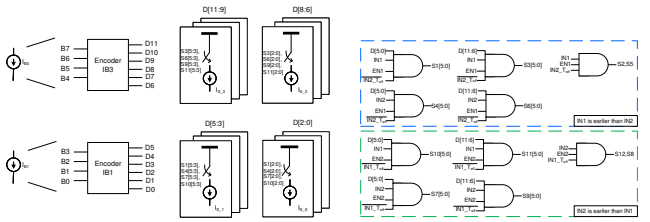


Fig. 6. (a) Current Source Control Switch diagram for I_{B1} and I_{B3}; (b) Current Source Control Switch circuit for IN1 leading IN2 and IN2 leading IN1.

Referring to Fig. 6(a), the output code D[11:6] corresponds to input code B[7:4] and current source I_{B3}, while code D[5:0] corresponds to B[3:0] and I_{B1}. The resulting thermometer code serves as input to Current Source Control Switch, corresponding to four groups of current sources with different weights or values. Its function is demonstrated as follows: assume the 4 currents, I_{S_0} = 10 μA, I_{S_1} = 50 μA, I_{S_2} = 100 μA, and I_{S_3} = 150 μA. If the B[3:0] is high and B[7:4] is low, the total current will be 10 μA$\times$3 + 50 μA$\times$3 = 450 μA. The resulting total current depends on the thermometer input code (B[7:0]). Current sources I_{B1}, I_{B2}, and I_{B3} are controlled by Current Source Control Switches (made of 3 or 4-input AND gates), S1 to S12, as shown in Fig. 6(b). Different switch architectures are made provided that IN1 is earlier than IN2 or IN2 is earlier than IN1.

C. Core Circuit of Time-Difference Amplifier (TDA)

The operation of the proposed symmetric Core Circuit of TDA as shown in Fig. 4 is described as follows: When IN1 is earlier than IN2: The two input signals IN1 and IN2 remain low initially. Letting C1 = C2 = C and $I_{A1} = I_{A2}$, node O1 of Fig. 4 will be as follows:

$$\begin{aligned}(I_{B1}+I_{B3})\cdot(\Delta T_{IN}+T_{off})+I_{B2}\cdot\\ [T3-(\Delta T_{IN}+T_{off})]=V_H\cdot C\end{aligned} \tag{1}$$

Meanwhile, node O2 of the same figure becomes:

$$\begin{aligned}(I_{B1}+I_{B3})\cdot T_{off}+I_{B2}\cdot\\ [T4-(\Delta T_{IN}+T_{off})]=V_H\cdot C\end{aligned} \tag{2}$$

Getting the values T3 (Eqn. (3)) and T4 (Eqn. (4)) to determine the TDA's gain (Eqn. (5)) :

$$\begin{aligned}T3=\frac{V_H\cdot C-(I_{B1}+I_{B3})\cdot(\Delta T_{IN}+T_{off})}{I_{B2}}\\ +(\Delta T_{IN}+T_{off})\end{aligned} \tag{3}$$

$$T4=\frac{V_H\cdot C-(I_{B1}+I_{B3})\cdot T_{off}}{I_{B2}}+(\Delta T_{IN}+T_{off}) \tag{4}$$

$$Gain = \frac{\Delta T_{OUT}}{\Delta T_{IN}} = \frac{T4 - T3}{T1 - T0} = \frac{I_{B1} + I_{B3}}{I_{B2}} \quad (5)$$

where V_H is the high compare switching voltage of Schmitt trigger comparator (V_H= 0.7 V), and V_L is the low compare switching voltage (V_L= 0.2 V), IN1_Toff and IN2_Toff are the delayed signals of IN1 and IN2, respectively, T_{off} is the delay time (assuming 640 ps), ΔT_{IN} is input time difference (T0-T1), and ΔT_{OUT} is out time difference (T4-T3). Fig. 7 shows the resulting timing diagram of the proposed TDA in Fig. 1 when IN1 is earlier than IN2.

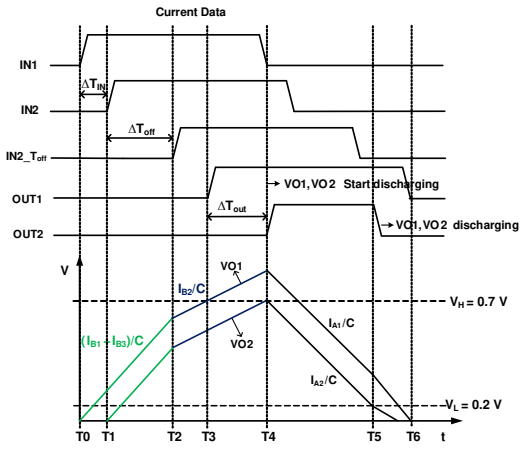


Fig. 7. Timing diagram of the proposed TDA when IN1 is earlier than IN2.

The timing diagram in Fig. 7 is explained as follows. At node O1, the operation is:

- At time intervals T0-T2: It is (ΔT_{IN} + T_{off}) where current sources I_{B1} and I_{B3} are charging C1. At T0, IN1 goes high, and IN2_Toff remains low.
- In T2-T3, I_{B1} and I_{B3}'s switches are closed. I_{B2} is charging C1. At T2, IN1 remains high and IN2_Toff goes high. At T3, O1's voltage (VO1) equals V_H and OUT1 goes high.

Apparently, the operation at node O2 is described as:

- At T1-T2: That is T_{off}. I_{B1} and I_{B3} are charging C2. At T1, IN2 goes high and IN2_Toff remains low.
- In T2-T4, I_{B1} and I_{B3}'s switches are closed. I_{B2} is charging C2. At T2, IN1 remains high and IN2_Toff goes high. At T4, O2's voltage (VO2) equals V_H and OUT2 goes high.

When OUT1 and OUT2 become high, the time amplification is finished. Then, discharging is done by the Reset Circuit in Fig. 1. Based on the timing diagram (Fig. 7), the discharging is explained as follows:

- In T4-T5: When OUT1 and OUT2 become high, reset switches for I_{A1} and I_{A2}, namely, DS1 and DS2, respectively, in Fig. 4 start discharging C1 and C2.
- In T5-T6: To avoid I_{B2} and I_{A1} & I_{A2} for charging and discharging C1 or C2, respectively, at the same time, another reset switches for NM1 and NM2, namely LS1 and LS2, respectively, are included. When any of the signals, namely, IN1, IN2, OUT1, OUT2, $\overline{OUT1}$, $\overline{OUT2}$ are low, LS1 and LS2 become high; thus, C1 and C2 are discharged.
- After T6: the reset function is finished.

As an example, Table I shows all the states of the Current Source Control Switches and Reset Switches (DS1, DS2, LS1, LS2) in Fig. 4 when thermometer codes B[7:1] is low, B[0] is high, and S1[5:1], S3[5:1], S4[5:1], S6[5:1] are low. Only I_{S_0} is selected.

TABLE I
STATE TABLE OF CURRENT SOURCE CONTROL SWITCHES AND RESET SWITCHES FOR EVERY TIME INTERVAL

Time Interval	S1[0]	S3[0]	S4[0]	S6[0]	S2	S5	DS1, DS2	LS1, LS2
T0-T1	1	1	0	0	0	0	0	0
T1-T2	1	1	1	1	0	0	0	0
T2-T4	0	0	0	0	1	1	0	0
T4-T5	0	0	0	0	0	0	1	0
After T5	0	0	0	0	0	0	0	1

Since the gain of the proposed TDA must be kept at a current bias ratio $\frac{(I_{B1}+I_{B3})}{I_{B2}}$, VO1 and VO2 should not exceed V_H when I_{B1} and I_{B3} are charging C1 or C2 as shown by Eqn. (6).

$$\frac{I_{B1} + I_{B3}}{C} \cdot (\Delta T_{IN} + T_{off}) \leq V_H \quad (6)$$

Therefore, the maximum linear input time difference (ΔT_{INMAX}) for this proposed TDA is given by Eqn. (7):

$$\Delta T_{INMAX} \leq \frac{V_H \cdot C}{I_{B1} + I_{B3}} - T_{off} \quad (7)$$

From the timing diagram (Fig. 7), during T1 to T2 time intervals (first stage of charging), VO1 and VO2 will be charged to a voltage value of $\frac{(I_{B1}+I_{B3})\cdot T_{off}}{C}$. Then, during the next intervals (second stage), they will be charged by I_{B2}. This scenario is represented as Eqn. (8):

$$(I_{B1} + I_{B3}) \cdot T_{off} + I_{B2} \cdot (t - T_{off}) = V_H \cdot C \quad (8)$$

Then, by manipulating Eqn. (8), the maximum input signal frequency (f_{MAX}) is determined in Eqn. (11):

$$t \geq \frac{V_H \cdot C - (I_{B1} + I_{B3} - I_{B2}) \cdot T_{off}}{I_{B2}} \quad (9)$$

$$T_{MIN} \geq \frac{2[V_H \cdot C - (I_{B1} + I_{B3} - 2I_{B2}) \cdot T_{off}]}{I_{B2}} \quad (10)$$

$$f_{MAX} \leq \frac{I_{B2}}{2[C \cdot V_H - (I_{B1} + I_{B3} - 2I_{B2}) \cdot T_{off}]} \quad (11)$$

where T_{MIN} is the shortest cycle of IN1 and IN2 while (t + T_{off}) is the shortest time when IN1 and IN2 remain high.

D. Reset Circuit

For the Reset Circuit, the Boolean functions are given by: $LS1, LS2 = \overline{IN1 \cdot IN2 \cdot OUT1} + \overline{IN1 \cdot IN2 \cdot OUT2}$ and $DS1 = DS2 = OUT1 \cdot OUT2$ where DS1 and DS2 are switches of I_{A1} and I_{A2}, respectively while LS1 and LS2 are switches for MN1 and MN2, respectively.

TABLE II
COMPARISON OF THE PERFORMANCE OF PROPOSED TDA WITH THE EXISTING TDAS

	This work	ICECS [10]	ISCAS [8]	NRSC [14]	DCAS [9]	ISCAS [7]	EL [15]	EL [11]	VLSI [6]
Year	2021	2020	2018	2016	2016	2016	2012	2011	2009
Process (nm)	40	180	65	130	130	180	90	65	65
Result[1]	Post-sim	Meas.	Pre-sim	Pre-sim	Pre-sim	Pre-sim	Pre-sim	Pre-sim	Meas.
Supply Voltage (V)	0.9	1.8	1.0	1.2	1.2	1.2	1.0	1.0	1.2
Gain	2.4-57.8	1.54	2-8	4	25.06-734.9	2	21	2-20	4.784±1.4%
Input Diff. Range (ps)	±13730	±130	200	34	±20	300	30	±400	±300
Gain Error (%)	<4	<6.5	<4	N/A	N/A	N/A	N/A	0.10	1.4
Max. clock freq. (MHz)	14	1000	0.45	1000	2	1000	N/A	N/A	N/A
Power (μW)	4311	2230	518.8	N/A	91.54	28	N/A	740	314 (core)
Core area (mm^2)	0.01775	0.000182	N/A	N/A	N/A	N/A	N/A	N/A	0.1127
FOM[2]	5.8	2.8	3.2	2.3	4.3	2.9	2.5	3.9	3.3

[1]Pre-sim = pre-layout simulation; Post-sim = post-layout simulation; Meas. = Measured results
[2]FOM = log[Input Difference Range × Gain × (Supply Voltage)^2] (ps·V^2)

III. SIMULATION RESULTS

The proposed TDA was realized using TSMC 40-nm CMOS process. Its layout is shown in Fig. 8 where its core area is 209.42×84.775 μm^2. Based on post-layout simulation results at a clock frequency of 3.3 MHz, I_{B1}+I_{B3} = 321.3 μA and I_{B2} = 19.6 μA where the ideal gain = $\frac{I_{B1}+I_{B3}}{I_{B2}}$ = 16.4. When IN1 leads IN2 as shown in Fig. 9, the resulting gain = $\frac{2.11\ ns}{130\ ps}$ = 16.23 and the gain error = $\frac{|16.4-16.23|}{16.4}$ = 1.036%; otherwise, when IN2 leads IN1 as shown in Fig. 10, the resulting gain = $\frac{511\ ps}{30\ ps}$ = 17 and the gain error = $\frac{|16.4-16.23|}{17}$ = 3.65%. A gain error is blamed to the leakage current when the current source is switched and the current source changes with VO1 and VO2. Fig. 11(a) showing the input time vs. output time difference curve proves the linearity of the gain of the proposed TDA at different possible variable gains. Fig. 11(b) shows that the TDA's gain error is kept under 4%. The performance of the proposed TDA is compared with several prior works and summarized in Table II. Notably, the widest input difference range and the largest Figure of Merit (FOM) were achieved by the proposed TDA (designed in the lowest supply voltage) among all existing TDAs.

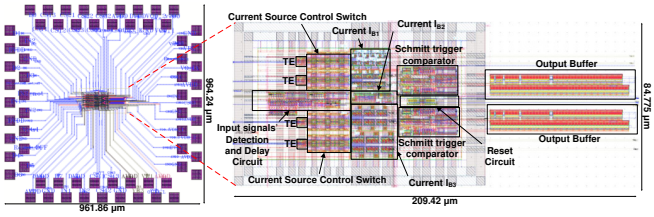


Fig. 8. Layout of the proposed TDA.

IV. CONCLUSION

In this study, a time-difference amplifier (TDA) is designed using 40-nm CMOS process having a widest time-difference input range and largest FOM compared with prior works. Future work and development include fabrication, testing, and measurement of the proposed TDA chip.

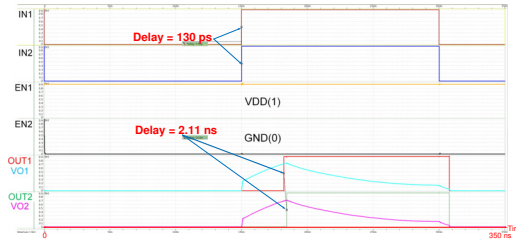


Fig. 9. Time amplification when IN1 is leading IN2 at ΔT_{IN} = 130 ps

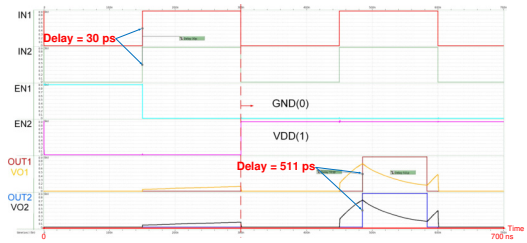
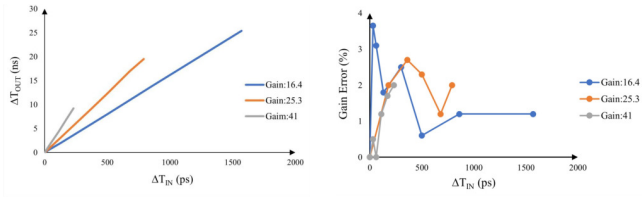


Fig. 10. Time amplification when IN2 is leading IN1 at ΔT_{IN} = 30 ps



(a) (b)

Fig. 11. (a) Input time difference vs. output time difference of the proposed TDA at different gain values; (b) Gain error of the proposed TDA at different gain values.

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