On-chip CMOS Corner Detector Design for Panel Drivers*

Pang-Yen Lou
Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email: lou0105cat@vlsi.ee.nsysu.edu.tw

Ying-Xuan Chen
Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email: polarcatnt@vlsi.ee.nsysu.edu.tw

Chua-Chin Wang[1]
Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

***Abstract*—A high accuracy all-PVT-corner sensing system consisting of three individual sensors is demonstrated in this investigation. The supply voltage sensor is featured with a feedback control block comprising multi-stage delay cells using high Vth devices. The temperature senor realized basing on a current-to-pulse converter is proved to attain a transfer function with very high linearity of sensing. The N- and P-device process variation detectors are carried out using ring oscillators, respectively, such that all the process corners can be clearly differentiated using pulse counts.**

***Index Terms*—PVT corners, high resolution, pulse count, linearity, ring oscillator**

I. Introduction

The consistency of panel displays has become the major quality and reliability so as to cause the demand of ensuring high quality of panel driver ICs. Three well-known factors affecting the quality of driver ICs are manufacturing process, supply voltage, and temperature variations, namely PVT variations or corners. Not surprisingly, many prior methods were reported to sense or detect PVT variations on chip, e.g., [1]. Though many of these works have been proved effectively on PVT corner detection, they were not specifically considered for the panel applications. If the display device is used in a poor voltage or high temperature scenario, the controller thereof might like to take certain actions correspondingly to keep the brightness or contrast of the display. In this investigation, high precision P, V, T, sensors are proposed, respectively, to resolve the demand of consistency display quality of panel-based products.

II. High-precision PVT Corner Sensors

In order to achieve high resolution sensing of PVT corners for panel applications, a cost-effective solution is disclosed in Fig. 1, where the sensing of P, V, T are individually carried out by 3 different circuits such that any possible inter-correlation or interference of these variations is avoided. These 3 sensing circuits will finally generate their respective digit codes to be used in any follow-up usage.

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[1]Prof. C.-C. Wang is also with Inst. of Undersea Tech., National Sun Yat-Sen Univ., Kaohsiung, Taiwan. He is also the contact author.

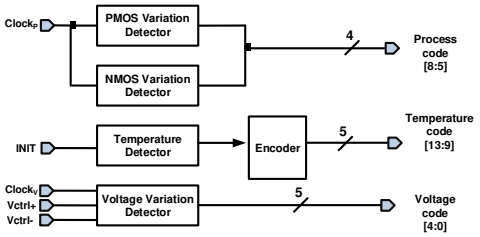

Fig. 1. Proposed PVT corner sensing system

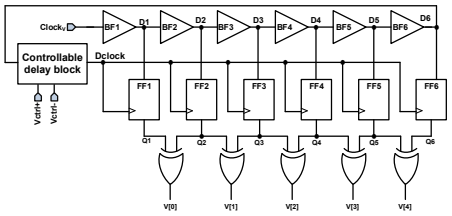

Fig. 2. Schematic of the proposed voltage variation detector

A. Supply voltage sensing

The schematic of Voltage Variation Detector in Fig. 1 is shown in Fig. 2, consisting of a buffer delay line (BDL), DFFs, XORs, and a Controllable Delay Block (CDB). Notably, all the cells in this circuit is also driven by the same V_{in}(VDD) such that it is a robust design. The operation of this circuit is summarized as follows.

- Due to the variation of V_{in}(VDD), the delay generated by the buffer delay line will be varied accordingly.
- The generated codes at each delay cell are registered by corresponding DFFs, which are then XORed with the output of the adjacent DFF to generate Voltage code, V[0]-V[4].
- D6, namely the last output of the buffer delay line, is coupled to an input of CDB such that it is a feedback system.

B. Wide range temperature sensing

Referring to Fig. 1 again, the temperature sensor block diagram is given in Fig. 3, where Current Generator (CG), Charge and Discharge Circuit (CDC), and Voltage Window Comparator (VWC) are major subcircuits. Regarding CG,

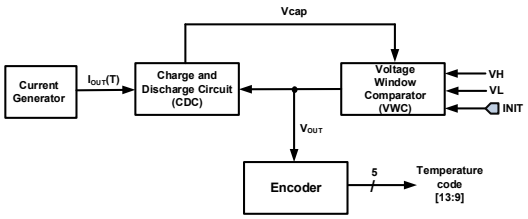

Fig. 3. Proposed temperature sensor

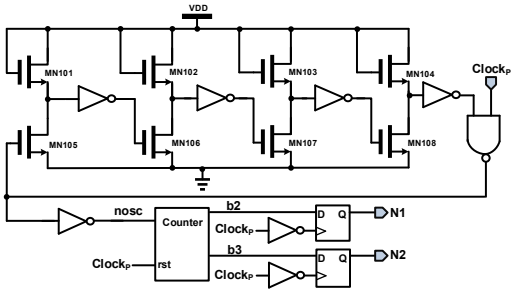

Fig. 4. N-device variation detector

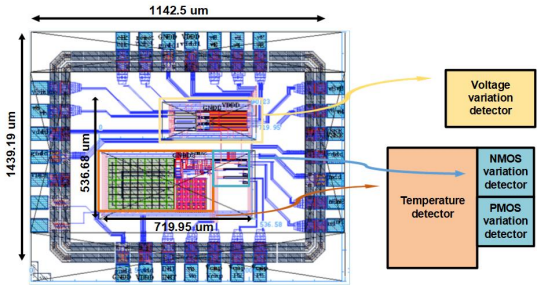

Fig. 5. Layout of the proposed design

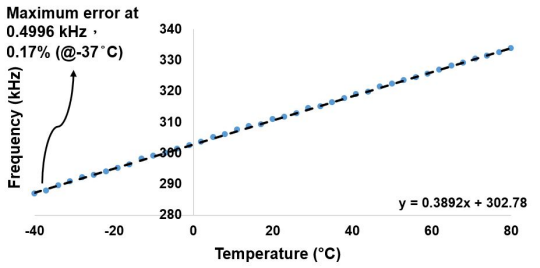

Fig. 6. Temperature sensing curve by post-layout simulations

CDC and VWC in Fig. 3, they are similar to those corresponding circuits in our previous work [2].

C. Process variation sensors

Two individual process variation detectors are required for P- and N- devices, respectively, so as to find out all the possible process corners. Referring to the N-type process variation detector in Fig. 4, $clock_P$ is coupled from the system clock source to an NAND gate to trigger the ring oscillator composed of N-device-only delay stages. Different pulse counts are attained at the counter output given that N devices are at F (fast), T (typical), S (slow) corners, respectively. Similarly, the differentiation of P device corners is also attained by similar circuit design except that all the N devices are replaced with P devices in the ring oscillator.

III. Simulation and Analysis

The proposed all-PVT-corner sensor design is realized using TSMC 180-nm CMOS process, where the layout of chip area is $1142.5 \times 1439.19\ \mu m^2$ is shown in Fig. 5. Due to the page limitation, only various temperature simulations are shown to conclude that the high linearity of the proposed sensor as shown in Fig. 6. So are the results of voltage and process corner sensing in the all-PVT-corner post-layout simulations.

To justify the performance of our design, a few prior on-chip PVT sensors with ours are tabulated in Table I. A fair FOM (figure of merit) is formulated in Eqn. (1). Apparently, our design attains the best FOM.

$$\text{FOM} = \frac{\text{Process\#}}{(\text{Volt. Resol.}(\%)\ ) \cdot (\text{Temp. Err.}(\%))} \qquad (1)$$

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TABLE I
PERFORMANCE COMPARISON WITH PRIOR PVT SENSORS BASED ON SIMULTION RESULTS

	[1]	[5]	[4]	[3]	ours
Year	2010	2014	2018	2020	2021
Process	65 nm	16 nm	65 nm	90 nm	180 nm
VDD (V)	0.3-1.0	0.7	0.45	1.2	3.3
Resol. (mV)	50 (5%)	4 N/A	N/A N/A	60 (5%)	16.5 (0.5%)
Range (^{o}C)	0 $\sim$ 100	-10 $\sim$ +90	-20 $\sim$ +80	0 $\sim$ 100	-40 $\sim$ +80
Err. (^{o}C)	$\pm$0.8	$\pm$1.0	$\pm$0.23	N/A	$\pm$0.5
Process#	3	1	1	5 (all)	5 (all)
Power	3.7 uW	70 uW	11.2 nW	2.22 mW	48.5 mW
FOM	0.75	0.37	N/A	N/A	23.81