A 12-bit 100-Msps DAC with 75.3 dB SFDR Using Randomized Biasing Current Source Selection for Real-time FOG Systems

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***Abstract*—In this investigation, a randomized current source selection approach to reduce the current mismatch for a 12-bit current steering DAC (digital to analog converter) particularly designed for the applications in FOG (fiber optic gyroscope) systems is demonstrated with TSMC 40 nm CMOS technology. The proposed randomized selection and mismatch reduction approach takes advantage of a near wide-bandwidth white noise generator to generate an unpredictable seed for digital PRNG (pseudo-random number generator) such that the correlation of the selected current sources between adjacent conversions is drastically reduced. Not only is the mismatch of current sources reduced, the dynamic performance, namely SFDR (spur-free dynamic range), is improved. Besides, RTZ (return to zero) is carried out by individual single logic gates to reduce the delay as well as the chip area. Based on post-layout simulations, the conversion rate is over 100 Mbps, 32.81 mW at 0.9 V supply voltage. INL and DNL are 1.940 and 0.080, respectively. Most important of all, SFDR is found to be 76.80 dBc at f_{in} = 10MHz, which is 1/10 of the system clock rate, to attain over 11 bits of ENOB (effective number of bits).**

Keywords—digital to analog converter, current steering, current mismatch reduction, return to zero, random number generator

I. INTRODUCTION

In the recent research for fiber optic gyroscope (FOG) systems, it can be completely solid-state fabricated, which is typically considered low cost, small size, long operation time, and high yield thanks to low manufacturing complexity compared to ring laser gyroscope (RLG) [1]. In FOG systems, two beams from a laser are splitted and injected into the same fiber but in opposite directions, namely clockwise vs. anticlockwise. Due to the Sagnac effect, the beam traveling against the rotation experiences a slightly shorter path delay than the other beam. The path delay is then converted into a phase shift denoting the angel of rotation. Unlike the classic spinning-mass gyroscope or resonant/mechanical gyroscopes, FOGs have no moving parts and no inertial resistance so that the consecutive samples are almost free from noise and other interferences. This feature leads to high similarity or correlation between two consecutive samples to be converted on both sides. The phase shift difference caused by the Sagnac effect is calculated by the system shown in Fig. 1.

As a matter of fact, it is also the baseband integrated circuit of the entire FOG. SAR-ADC receives the amplified and downconverted signal generated by the photo detector, and converts into digital code coupled to "Logic Core" which carries out the computation tasks. Logic core, on the other way around, will trigger the adaptive reset if necessary. The feature of the input voltage signal of FOG generated by photo detector is demonstrated in Fig. 2, where it is like a impulse train.

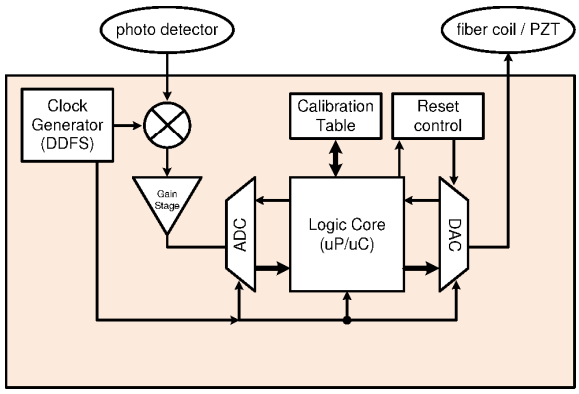

Fig. 1. Diagram of FOG baseband system

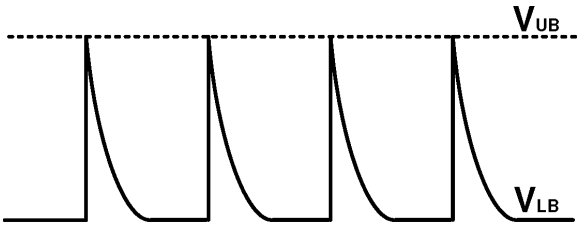

Fig. 2. Typical waveform generated by FOG's photo detectors

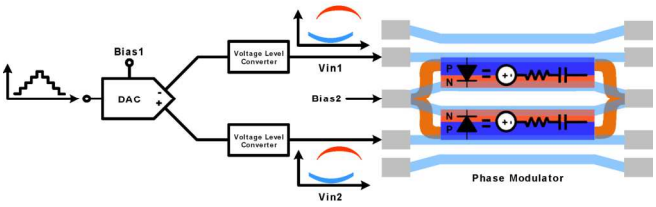

Fig. 3. Positioning of DAC in FOG systems

Although many researchers have paid attention to the design the required high speed ADCs, e.g., [2], [3], etc., for optoelectro real-time applications, the DAC (digital to analog converter) in Fig. 1 is another critical but long-ignored component. DAC is in charge of the feedback control of phase modulators so that high precision and high speed of phase detection are a must. Another feature required by the integration with other FOG discretes is that the DAC has to be a differential signal processing with the load of voltage

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level converters which carry out the amplification and translation of converted output, as shown in Fig. 3. Although many DACs were reported [4], [5], [6], none of these designs were designed for FOG systems or related real-time applications.

II. 12-BIT DAC DESIGN FOR FOG SYSTEMS

Referring to Fig. 4, the proposed DAC mainly consists of 4 groups of current arrays, namely I_{MSB}, I_{ULSB}, I_{LSB}, I_{LLSB}, where each of this current array group convert digital codes, B_{11},B_{10},B_9,…,B_2,B_1,B_0, respectively. R_L's stand for the following voltage level converters. Each group has a DEM Coder (dynamic element matching coder), a DEMRTZ Control circuit (RTZ = return to zero), and 7 individual current sources with corresponding Switch Driver. The proposed DAC is featured with randomized current source selection to auto-cancel mismatch among current sources.

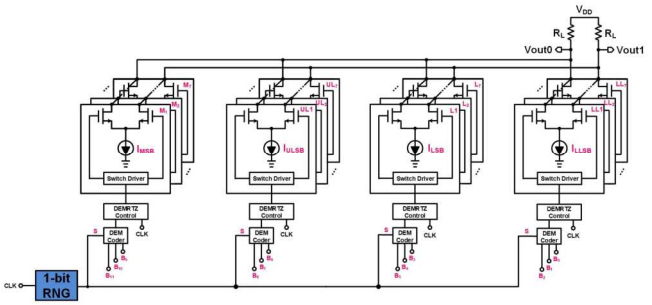

Fig. 4. Block diagram of the proposed DAC in FOG systems

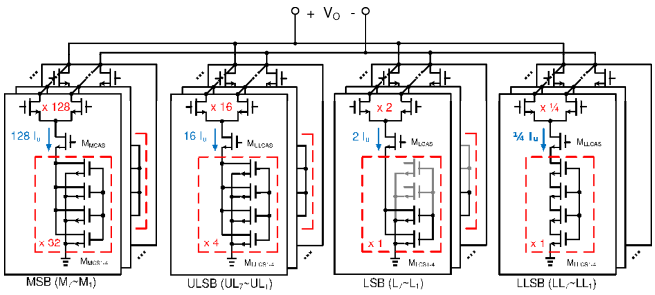

Fig. 5. Current source array

A. Current source array

The schematic details of the current array clocks in Fig. 4 are disclosed in Fig. 5. The stacked transistors, namely M_{MCAS}, M_{ULCAS}, M_{LCAS}, M_{LLCAS}, are needed to enhance the output impedance so that the gain will be boosted. The pulldown NMOS in each block is split into 4 stacked transistors, namely, M_{MCAS1}-M_{MCAS4}, M_{ULCAS1}-M_{ULCAS4}, M_{LCAS1}-M_{LCAS4}, M_{LLCAS1}-M_{LLCAS4}, is due to the prevention of layout mismatch caused by over-etching during manufacturing. Notably, the aspect ratio of these 4 current arrays are design to be 128:16:2: 1/4 to cover the entire range of 12 bits.

B. Switch driver

Referring to Fig. 4 again, Switch Drivers are needed in each current array block to synchronize the inputs to every block. The necessity of input synchronization is caused by the delay mismatch of the respective DEM coder and inverters in the path of each block. More specifically, the delay mismatch of different paths will lead to a possible scenario that the falling edge and rising edge of digital signal therewith are not correctly switched at 1/2VDD. By contrast, Switch Driver shown in Fig. 6 takes advantage of cross-coupled latch as well as a back-to-back inverter pair to ensure the switchings of both edges are higher than 1/2VDD simultaneously.

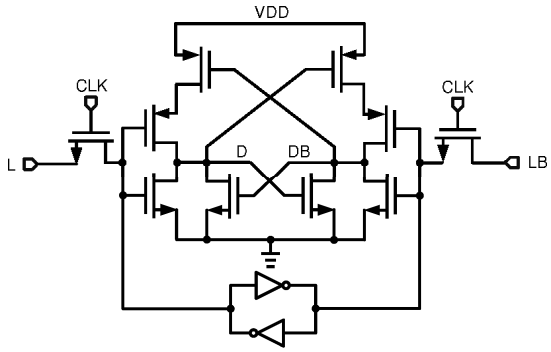

Fig. 6. Switch Driver circuit

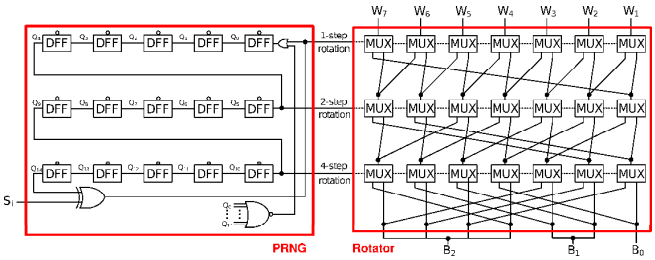

Fig. 7. Schematic of DEM Coder

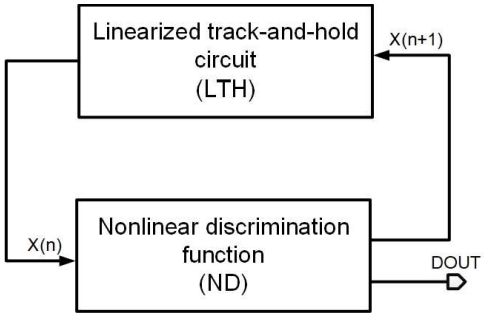

Fig. 8. Block diagram of 1-bit RNG

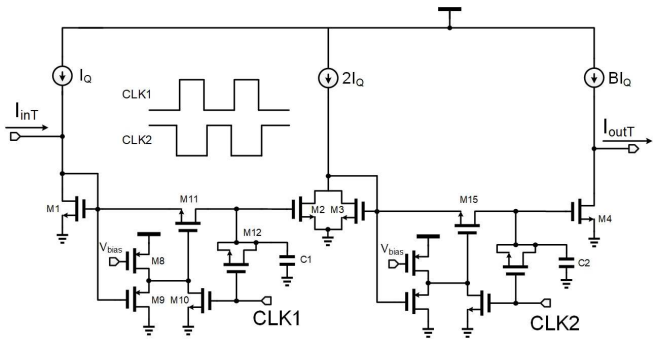

Fig. 9. LTH circuit (linearized track-and-hold circuit)

C. DEM Coder and logic control

One of the biggest reasons that conventional current-steering DACs cannot attains high SFDR is the mismatch of current sources. However, the variations cause by manufacturing are unavoidable so that a strategy scrambling selection of current sources is used in this design. Referring to Fig. 7, the PRNG (pseudo-random number generator) at the left-hand side randomly generates 3 selection signals coupled to the Rotator at the right-hand side such that each group of B_2,B_1,B_0 will not select the same combination of the

current arrays every time. Thus, the mismatch will be equalized in each DAC conversion.

D. 1-bit RNG

With reference to Fig. 8, it is a modified design of the 3-bit RNG disclosed in [11]. The theory of the random number generation is based on DTC (discrete time chaos) as follows.

$$X(n+1) = B \cdot X(n) - A \cdot \mathrm{sgn}(X(n))$$
$$X(0) = A/(B\text{-}1) \quad (1)$$

where $X(\cdot)$ is the generated sequence, A and B are floating numbers. B determines the dynamic range within [1,2] to ensure that $X(n)$ will be in the range of [$-A$, $+A$]. The schematic design of LTH ((linearized track-and-hold circuit) in Fig. 8 is shown in Fig. 9. I_{outT} is B times of I_{inT} . I_Q is set to 10 µA in this design. The aspect ratio of M1, M2, M3, M4 is 1:1:1:2. Two non-overlapping clocks are needed for CLK1 and CLK2. A linearized sampling switch is composed of M8, M9, M10, M11, and M12, where M9 is employed to stabilize the gate drive of M11 to prevent channel conductance input-dependent variation and charge injection effect.

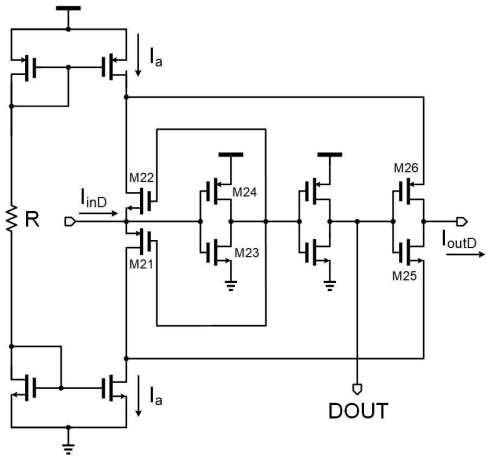

Fig. 10. ND circuit (nonlinear discrimination circuit)

The ND circuit (nonlinear discrimination circuit) in Fig. 8 is in charge of carrying out the function of sgn(·) in Eqn. 1. The detailed schematic of the ND circuit is shown in Fig. 10, where I_{inD} and I_{outD} are coupled to I_{outT} and I_{inT}, respectively, to form a loop. One of the following functions will be proceeded.

- If I_{inD} is positive, M21 and M23 on, M22 off to generate $DOUT = 1$. M25 is on to force $I_{inD} - I_a$.
- If I_{inD} is negative, M22 and M24 on, M21 off to generate DOUT = 0. M26 is on to force $I_{inD} + I_a$.

III. Simulation and Verification

The proposed buffer design is realized by TSMC 40 nm CMOS process. Fig. 11 shows the layout of the proposed design, where the chip area is 654◊711 µm^2 and the core area is 123◊124 µm^2.

Referring to Fig. 12 and 13, SFDR of the proposed DAC's outputs is demonstrated given that $B_0B_1\ldots B_{11}$ is scanned from 00…0 to 11…1 (12 bits). Thus, the conversion functionality as well as the ENOB are ensured.

Table I summarizes the comparison of our work with several prior 12-bit DAC works. Apparently, the proposed design provides the only solution for 100 MHz by taking advantage of advanced CMOS process as well as the proposed mismatch auto-cancelling design methods. Notably, the proposed design attains the best FOM among all the DACs in the table.

$$\mathrm{FOM} = \frac{2^{\frac{SFDR-1.76}{6.02}} \times f_s}{\mathrm{Area}} \times 10^{-6} \quad (2)$$

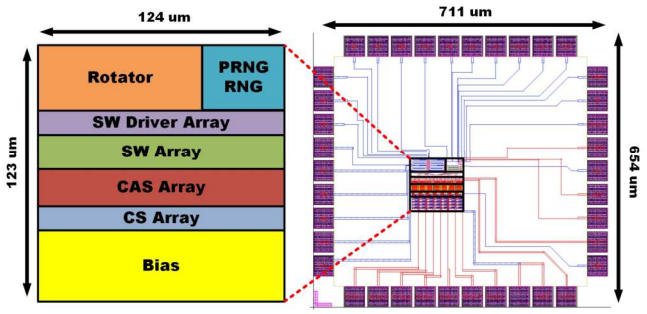

Fig. 11. Layout of the proposed DAC design

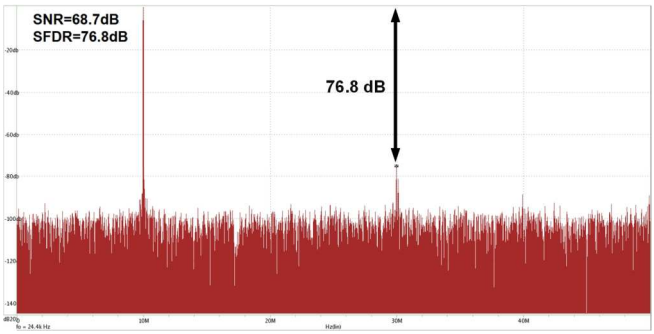

Fig. 12. SFDR performance of the proposed DAC at 10 MHz

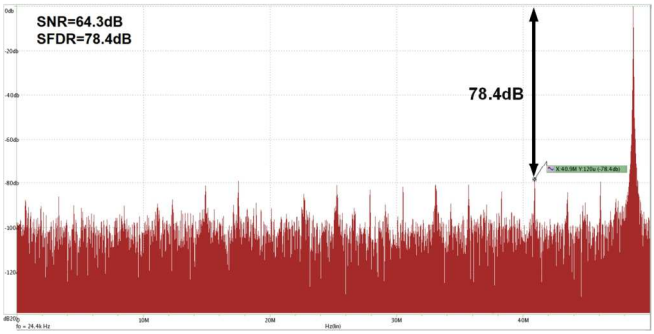

Fig. 13. SFDR performance of the proposed DAC at 48.7 MHz

IV. Conclusion

The proposed 12-bit DAC design featured with scrambled current array selection to reduce current source mismatch is proved to attain 76.84 dB at 1/10 of the system clock. The scrambling is carried out using a 4-bit random number generator to drive DEM Coder. The simulated SFDR performance validates over 11-bit ENOB.

Acknowledgment

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(Nation Applied Research Laboratories), Taiwan, for the assistance of EDA tool support and chip fabrication.

TABLE I. PERFORMANCE COMPARISON OF OUTPUT BUFFERS

	[7] 1998	[8] 2009	[9] 2003	[10]** 2018	[12] 2011	[13] 2012	[14] 2012	[15] 2015	[16] 2018	This work
Process (nm)	600	500	350	350	180	90	180	65	130	40
Bits	12	12	12	12	12	12	10	14	12	12
Verification	Simu.	Meas.	Simu.	Meas.	Simu.	Meas.	Meas.	Simu.	Meas.	Simu.
VDD (V)	3.3	5.0*	3.3	3.2	3.3/1.8	2.5/1.2	1.8	2.5/1.2	1.5/1.2	0.9
INL (LSB)	0.8	0.98	N/A	1.51	0.4	0.4	N/A	N/A	N/A	1.94
DNL (LSB)	0.2	0.87	N/A	0.49	0.5	0.3	N/A	N/A	N/A	0.08
SFDR (dB)	N/A	N/A	65	N/A	76	73.6	61	80	62.1	75.3
Sampling (MHz)	65	1.0	53	N/A	500	400	500	1000	100	100
Power (mW)	71.7	0.5*	N/A	0.46***	205	92	24	N/A	18	32.81
Area (mm2)	N/A	0.0864	1.782	0.0465	1.44	0.18	0.034	0.48	0.21	0.015
FOM	N/A	N/A	0.04	N/A	1.7	8.7	13	17	4.9	31

* estimated, **RR DAC, ***only buffers

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