A 100 MHz 9.14-mW 8-Bit Shift Register Using Double-Edge Triggered Flip-Flop*

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***Abstract*—Double-edge triggered flip-flops (DETFF) project a solution to clock power reduction by lowering the clock frequency and maintains the same data rate. Hence, they are appropriate to be used as shift registers. This paper has reviewed several earlier designs of double-edge triggered flip-flops and presented an 8-bit low power shift register by using a newly designed DETFF. The major contribution of this work takes advantage of two parallel data paths that work in opposite phases of the single clock without an inverted input trigger. The proposed shift register design is realized using a typical 90-nm CMOS process. The post-layout results show that the proposed shift register reduces the power consumption by at least 17.2%.**

***Index Terms*—DETFF, shift register, short delay, layout, power delay product (PDP).**

I. Introduction

Nowadays, every IC designer aims to reduce power consumption and decrease the size of electronics to reduce the cost of manufacturing. Each module of a digital system required appropriate design for the lowest possible power to keep pace with the scaling of technology, a single-chip integrated by billions of transistors using nano-scale CMOS processes [1][2].

There are several ways to implement a double-edge triggered flip-flop; one method is to insert an additional circuit (XOR with delay) to generate internal pulse signals on each clock edge [3][7]. The second method is to duplicate the pathway to enable the flip-flop to sample data on every clock edge [10]. Double edge triggering or latching is also widely used in pipelining designs to reduce the sequencing overhead [11][12].

For the two-way data path method, there are many existing designs such as using transmission gate logic, pass transistor logic, etc. Johnson *et al.* developed a static double-edge triggered flip-flop in which, kept the same transistor count as the conventional transmission gate based single edge-triggered flip-flop (SETFF) and reduced the operating frequency by half when compared to the SETFF for fixed data throughput but least concentrated on reducing power consumption [5]. Hossain *et al.* has indicated that double-edge triggered flip-flops are capable of significant energy savings, for only a small overhead in complexity than SET flip-flops [4]. Tyagi *et al.* designs an LFSR which works on positive feedback source coupled logic which tries to reduce the power consumption [13]. When comes to delay reduction, the circuit doesn't meet the expected result because it follows the single edge triggering technique. Sung *et al.* designed a low power DETFF using the clock gating technique which uses a lower swing [6]. However, methods using multi-Vth suffer from the problem that low-Vth transistors occupy a larger area than the normal transistors and subthreshold current is increased.

The built-in self-test (BIST) is widely used for testing any VLSI circuits as it provides a larger range of low power applications. Praveen *et. al* developed a reversible linear phase shift register (8-bit) that resulted in a 10% power reduction to the conventional LFSR [8]. Abhilash *et. al* proposed an LFSR (8-bit) using a weighted random test pattern generator to improve the total performance that results good in the reduction of time-delay but ends in higher power consumption [9]. To resolve all the mentioned issues, this research work represents an 8-bit shift register using a DETFF to reduce both the delay and power consumption.

II. Design and Implementation

Figure 1 shows the schematic design of the 1-bit double-edge triggered flip-flop described in [10] composed of six pass transistors, two latches, and an output keeper circuit. Among them, the latches are respectively constructed by the back-to-back configuration of inverters I11 and I12 and inverters

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I13 and I14. The whole setup looks complicated and must go through a long way to reach the output, Q which results in consuming more power. The inverter latches, I11-I12, and I13-I14, when replaced with the same keeper circuit used at the output side also result in the same functionality.

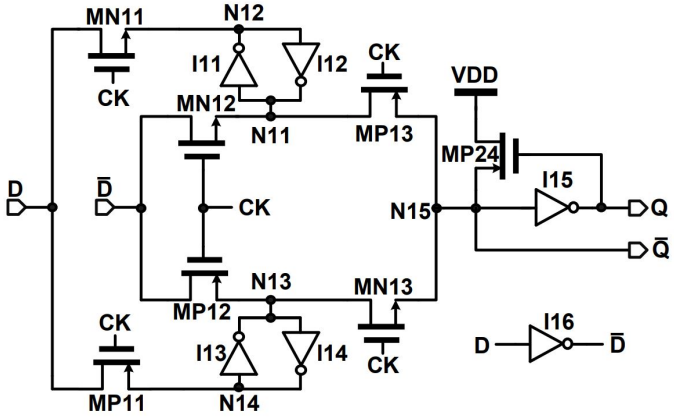

Fig. 1. DETFF in [10]

A. Proposed Low-Power DETFF

The proposed design in Figure 2 is enhanced by removing the inverted input trigger and the following MN12 and MP12 transistors. All these new devices don't affect the functionality of the flip-flop, but also reduces the number of transistors that results in a lower core area, so as reduces the price to pay and power consumption.

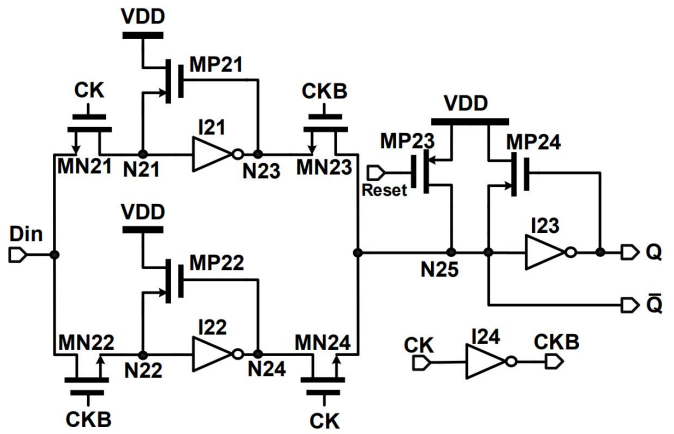

Fig. 2. Proposed DETFF of this work

By considering the following factors, the proposed design is enhanced:

- In the previous design (Fig. 1.), at node N11, there are two gate capacitance (MN12, MP13) and two diffusion capacitance (I11, I12), whereas in the proposed design (Fig. 2.), at node N23, there are two gate capacitance (MN21, MP21) and only one diffusion capacitance (I21). Hence, the load at the node N23 becomes less so as the charging and discharging time decreases which results in less power and energy consumption. In digital CMOS circuits, the switching power is defined as:

$$P_{sw} \propto f.\ C.\ V^2 \tag{1}$$

where P_{sw} is switching power, C is capacitance, V is power supply, and f is frequency. Assuming f and V are the same for both designs, the power at the nodes N11 and N23 can be expressed as:

$$P_{N11} \propto 2C_g + 2C_{diff} \tag{2}$$

$$P_{N23} \propto 2C_g + C_{diff} \tag{3}$$

where C_g is the gate capacitance (0.4 nF) and C_{diff} is the diffusion capacitance (0.25 nF), whose ratio is 8:5, respectively. TSMC 0.18-μm 1P6M CMOS process is considered as an illustrative example. By mathematical calculations, it is conclusive that P_{N11} is 1.2 times greater than P_{N23}. The same amount of power is consumed at the nodes, N13 and N24 in the opposite phase of the clock.
- Since the number of devices used in this design is less than the design in Fig. 1, the wiring of the clock line decreases so as power consumption of clock reduces.

Hence, these factors conclude that the proposed design consumes low power when implemented.

B. Circuit Analysis

As discussed above, the proposed design is a dual-path model that follows the dual pathway to enable the flip-flop to sample data on every clock edge. When the clock signal CK is at logic high, the transistors MN21 and MN24 are turned on where the transistors MN22 and MN23 are turned off. The input Din passes through MN21 and then the signal is flipped by the inverter, I21. This signal is stored at node N23 until the clock becomes logic low. However, for the next half clock cycle, the CKB becomes logic high and MN23 opens. So, the previously stored signal at N23 passes through MN23 and flipped by the inverter I23 and gives the output Q with respect to the reset. On the other hand, when the clock is logic low the input signal passes through the transistor MN22, and the same process is continued as the first path. If there is any voltage swing when the signals go through several devices, the regenerative transistors (MP21, MP22, and MP24) which are associated with the power supply are helpful to boost the signal. Through this continuous process, the output Q is observed at every edge of the clock. Therefore, when the clock makes an inverse transition, the role of the upper pathway and the lower pathway is exchanged, exhibiting alternative sampling, and transferring behavior.

The enhanced DETFF has been assembled into a shift register which is operated using the same clock and the reset as shown in Figure 3, in which the power consumption and time delay have been tested using the HSPICE Cadence Virtuoso Tool.

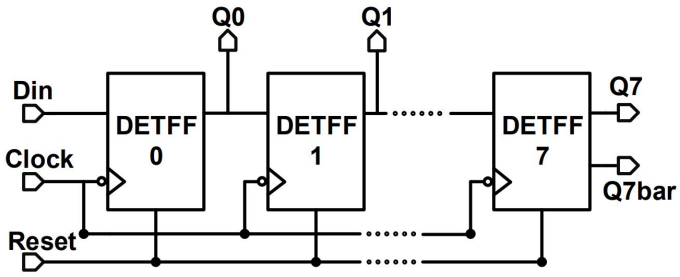

Fig. 3. Block diagram of proposed 8-bit shift register using DETFF

III. Simulations and Discussion

The proposed 8-bit shift register design is implemented using TSMC mixed-signal/RF 1P9M low-power 90-nm CMOS process with ultra-thick (34 kA) top metal options. Figure 4 and Figure 5 shows the schematic and layout (including the floor plan) of the full chip, respectively, where the chip area is 966 x 966 μm^2 and the active area is 215.8 x 162.5 μm^2. The proposed circuit has been simulated at several clock frequencies and maintained a correct functionality above 500 MHz. The operating frequency can be increased by accurate scaling of the transistors. Fig. 6 and fig. 7 demonstrates the layout of proposed 8-bit shift register and pre-layout simulation result respectively.

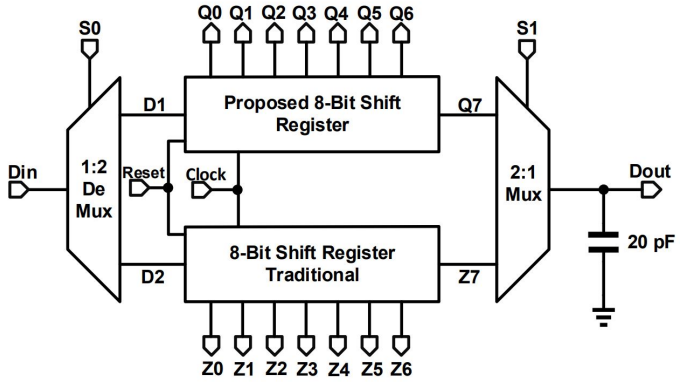

Fig. 4. Schematic of the chip

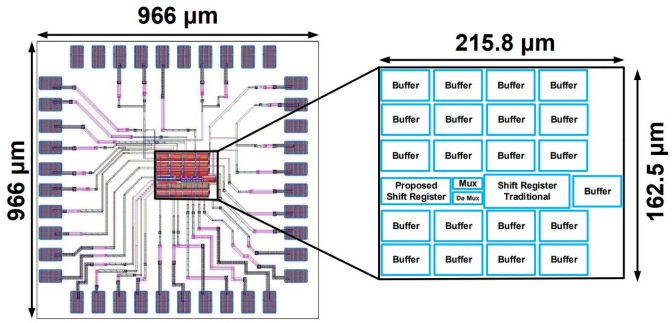

Fig. 5. Full chip layout with floorplan

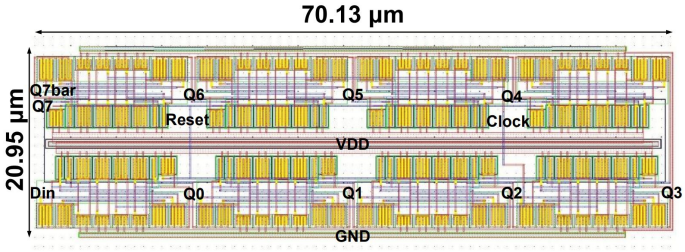

Fig. 6. Layout of proposed 8-bit shift register using DETFF

As per the reliability concern, the proposed design has undergone the all-PVT-corner simulation whose process corners are SS, TT, FF, FS, and SF. The power supply is 1 V with a variation of 10% i.e., 0.9 V and 1.1 V. The Temperature corners are 0^0, 25^0, and 75^0. The post-layout simulations (including all PVT corners) of the 8-bit shift register which is realized using HSPICE offline simulation are observed in fig 8.

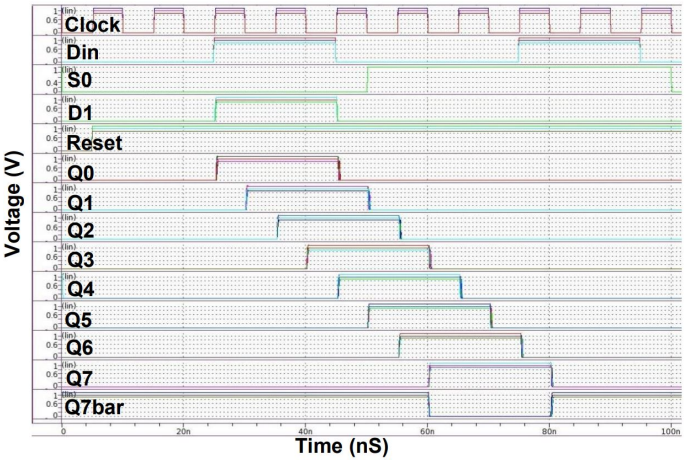

Fig. 7. Pre-layout simulation of 8-bit shift register using DETFF

Table 1 gives the performance comparison with several prior works. Notably, measurement requires to drive 20 pF because of the need to drive large loads. 20 pF load is chosen as a common parameter for a justified comparison [8][9]. FOM is needed to compare all the prior works to find the superiority. The following equation states that:

$$FOM(Figure\ of\ Merit) = \frac{Power*Delay}{Load*Frequency*Bits}$$

Also, the normalized power and the normalized delay are calculated according to the following equations, respectively:

$$Normalized\ Power = \frac{Power}{VDD^2}\ ,$$

$$Normalized\ Delay = \frac{Delay}{Process^2}$$

Although our work attains the second-best FOM right after the work presented in 2018 [10], the proposed 8-bit shift register is superior in terms of no. of bits and better in

TABLE I
COMPARISON WITH PRIOR WORK

	IJCSIT 2018 [10]	**ICCTICT *2016 [13]***	**APCCAS *2006 [3]***	***WCSE 2018 [7]***	***ICISC 2017 [8]***	***ICISS 2019 [9]***	***This Work [2020]***
Process (nm)	180	180	180	180	180	180	90
Simul.	Pre	Pre	Meas.	Post	Pre	Pre	Post
VDD (V)	1.8	1.8	1.5	1.8	N/A	N/A	1
Delay (nS)	0.251	0.573	0.375	2.2	2.32	0.775	1.5
Power (mW)	0.028	2.015	0.0317	35.25	37.2	71	9.14
PDP(pJ)	0.0072	1.154	0.011	78.18	86.4	55	13.71
Frequency (MHz)	500	100	10	125	100	10	100
Bits	1	4	1	8	8	8	8
Normalized Delay (fS)	7.74	17.6	10.648	67.9	71.6	23.91	0.185
Normalized Power (mW)	0.00867	0.621	0.0097	10.86	N/A	N/A	9.14
Load (pF)	0.025	0.05	0.1	20	N/A	N/A	20
FOMx10^{-10}	5.76	577K	110	38.775	53.94	343.9	8.56

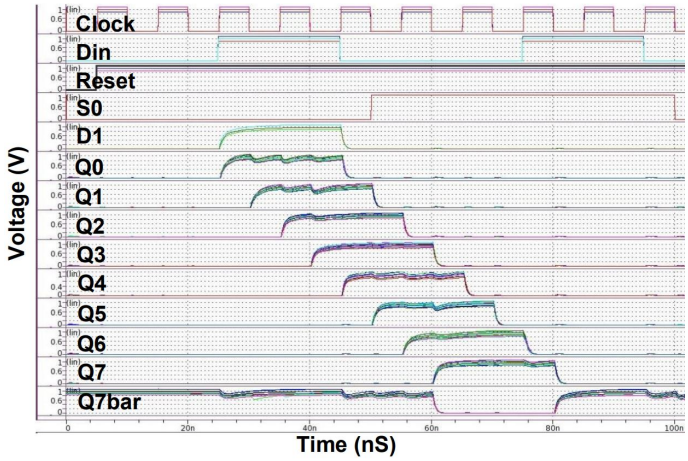

Fig. 8. Post-layout simulation of 8-bit shift register using DETFF

normalized time delay. These results assess that the power delay product (PDP) does pretty well when compared to the prior works. The normalized power is reduced by 17.2% when compared with the previous work presented in 2018 [7]. The normalized power of the research works, [10], [13], and [3] is very less because of the small output load and less number of bits, but when it comes to FOM comparison, the proposed work beats them with a large scale.

IV. Conclusion

In this work, an 8-bit low power consuming shift register is designed using double-edge triggered flip-flops for low power and high-performance digital system applications which has an advantage of reducing glitches in the observed output at high loads. The future of this design can be modified by interchanging suitable MOS with low Vth transistors to reduce active area or speed up the operation including the power reduction and also using a better CMOS process.

Acknowledgement

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References

[1] S. Kukrety, G. Singh and V. Sulochana, "A low power 32-bit CMOS ROM using a novel ATD circuit," *Int. Journal of Electrical and Computer Eng. (IJECE),* vol. 3, no. 4, pp. 509-515, Aug. 2013.

[2] R. Sharma and B. Singh, "Design and analysis of linear feedback shift register (LFSR) using gate diffusion input (GDI) technique," in *Proc. IEEE Conf. of Wireless Networks and Embedded System (WECON)*, pp. 1-5, Oct. 2016.

[3] C.-C. Wang, G.-N. Sung, M.-K. Chang, Y.-Y. Shen, "Energy-efficient double-edge triggered flip-flop," in *Proc. IEEE Asia Pacific Conf. on Circuits and Systems (APCCAS)*, pp. 127, Dec. 2006.

[4] R. Hossain, L. D. Wronski and A. Albicki, "Low power design using dual edge triggered flipflops," in *Proc. IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 2, pp. 261-265, Jun. 1994.

[5] T. A. Johnson and I. S. Kourtev, "A single latch, high speed double-edge triggered flip-flop (DETFF)," in *Proc. Int. Conf. on Electronics, Circuits and Systems IEEE*, pp. 189-192, Jan. 2001.

[6] Y.-Y. Sung and R.-C. Chang, "A novel CMOS double-edge triggered flip-flop for low-power application," in *Proc. IEEE Inter. Symp. on Circuits and Systems*, pp: II-665, vol. 2, May 2004.

[7] A. Baskoro, O. Setyawati, P. Siwindarto and C.-C. Wang,"Low-Power High-Speed 8-Bit Shift Register Using Double-Edge Triggered Flip-Flops," in *Proc. 8th Int. Workshop on Computer Science and Engineering (WCSE)*, pp. 151, Jun. 2018.

[8] Y. G. Praveen Kumar, B. S. Kariyappa and M. Z. Kurian, "Implementation of power efficient 8-bit reversible linear feedback shift register for BIST," in *Proc. Int. Conf. on Inventive Systems and Control (ICISC)*, pp. 1-5. Jan. 2017.

[9] A. Bagalkoti, S. B. Shirol, S. Rama Krishna, P. Kumar and R. B. S, "Design and implementation of 8-bit LFSR, bit-swapping LFSR and weighted random test pattern generator: A performance improvement," in *Proc. Int. Conf. on Intelligent Sustainable Systems (ICISS)*, pp. 82-86, Feb. 2019.

[10] C.-C. Yu and C.-C. Tsai, "Dual edge-triggered d-type flip-flop with low power consumption," *Int. Journal of Computer Science and Information Technology (IJCSIT)*, vol 10, no. 5, pp. 1-12, Oct. 2018.

[11] C.-C. Wang, C.-J. Huang and K.-C. Tsai, "A 1.0 GHz 0.6-μm 8-bit carry look ahead adder using PLA-styled all N-transistor logic," in *Proc. IEEE Trans. of Circuits and Systems, Part II: Analog and Digital Signal Processing,* vol. 47(2), pp. 133–135, Feb. 2000.

[12] C.-C. Wang, C.-F. Wu and K.-C. Tsai, "A 1.0 GHz 64-bit high-speed comparator using ANT dynamic logic with two-phase clocking," in *Proc. IEEE Trans. on Computers and Digital Techniques*, vol. 145(6), pp. 433–436, Nov. 1998.

[13] A. Tyagi, N. Pandey, K. Gupta, "PFSCL based linear feedback shift register," in *Proc. Int. Conf. on Computational Techniques in Information and Communication Technologies (ICCTICT)*, pp. 580-585, March 2016.