67.5-fJ Per Access 1-kb SRAM Using 40-nm Logic CMOS Process*

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***Abstract*—A very low energy -consuming SRAM design based on single-ended cells is demonstrated in this work. To resolve poor SNM (static noise margin) of prior single-ended memory cells, the porposed SRAM cell is equipped with a pull-up PMOS and a high-Vthn NMOS foot switch such that the cell state is not bothered by noise when the suppy voltage is getting lowered. Moreover, a PFOS (Positive Feedback Op-Amp Sensing) circuit is added between bitlines ($\overline{\text{BL}}$, BL) to reduce the read delay and generate full-swing output. Last but not least, a voltage mode select (VMS) circuit is added to each column to reduce the static power of unselected cells such that idle power is drastically reduced. The reason is that the a lower voltage able to keep the state of bits is applied to those unselected cells. Not only are detailed description and all-PVT-corner simulations provided to predict the low power performance, a 1-kb SRAM design based on the proposed cells with BIST (build-in self test) circuit is realized using typical 40-nm CMOS technology. The worst energy/access and energy/bit are found to be 67.5 fJ, and 2.1 fJ, respectively.**

***Index Terms*—SRAM, single-ended cell, SNM, positive feedback op-amp sensing, voltage mode select**

I. Introduction

According to the recent report predicted by ITRS, the overall area of memory devices in an SOC (system on chip) will occupy over 90% of the entire chip area very soon. Low-power memory devices will then dominate the overall power consumption of these products, particularly battery-operated ones [1]. SRAM has been widely used as caches in various processors, e.g., CPU, AP, etc. The SRAM power reduction certainly propels the advacne of these processors. Though many SRAMs have been proposed to achieve low power operations, the generic loadless SRAM cell was condidered to attain the edge of small area and low power [2]. However, the loadless cell is bothered by the potential weak "0" state such that it is always under the threat of read/write disturbance and instability, particularly it is used in single-ended bitline structure. This issue also results in SNM (static noise margin) degradation therewith [3]. Many auxiliary circuits were reported to resolve these problems, including readout assit circut [4], write assist circuit [5] [6], etc. Besides, when the SRAM technology evolves toward nano-scale, leakage becomes the imminent problem for power reduction [7]. Only a few SRAM designs, however, were meant to carry out leakage detection and compensation . In brief, none of the mentioned reports showed a comprehensive result to reduce the power, reject the coupled noise, fasten access speed, and increase SNM at the same time.

To resolve all the issues in single-ended SRAM designs, many circuit features are proposed to reduce power and enhance performance simultaneously different aspects, including cell circuit, bitline architecture, and power supply mode selection. More specifically, the porposed SRAM cell is equipped with a pull-up PMOS and a high-Vthn NMOS foot switch to assist the R/W if selected, and gound the stored state, respectively. Consequently, the SNM is drastically increased. Regarding the read speed, a (Positive Feedback Op-Amp Sensing) circuit is added between bitlines ($\overline{\text{BL}}$, BL) to reduce the delay. To reduce power dissipation, a supply voltage select mode is added to every column of SRAMs, where the supply votlaged of the column unselected is reduced to save idle power. The proposed SRAM with 1-kb cells is realized using typical 40-nm logic CMOS process. All-PVT-corner post-layout simulations justifies that the worst energy/access and energy/bit are 67.5 fJ, and 2.1 fJ, respectively, which are by far the best to date.

II. Low Energy-Consuming SRAM Design

With reference to Fig. 1, the architecture of the proposed 1-kb SRAM is disclosed, where an SRAM array, a Controller circuit, a voltage mode select (VMS) circuit, AVD (adaptive voltage detector), PVB (pass-transistor gate voltage boosting), a PFOS, and a BIST (build-in self test) circuit are included. Since AVD and PVB circuits are referred to the same circuitry reported in [8], their details are note covered in the folliwing text. By contrast, the features of the proposed SRAM will be fully described.

A. 6-T SRAM cell with pull-up assist

As addressed earleir, prior single-ended SRAM designs were suffered from poor SNM, though they could reduce

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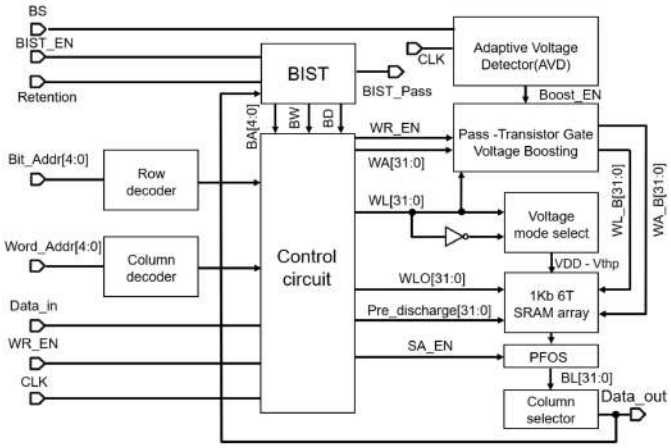

Fig. 1. Proposed low energy-consuming SRAM system diagram

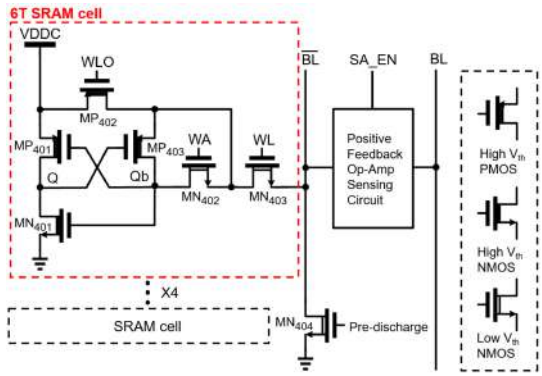

Fig. 2. Proposed 6T SRAM cell to enlarge SNM

the area and the power by saving one bitline. The major reasons are the "0" state of storage node is easily flipped by lacking a grouding path, and the P-latch becomes a resistive network when the storage node is to written with new states. Therefore, two extra devices are added as shown in Fig. 2.

• MP_{402} : It is a high Vthp PMOS driven by WLO. When the cell is written with "1", it is cut off to kill the current path from VDDC to the P-latch such that Qb can be easily flipped. If written with "0", it is turned on to supply a current to the P-latch from VDDC. That is, it becomes a pull-up assist loop.
• MN_{401} : This is a high Vthn NMOS driven by node Qb. If the state at Qb is low, it is off to keep the charge at node Q as high. By contrast, if Qb is high, MN_{401} will be on to couple Q perfectly to ground.

Apparently, thanks to the added pull-up assist by MP_{402} and grounding path by MN_{401}, the SNM of the cell shall be enlarged significantly.

B. Positive Feedback Op-Amp Sensing (PFOS)

Another hazard in prior single-ended SRAM designs is that the output swing was never ensured to be full swing, particularly when reading "0". A PFOS circuit is added bewteen $\overline{BL}$ and BL, as shown in Fig. 2, where the schematic is given in Fig. 3.

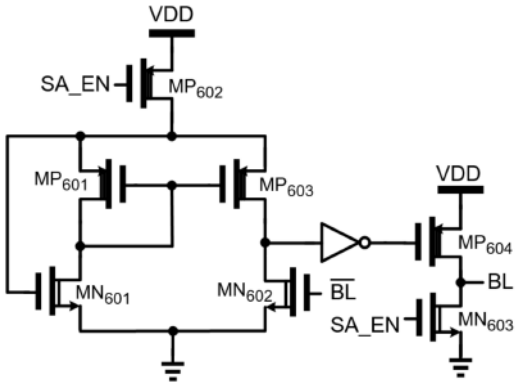

Fig. 3. Positive feedback op-amp sensing circuit

• SA_EN = 1 : MN_{603} is turned on to ground BL, while MP_{602} is cut off to deny any current injecting into the differential amplifier.
• SA_EN = 0 : MN_{603} is off. MP_{602} is turned on to drive MN_{601} from the drain of MP_{602} and the source of MP_{601}, consitituting a positive feedback path. Then, the output of the differential amplifier is pulled high to drive MP_{604} via an inverter so that BL will become high.

C. Voltage mode select (VMS)

To further reduce the standby power when the cell is not accessed, a power-gated mechanism is employed in Fig. 4, where 3 low-Vthp PMOS transistors are added to every column of memory cells.

(1). If any cell in the same column is accessed, WL is high to cut off MP_{706}. MP_{704} is turned on by WLB (low) such that the entire column is driven by the normal VDD.
(2). If no cell in the column is accessed, WL is low and WLB is high. A reduced supply voltage, VDD - Vthp, is coupled to the entire column, namely VDDC in the memory cell. Thus, the supply voltage is dropped by Vthp to save power in such an idle state.

D. R/W cycle timing

Referring to Fig. 2 and 3, read cycle operations of the proposed SRAM cell are briefed as shown inFig. 5.

• Read "1" : Pre-discharge is asserted before WL=1 to ground $\overline{BL}$. WL=WA=1 to turn on MN_{402} and MN_{403}, respectively. WLO is set to high shutting down MP_{402}. Thus, "0" at Qb will be coupled to PFOS of $\overline{BL}$ via MN_{402} and MN_{403} to raise BL high.
• Read "0" : WL=1, WA=1, WLO=0 to turn on MN_{402}, MN_{403}, MP_{402}, respectively. Due to the presence of the pull-up assit loop by turning on MP_{402}, "1" at Qb will be stable, which coupled to PFOS of $\overline{BL}$ via MN_{402} and MN_{403}

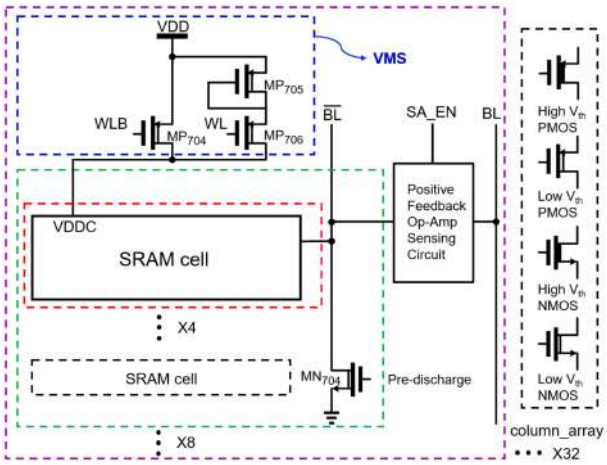

Fig. 4. Voltage mode select circuit

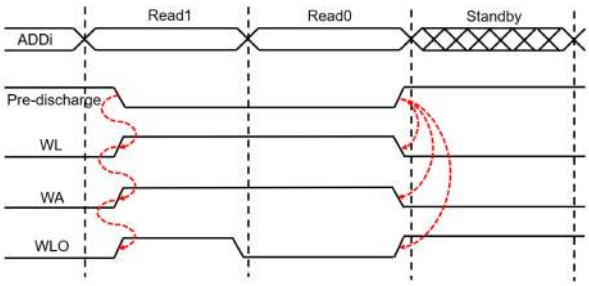

Fig. 5. Read cycle timing

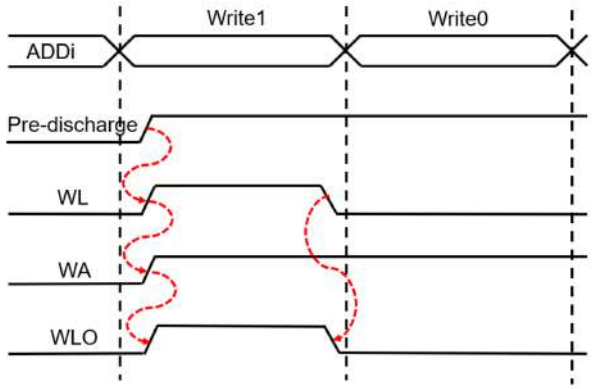

Fig. 6. Write cycle timing

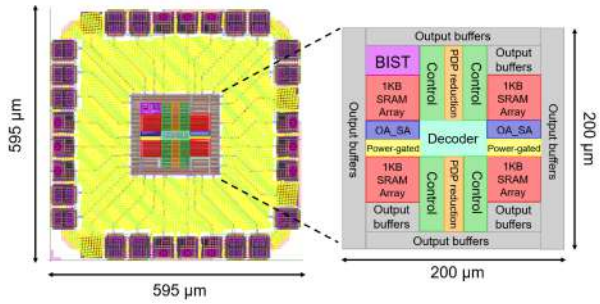

Fig. 7. Layout of the proposed 1-kb SRAM

to pull down BL.

• Standby : The SRAM enters the standby mode after Pre-discharge is unasserted.

Similarly, write cycle operations are given in Fig. 6, where the details are as follows.

• Write "1" : WL=1, WA=1, to turn on MN_{403} and MN_{402}, respectively. WLO is set high to shut off MP_{402}. Pre-discharge is asserted high to ground $\overline{BL}$. Thus, Qb is low to turn on MP_{401} and cut off MN_{401}. Q node will then be high.

• Write "0" : WL=0 to shut off MN_{403}. WA is high to turn on MN_{402}, and WLO is low to activiate the pull-up assist loop such that Qb becomes "1". Then, MN_{401} is turned on to ensure Q=0.

III. Simulation and Discussion

The proposed 1-kb SRAM featured with 6T single-ended cells is realized using TSMC 45 nm CMOS LOGIC (40G) process. The layout is demonstrated in Fig. 7, where the chip area is 595×595 μm^2, and the core ares is 200×200 μm^2

A. Post-layout simulations

To validate the advantages resulted from the features of the proposed SRAM and the cells, all-PVT-corner simulations (5 process corners, 3 VDD voltages, 5 temperatures) are carried out. Fig. 8 shows all the R/W functions, where the worst case R/W delay is 1.43 ns.

As for the noise margins, Fig. 9 and Fig. 10 showns the SNM and DNM (dynamic noise margin) of the proposed 6T SRAM cells. The SNM is enlarged to 706/377 mV, which is the best by far. Another feature is that the cell will resist any noise under 100 ps@0.3 V given VDD=0.9V and 200 MHz system clock.

B. Performance comparison

To make a fair apple-to-apple comparison between the proposed design and prior SRAMs, a few SRAMs designed

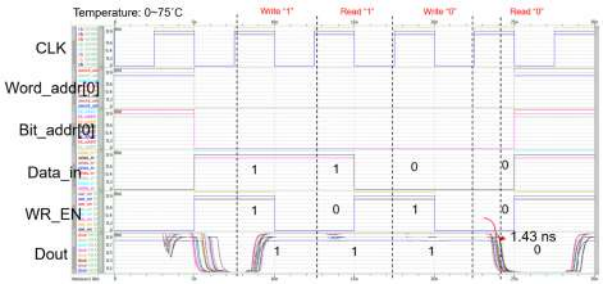

Fig. 8. All-PVT-corner post-layout simulation

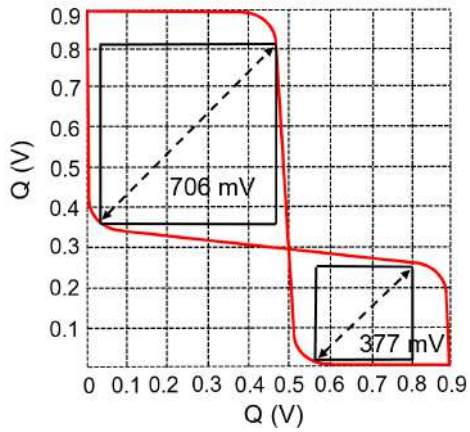

Fig. 9. SNM plot

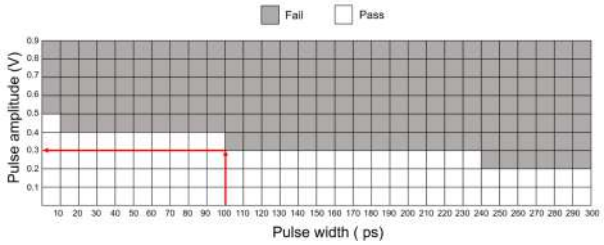

Fig. 10. DNM plot

using 40-nm CMOS process are tabulted in Table I. Notably, we also use the numbers of these works given by simulations for the sake of fairness. Apparently, the proposed 6T singl-ended SRAM attains the edge of lowest energy/access and energy/bit to date. This fact justifies that the added pull-up assist loop, VMS, and grounding foot switch indeed resolve the poor SNM and power dissipation problem.

TABLE I
PERFORMANCE COMPARISON WITH PRIOR CMOS SRAMS BASED ON SIMULTION RESULTS

	[9]	[10]	[11]	[12]	ours
Year	2012	2013	2015	2019	2020
Pub.	ISQED	ISLPED	TVLSI	TVLSI	
Cell type	8T	11T	9T	11T	6T
Cell area (μm^2)	0.6679	4.56	0.8446	1.407	0.825
Verification	Meas.	Meas.	Meas.	Post.	Post.
VDD	0.6	0.32	0.325	0.5	0.9
SNM (mV)	86	111.4	98	96.23	706/377
PDP (fJ)	N/A	12.16	N/A	13.28	12.15
Clock (MHz)	10	3.5	0.6	40	200
Capacity (kb)	256	4	72	4	1
Word Length	16	16	32	8	32
Energy/access (pJ)	11.8	1.5667	0.267	0.1227	**0.0675**
Energy/bit (pJ)	0.699	0.27125	0.18063	0.086	**0.0021**

IV. CONCLUSION

A low energy-consuming SRAM design is demonstarted in this investigation, where several features are added to resolve SNM and power problems in prior SRAMs. More specifically, the added pull-up assit loop and the grounding switch not only enlarge the SNM, but also enhance the noise rejection capability. The VMS circuit reduces the idle power of every unselected column such that the overall power dissipation is reduced. The design can be easily expanded a large memory array, e.g., 1-Mb, since the design methodology is the same.

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