High Resolution Time-to-Digital Converter Design with Anti-PVT-Variation Mechanism

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2021 IEEE 4th International Conference on Electronics Technology (ICET) | 978-1-7281-7673-4/20/$31.00 ©2021 IEEE | DOI: 10.1109/ICET51757.2021.9451146

***Abstract*—This paper presents a 5.4-ps resolution with anti-PVT-variation Time-to-Digit Converter (TDC) using 90-nm CMOS technology. This proposed TDC uses the two-step architecture in which the first stage is Buffer Delay line to get a wide dynamic range and then the delayed start and stop signals are given to the second stage (Vernier Delay line) by an edge detector for higher resolution. This whole two-step architecture is monitored by a PVT Detector to resist Process, Voltage, Temperature (PVT) variation. The proposed TDC archives 5.4 ps resolution with 2 ps delay variation and 890 ps of dynamic range. INL and DNL are simulated to be 1 LSB and 0.8 LSB, respectively.**

***Index Terms*—Buffer delay line, Vernier delay line, Dynamic range, PVT Detector, Resolution**

I. Introduction

TDCs are devices used to measure the time interval between two events and convert this analog information into digital codes. The input time interval of the event is restricted by the dynamic range and resolution of the TDC. Thus, a TDC with fine resolution and wide dynamic range is needed in today's applications such as radar ranging, time of flight, etc. In 1970s, high-energy physics as well as related circuits played a major in nuclear science [1], including the TDC deployment in ADCs [2] and all-digital PLL [3], digital converters [4], to realize analog signals. The traditional TDC (e.g., Buffer Delay Module) is based on digital delay elements which has limited propagation delay [5]. By contrast, Vernier Delay Module has good propagation delay, but limited dynamic range [5]. These both modules suffer from PVT variations. This paper proposes a new TDC which overcomes all these problems and provides fine resolution with a wider dynamic range.

This investigation was partially supported by Ministry of Science and Technology, Taiwan, under grant MOST 108-2218-E-110-002 and 109-2218-E-110-007.

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II. PVT-insensitive Time-to-digit Converter (TDC)

The block diagram of the proposed TDC is in Fig. 1. "start" and "stop" are the beginning and the end of the timing event. This event is sampled by Buffer Delay Module and later the delayed start signal which has close lag to "stop" signal is detected by Edge Detector and sends it to Vernier Delay Module for higher rate sampling. "clk" signal is the input for PVT Detector, where 4-bit code, namely Cin[3:0] is generated to resist the PVT variation in TDC core (two-step architecture). Buffer Delay Module will then generates the digital code of the sampled timing, which is assumed to be 31-bit thermocode Q[30:0] in our demonstration. The 31-bit thermometer code is finally converted into 5 bits, E[7:3], by an encoder. Similarly, 7-bit thermocode V[6:0] of Vernier Delay Module is converted into E[2:0] by the encoder.

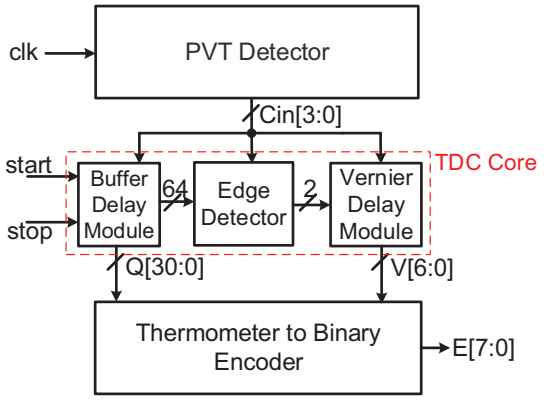

Fig. 1. Block diagram of proposed TDC

A. Buffer Delay Module

As shown in Fig. 2, the start signal is applied to Buffer Delay Line in which each stage output is given as data input

of flip-flop and stop signal is fed to the clock input. The time difference between the rising edges of start and stop signals decreased after each step until the start signal leads the stops signal the output of the flip-flop is '1' after that it becomes '0'. This is illustrated in Fig. 3.

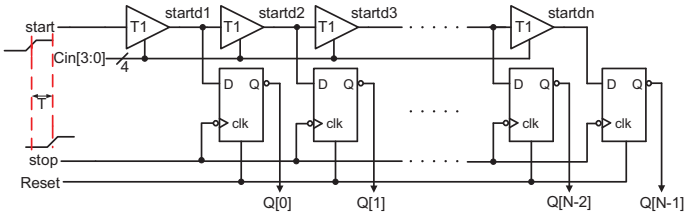

Fig. 2. Buffer Delay Module

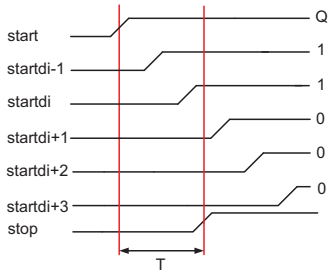

Fig. 3. Timing diagram example of buffer delay module

If the number of delay elements = *N*, then the dynamic range *DR* = *N*×*T1*. The values considered in this work are *T1*=28.7 ps and *N*=31, hence *DR*=890 ps. As for the delay cell design is concerned, it is discussed in Section II-E.

$$DR = N \times T1 \tag{1}$$

B. Edge Detector

Edge Detector is used to detect the delayed start signal in Buffer Delay Module which has a closer lag to stop signal. For example, in Fig. 3, startdi is the closer signal to stop signal. This signal is sent to Vernier Delay Module for further sampling. As shown in Fig. 4, Edge detector contains an NOR gate in which one input is given by $\overline{Q}$ of the present stage with T1 delay and another input is given Q of the next stage flip-flop. NOR gate gives output '1' only when these two inputs are '0'. This happens only when the start signal leads to the stop signal. "v-start" is the output of Edge Detector. "v-stop" is the delayed signal of "stop" signal by T. This delay depends on enable signal.

C. Vernier Delay Module

As shown in Fig. 5, v-start signal is a given input for the upper delay line where each stage output is given to data input of the flip-flop and the v-stop signal is a given input for the lower delay line where each stage output is given as a clock signal to the flip-flops. The time period is the time difference between the propagation of delay cells in the upper and lower

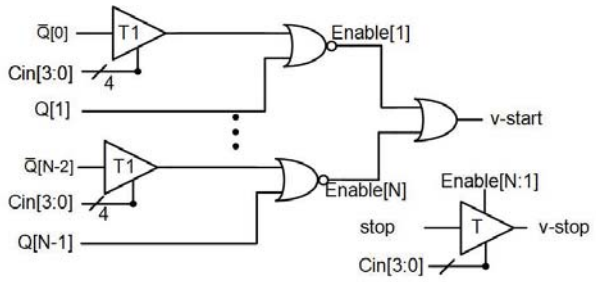

Fig. 4. Edge Detector

delay chain in this structure which is "*T2-T3*", where T2, T3 are the propagation delays of each delay cells at the upper and lower delay line, respectively.

$$T = T2 - T3 \tag{2}$$

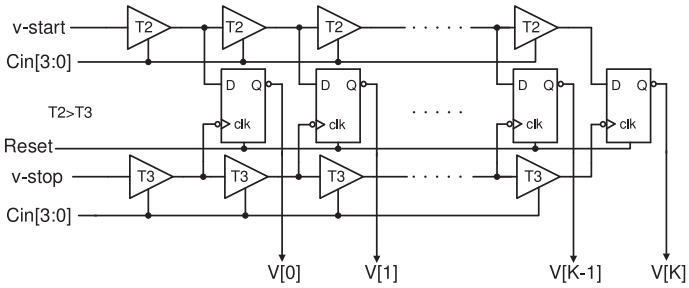

Fig. 5. Vernier Delay Module

D. PVT Detector

A small change in process, voltage, and temperature variation will post large effect on the delay of buffer delay cells. So, using this delay as a reference signal to resist the PVT variation of the TDC core (two-step architecture). As shown in Fig. 6, the PVT Detector is made up of the buffer delay chain in which each stage output is given as input for negative edge trigger flip-flops. "clk" is an input of the delay chain, and it is for negative edge flip-flops.

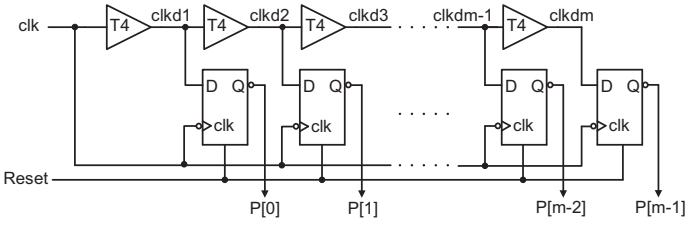

Fig. 6. PVT Detector [9]

This periodical signal is delayed by the buffer chain, wherein each delay buffer delays the "clk" by T4. A total of m delay buffers are used such that clkd1, clkd2,.. clkdm are generated. Notably, in this work, m=36. The m delayed pulse trains are latched by corresponding DFFs triggered by the

original “clk" falling edge. By thorough simulations addressed in Section III, the 19th, 22th, 26th, 29th, and 34th stages of the delay line in PVT Detector are found as the best thresholds to resist PVT variation in Buffer Delay Module and Vernier Delay Module. The outputs of the corresponding DFFs are from the inverted Q is given to encoder to generate Cin[3:0].

TABLE I
CODES GENERATED BY PVT DETECTOR

P19	P22	P26	P29	P34	Cin[3]	Cin[2]	Cin[1]	Cin[0]
1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	0
1	1	1	0	0	1	1	0	0
1	1	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0

The delay cell in this delay line is not same as delay cell in Buffer Delay Module and Vernier Delay Module. The delay cell in PVT Detector is shown in Fig. 7. Mn703 act as a resistor because it is always on. Mn704 acts as a capacitor because source and drain thereof are shorted. An RC delay is then formed by Mn703 and Mn704.

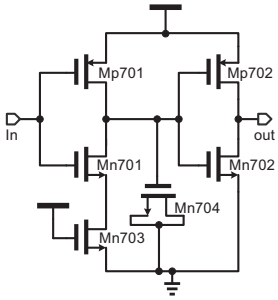

Fig. 7. PVT delay cell [10]

E. Delay cell of TDC Core

With reference to Fig. 2 and Fig. 5 again, the delay cells in the delay lines of Buffer Delay Module and Vernier Delay Module are governed by Cin[3:0], which is directly coupled to outputs of PVT Detector such that the delay will be auto-adjusted. The schematic of the delay cells in the TDC Core is shown in Fig. 8, where the generated PVT code is used to auto-adjust the current-sinking capabilities.

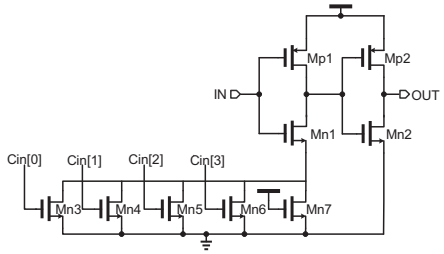

Fig. 8. Delay cell of TDC core

III. SIMULATIONS AND ANALYSIS

The proposed TDC with an anti-PVT-variation feature is implemented using the TSMC 90-nm CMOS process with ultra-thick (34 kA) top metal options. Fig. 9 shows the layout and the floor plan of the full chip, respectively, where the chip area is 798 $\times$ 798 μm^2 and the active area is 426 $\times$ 200 μm^2

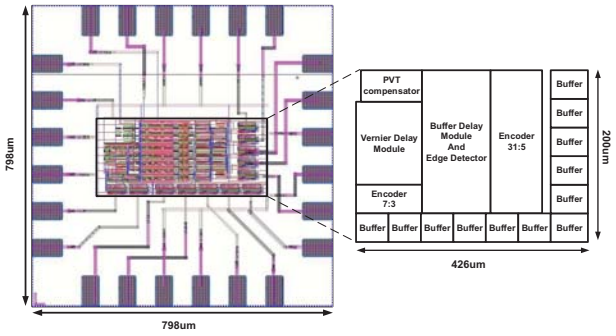

Fig. 9. layout

Fig. 10 is the simulation results of process (SS, SF, TT, FS, FF), voltage (-15%, -10%, -5%, 0%, +5%, +10%, +15%), temperature (25^0C) variation. In the worst corner, a 5.4 ps delay is found. Namely, the resolution of the TDC is 5.4 ps, and the delay variation is 2 ps. We already calculate the dynamic range in Eqn. (1) which attains 890 ps. Fig. 11 is the all-PVT-corner simulation results of the PVT Detector, where clkd19, clkd22, clkd26, clkd29, clkd34 are confirmed to be the thresholds to generate the signals P19, P22, P26, P29, P34 in Table I and Fig. 12 is the transfer function of the proposed TDC. Fig. 13 is the post-layout simulation result at the worst corner. Table II shows the overall performance comparison of the proposed TDC versus several prior works. Notably, the FOM (figure of Merit) is defined as follows. Our work attains best FOM. Besides, the proposed TDC is superior to every other work in terms of resolution and delay variation.

$$FOM = (|INL| + |DNL|) \times Power \times \\ Resolution \times DelayVariation \quad (3)$$

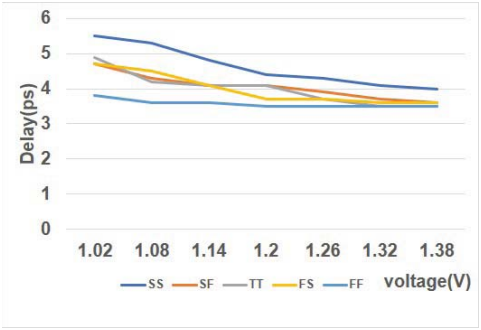

Fig. 10. Resolution at 25^0C for different VDD and process corners

TABLE II
TDC PERFORMANCE COMPARISON

	ISSCS 2015 [6]	*ICCE 2016 [7]*	*TCAS-II 2018 [8]*	*MEJ 2018 [9]]*	*TVLSI 2020 [10]*	*This work**
arch.	vernier	DLL	Ring OSC	Dual DLL	TDL	two step
Process	65nm	65nm	130nm	180nm	90nm	90nm
Verifi.	Simul.	Simul.	Meas.	Meas.	Meas.	Simul.
Resol.	6.15ps	2ps	43.2ps	15ps	30ps	5.4ps
DR	1260ps	1us	N/A	500ns	997ps	890ps
clock	40MHz	N/A	100MHz	100MHz	100MHz	100MHz
Power	2.5mW	69.7mW	1.72mW	75mW	2.22mW	9.1mW
INL	2LSB	1LSB	-2.5LSB	4LSB	0.2LSB	1LSB
DNL	1.2LSB	1LSB	-1LSB	1.7LSB	0.5LSB	0.8LSB
Delay variation	4ps (0.65LSB)	N/A	6.4ps (0.15LSB)	10ps (0.67LSB)	11ps (0.37 LSB)	2ps (0.37 LSB)
FOM	0.197	> 0.279	1.665	64.125	0.513	0.177

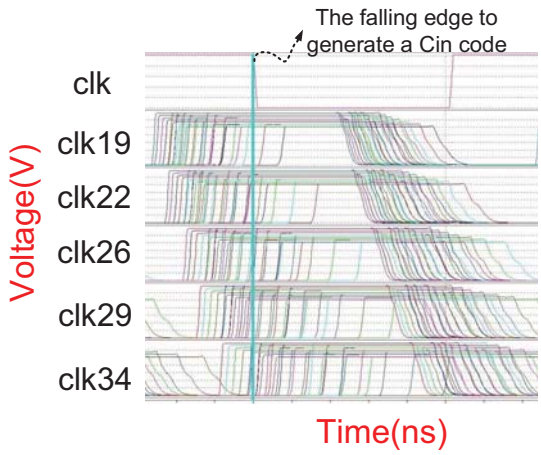

Fig. 11. All-PVT-corner simulation of PVT Detector

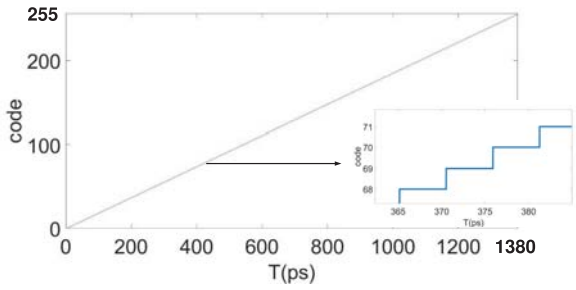

Fig. 12. Transfer function of the proposed TDC

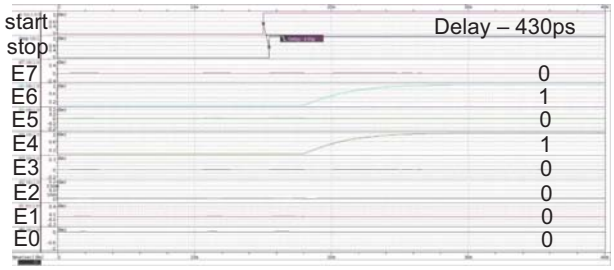

Fig. 13. post layout stimulation

IV. CONCLUSION

The major contribution of this work is to increase resolution with reasonable dynamic range and improve the efficiency of the self-adjustment capability provided by the PVT Detector.

ACKNOWLEDGMENT

The authors express their deepest gratefulness to Taiwan Semiconductor Research Institute (TSRI) of National applied Research Laboratories (NARL), Taiwan, for the providing a Research platform to work in 90-nm technology in cadence virtuoso tool.

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