4.15 W SIDO Buck Converter with Low Cross Regulation Using Adaptive PCCM Control

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***Abstract*—A 4.15 W SIDO buck converter is proposed in this paper. By using the adaptive PCCM control, the FW (freewheel) phase is automatic adjusted to improve the efficiency, which is the weakness in traditional PCCM control. Besides, the current mode comparison is utilized, such that the comparators are not required for the mode control. The proposed design is implemented using TSMC 0.18 µm CMOS HV process. Based on the simulation results, the circuit achieves the cross regulation of 0.097 mV/mA and 0.066 mV/mA for the dual outputs with the load current variation from 0.5 A to 0.4 A and from 0.45 A to 0.5 A, respectively.**

Keywords—SIDO, buck converter, cross regulation, PCCM.

I. INTRODUCTION

With the fast development of semiconductor technology, there are lots of components used in different electric products. It requires different power supply voltages, such that SIDO (Single inductor dual output) DC/DC converters are widely used to save the system cost and to reduce the system size [1]-[12].

Besides the load regulation, the cross regulation is another important specification to refer to cross effects caused by load variation of the dual outputs for the SIDO DC/DC converter. For a traditional SIDO buck converter, the cross regulation is not a problem when it operates in DCM because the driving current for the dual outputs, V_{OA} and V_{OB}, are separated, as shown in Fig 1(a) [2], [5]. However, the DCM is difficult to use for large driving current. An interleaving control is presented for the SIDO DC/DC converter to improve the current in CCM [3]. Referring to Fig. 1 (b), there are 4 phases in a period. Phase 1 and phase 4 are used to drive the first output, V_{OA}. Phase 2 and 3 are for the second output, V_{OB}. Although the driving current is increased, the control circuit is very complex. Power distributive control is another widely used method for large driving current in CCM [4], [7]-[9], because the control circuit is easy to implement. Referring to Fig. 1 (c), phase 1 is to charge the inductor. Phase 2 and phase 3 are used to drive the dual outputs, V_{OA} and V_{OB}, respectively. Because the driving currents of the dual outputs are successive for the above methods in CCM, the cross regulation is difficult to optimize. PCCM (Pseudo continuous conduction mode) is presented to improve the cross regulation by adding an additional operation phase using a freewheeling switch [1], [10]-[12]. As shown in Fig. 1 (d), in the FW (Freewheel) phase, the inductor current flows through the FW switch and the driving current for the dual output is separated such that the cross regulation is improved. However, the efficiency is poor for the PCCM control, because of the current waste in the FW phase caused by the parasitic resistor of the FW switch. The attenuation of efficiency becomes more serious when the driving current is large. Thus, traditional PCCM control is not a good choice for large power application.

In this work, a 4.15 W SIDO buck converter is proposed for the application of the 12 V miniature AUV (Automatic underwater vehicle) system [13]. By using the adaptive PCCM control, the FW phase is automatic reduced to improve the efficiency in large driving current application. The proposed design is carried out using TSMC 0.18 µm CMOS HV process. The simulation results show that the cross regulation is 0.097 mV/mA and 0.066 mV/mA for the dual outputs, V_{OA} and V_{OB}, respectively.

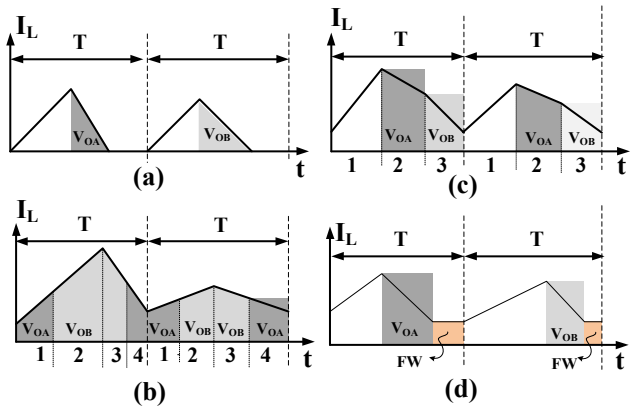

Fig. 1 Operating waveforms of I_L in traditional SIDO buck converters using (a) DCM (b) CCM with interleaving control, (c) CCM with power distributive control, and (d) PCCM.

II. THE PROPOSED SIDO BUCK CONVERTER USING ADAPTIVE PCCM CONTROL

Fig. 2 shows the block diagram of the proposed circuit, including a SIDO buck converter, a FW switch, an Adaptive PCCM control circuit, a PWM control circuit, a Mode Control circuit, a Current Sensor 1, two Current Sensors 2, a Driving circuit 1, and a Driving circuit 2. Except for the off-chip devices with gray shade, the proposed design includes the power MOS transistors on-chip. The power transistors, M_P and M_N, are 12 V devices to prevent the damage caused by the 12 V input voltage. The power transistors, M_A and M_B, are 5 V devices, because V_Y varies between 5 V and 3.3 V. The power transistors, M_{F1} and M_{F2}, are also 12 V devices to serve as the FW switch. Current Sensor 1 detects the inductor current and generates the output signal, V_{SENSE}, for PWM control circuit. The Adaptive PCCM control employs two Type 2 compensators for the frequency compensation for the two feedback signals, V_{fbA} and V_{fbB}. Besides, a counter and two switches, M_{EA} and M_{EB}, are used to select the control channel. The PWM control circuit utilizes a comparator, a SR-latch, and a Ramp & CLK Generator to generate the

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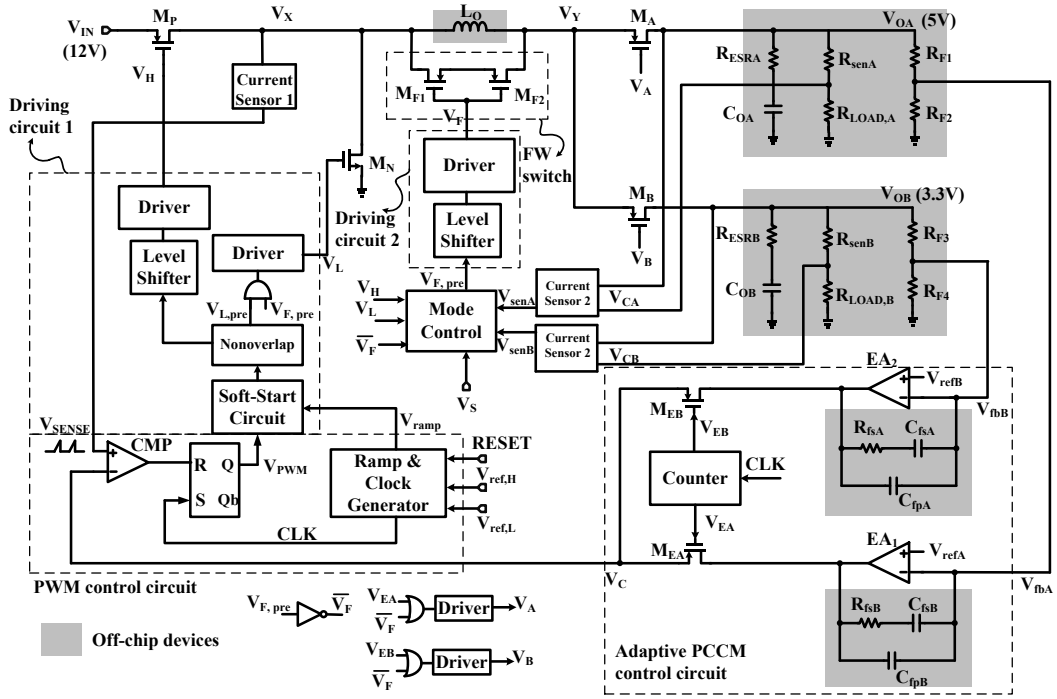

Fig. 2 Block diagram of the proposed SIDO buck converter with adaptive PCCM control.

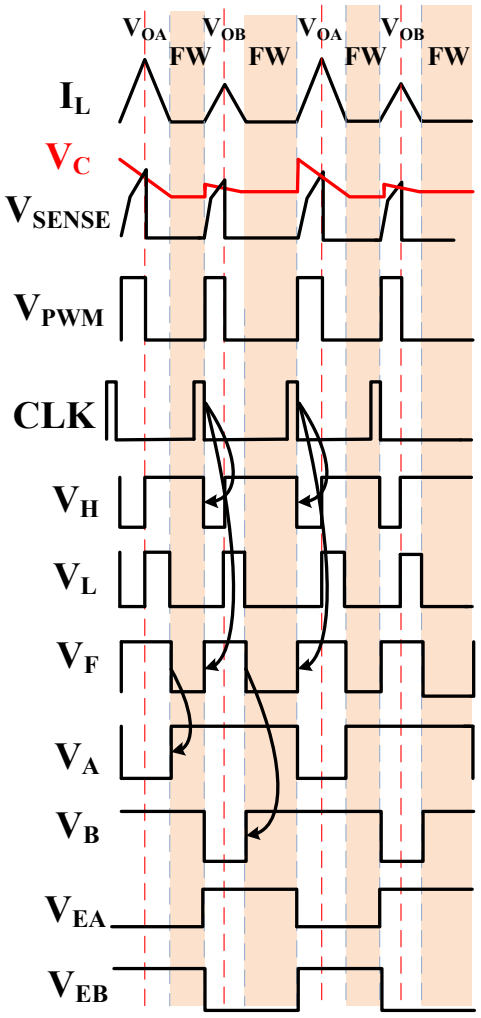

Fig. 3 Operating waveforms of the control signals..

PWM control signal, V_{PWM}. The Driving circuit 1 includes the Soft-Start Circuit, a Nonoverlap circuit, a Level Shifter, and Drivers to provide the control signals, V_H and V_L, for M_P and M_N, respectively. The Driving circuit 2 includes a Level Shifter and Driver for generating the control signal, V_F, for M_{F1} and M_{F2}. The two Current Sensors 2 detect the two driving currents, I_{OA} and I_{OB}, and generate the control signals, V_{senA} and V_{senB}, respectively, for the Mode Control circuit.

A. Adaptive PCCM Control

Referring to Fig. 2 and Fig. 3, the Counter generate the control signals, V_{EA} and V_{EB}, to select the feedback signal path from V_{OA} or V_{OB}. When V_{EA} is logic 0, the feedback loop from V_{OA} is used. When V_{EB} is logic 0, V_{OB} is then feedback to generate the signal V_C. V_C is then compared to the sensed inductor current signal, V_{SENSE}. V_{PWM} is pulled high when the pulse CLK occurs. When $V_{SENSE} > V_C$, V_{PWM} is then reset by the SR latch, which pulls V_H and V_L to logic 1. It indicates that the inductor charging phase is finished and the inductor starts to discharge to the outputs. V_A = logic 0 and V_B = logic 0 are used to enable the outputs, V_{OA} and V_{OB}, respectively. Notably, V_A becomes logic 0 when V_F is logic high and V_{EA} is logic 0. V_B is activated in the similar way.

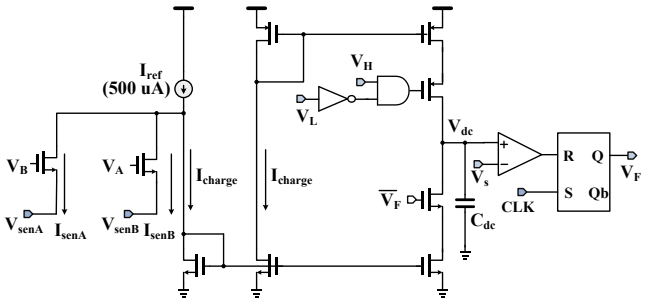

Fig. 4 Schematic of the Mode Control circuit.

B. Mode Control Circuit

Fig. 4 shows the schematic of the Mode Control circuit. V_H and V_L are used to control a charging current path for the capacitor, C_{dc}. $\overline{V_F}$ is used to control the discharging current path. The sensed current signals V_{senA} and V_{senB} is compared

in the current mode comparison. The charging current is expressed by the following equation.

$$I_{charge} = \begin{cases} I_{ref} - I_{senA}, & when\ V_{OA}\ is\ chosen \\ I_{ref} - I_{senB}, & when\ V_{OB}\ is\ chosen \end{cases} \quad (1)$$

The duration of the FW phase is then determined by Eqn. (2).

$$t_{FW} = \frac{C_{dc} \cdot V_S}{I_{charge}} \quad (2)$$

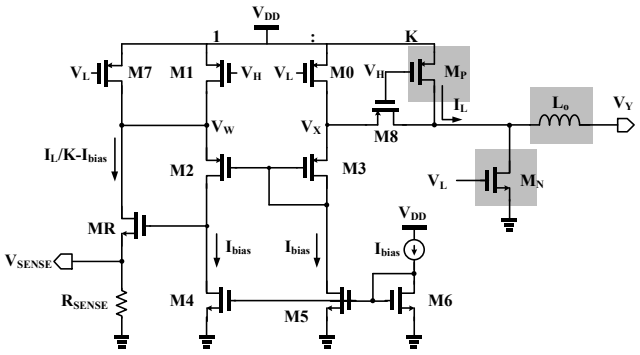

Fig. 5 Schematic of the Current Sensor 1.

C. Current Sensor 1 and Current Sensor 2

The Current Sensor 1 is revealed in Fig. 5. By choosing the feature size of the transistors of M1 and M_P with the ratio equaling to 1/K, the current through M1 and M2 would be $\frac{I_L}{K}$ and I_{bias}, respectively. Thus, the sensed internal current through MR equals to $\frac{I_L}{K} - I_{bias}$. The output voltage, V_{SENSE}, is then expressed by the Eqn. (3). If $I_{bias} \ll \frac{I_L}{K}$, V_{SENSE} is linearly proportional to the inductor current, I_L.

$$V_{SENSE} = \left(\frac{I_L}{K} - I_{bias}\right) \cdot R_{SENSE} \quad (3)$$

Referring to Fig. 6, the Current Sensor 2 use the resistor, R_{senA}, to sense the load current. Because of the virtual short in the feedback loop, the voltage drops on Rc and R_{senA} equal to each other. Thus, the sensed current is $I_{senA} = \frac{R_{senA}}{R_c} \cdot I_{LOADA}$. The sensed voltage is obtained in Eqn. (4).

$$V_{senA} = \frac{R_{sen2} \cdot R_{senA}}{R_c} \cdot I_{LOADA} \quad (4)$$

D. Ramp and Clock Generator

Fig. 7 shows the schematic of the Ramp and Clock Generator. The ramp signal is obtained by charging and discharging for the capacitor, C_{ramp}. V_{refH} and V_{refL} are the external reference voltages to determine the peak and the valley of the ramp signal. CLK signal is generated by the SR latch.

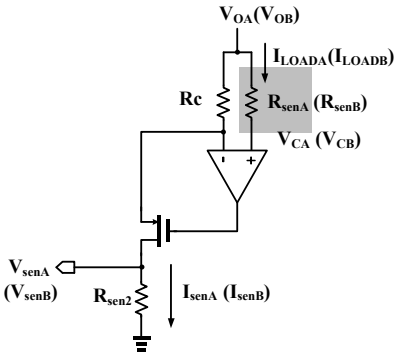

Fig. 6 Schematic of the Current Sensor 2.

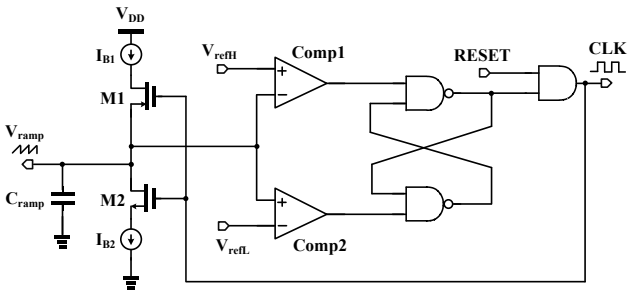

Fig. 7 Schematic of the Ramp & Clock Generator.

III. Implementation and Simulation Results

The proposed design is implemented using a typical 0.18 µm CMOS HV process. Fig. 8 shows the simulated waveforms of the dual output voltages with the load currents of 0.5 A. The DC voltage of V_{OA} is 5.0 V with ripple of 120mV. V_{OB} is at 3.3 V with ripple of 270 mV. The current ripple of I_A and I_B are 13 mA and 40 mA, respectively. Fig. 9 reveals the simulated line regulation. The overshoot is 1 mV and 1.61 mV for V_{OA} and V_{OB}, respectively, when V_{IN} varied from 12 V to 10.8 V. For V_{IN} changing from 10.8 V to 12 V, the overshoot for V_{OA} and V_{OB} is 1.68 mV and 1.5 mV, respectively. The line regulation is 1.4 mV/V and 1.34 mV/V for V_{OA} and V_{OB}, respectively. Fig. 10 shows the simulation results of the load regulation and the cross regulation for I_A varied between 0.5 A and 0.4 A. The load regulation for V_{OA} is 4.9 mV/mA. The cross regulation for V_{OB} is 0.066 mV/mA. Fig. 11 reveals the simulated waveforms for I_B varied between 0.5 A and 0.45 A. The load regulation of V_{OB} is 6.3 mV/mA. The cross regulation for V_{OA} is 0.097 mV/mA. The peak efficiency is simulated to be 86.315% for I_A = 0.5 A and I_B = 0.5 A.

Table I summarizes the performance comparison with several prior works. The proposed design provides the best cross regulation, the maximum output current and the maximum output power. The FOM (Figure of merit) is given by including the peak efficiency, the maximum load current and the cross regulation. The proposed design possesses the best performance.

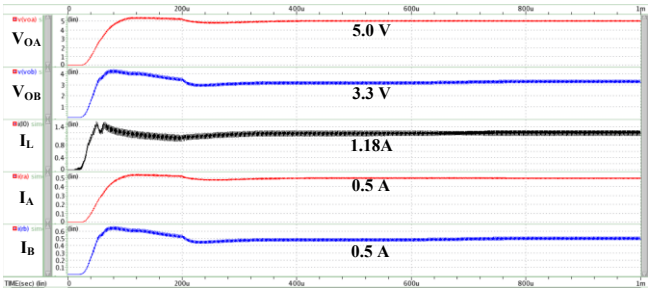

Fig. 8 Simulated waveforms with I_A of 0.5 A and I_B of 0.5 A.

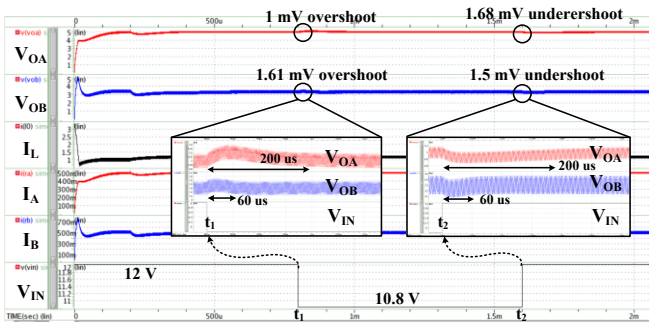

Fig. 9 Simulated line regulation with V_{IN} varied between 12 V and 10.8 V.

TABLE I. COMPARISONS WITH PRIOR WORKS

	[5]	[6]	[7]	[8]	[9]	This Work
Publication	VLSI DAT	CICC	ISNE	ISCAS	MEJ	SPIES
Year	2010	2012	2013	2016	2019	2020
Technology (μm)	0.35	0.35	0.18	0.13	0.18	0.18
Implementation	Meas.	Meas.	Sim.	Sim.	Meas.	Sim.
Type	Buck	Buck-Boost	Buck-Boost	Buck-Boost	Boost	Buck
Control Method	TMC	OPDC	TMC	TMC	OPDC	TMC
Input voltage (V)	3.6	3.7	1.6-3.3	1.8	0.5-1	12
Output voltage(V)	1.8/2.5	5/1.8	2.5/3.6	2/2.5/1.5/2.2	1.8/1.2	5/3.3
Frequency (MHz)	0.5	1	1	0.5	1	1
Max Load(mA)	36/20	80/80	100/180	50/50/50	40/40	500/500
Peak Efficiency (%)	80	82	91.5	83.76	91	86.315
Cross Regulation(mV/mA)	0.7	N/A	2.7/2	0.7	0.2/0.11	0.097/0.066
Load Regulation(mV/mA)	N/A	0.457/0.142	0.1/2.4	1.51	N/A	4.9/6.3
Line Regulation(mV/V)	N/A	7/ 7	1.0/5.0	N/A	N/A	1.4/1.34
FOM*	11.4	N/A	6.1/4.6	6.0	18.2/33.1	447.9/658.3

Note: * FOM = (Max. load current × peak efficiency)/(Cross-regulation).

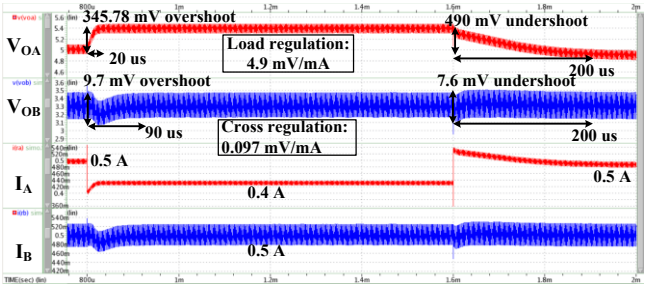

Fig. 10 Simulated load regulation and cross regulation with I_A varied between 0.5 A and 0.4 A.

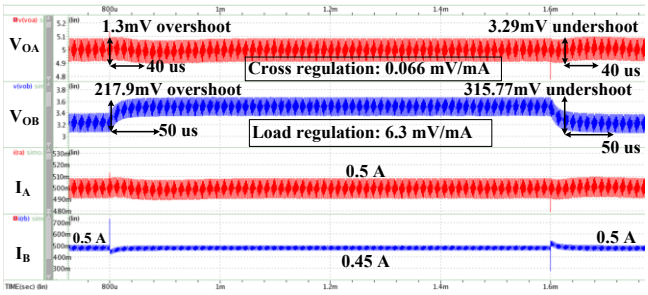

Fig. 11 Simulated load regulation and cross regulation with I_B varied between 0.5 A and 0.45 A.

IV. CONCLUSIONS

By using the adaptive PCCM control, the cross regulation is improved to be 0.097 and 0.066 mV/mA, for the dual output, respectively. Besides, the proposed design could provide large driving current of 0.5A for the two output at the same time, such that the maximum output power of 4.15 W is achieved.

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