Sampling Rate Enhancement for SAR-ADCs Using Adaptive Reset Approach for FOG Systems

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***Abstract*—In this investigation, an adaptive reset strategy of a 10-bit SAR-ADC particularly designed for the applications in FOG (fiber optic gyroscope) systems is demonstrated with TSMC 40 nm CMOS technology. The proposed adaptive reset approach takes advantage of high correlation of the phase shift generated by continuous FOG signals such that MSB bits of two consecutive samples likely remain the same, which implies there is no need to re-converted. By replacing conventional all-reset method with the adaptive-reset strategy, the throughput of the SAR ADC is theoretically increased up to around 100%. The sampling rate is increased by 2 times compared with the conventional counterpart.**

Keywords— FOG, SAR ADC, adpative reset strategy, sample rate, high throughput

I. Introduction

In the recent research for fiber optic gyroscope (FOG) systems, it can be completely solid-state fabricated, which is typically considered low cost, small size, long operation time, and high yield thanks to low manufacturing complexity compared to ring laser gyroscope (RLG) [1]. Considering the demand of low power, accuracy, and sampling rate in FOG systems, successive approximation register analog-to-digital converter (SAR-ADC) is considered as a better solution than other ADC designs. However, most of the FOGs might be used in mobile or portable systems, e.g., cellular phones. Attaining low power dissipation, high resolution, and high throughput in real time becomes a design dilemma. It is also true for the SAR ADCs to be applied in FOGs. To achieve low power consumption, accuracy with calibration, and high sampling rate, many methods have been proposed for SAR ADCs. For example, charge redistribution method for binary-weighted can reduce the switching energy [2] [3]. Background self-calibration approaches can ensure the accuracy of ADC's effective number of bits (ENOB) [4] [5]. Time-interleaved ADC using multi-channel can increase sampling rate to GS/s [6] [7].

When it comes to the required high sampling rate and low power demand of FOG applications in real time, none of the existing designs can fully increase the rate without penalty in power or area. Take the conventional 8-bit SAR-ADC as an example. It takes eight clock cycles to convert into digital codes and another one clock cycle to reset all the outputs. Although it generates the output codes periodically, which is predictable and easy to be applied in any system, it is considered as a waste of time and energy in certain applications of which the input signals are highly similar between two consecutive samples. Take the FOG as the illustrative example. Two beams from a laser are splitted and injected into the same fiber but in opposite directions, namely clockwise vs. anti-clockwise. Due to the Sagnac effect, the beam traveling against the rotation experiences a slightly shorter path delay than the other beam. The path delay is then converted into a phase shift denoting the angel of rotation. Unlike the classic spinning-mass gyroscope or resonant/mechanical gyroscopes, FOGs have no moving parts and no inertial resistance so that the consecutive samples are almost free from noise and other interferences. This feature leads to high similarity or correlation between two consecutive samples. Thanks to this feature, we propose to reset only LSB half of all bits when input signals are within in a certain range relative to the previous one to increase the throughput and save power at the same time.

II. Adaptive Reset for SAR Logic Used in FOGs

The phase shift difference caused by the Sagnac effect is calculated by the system shown in Fig. 1. As a matter of fact, it is also the baseband integrated circuit of the entire FOG. SAR-ADC recieves the amplified and downconverted signal generated by the photo detector, and converts into 10-bit digital code coupled to Logic Core which carries out the computation tasks. Logic core, on the other way around, will trigger the adaptive reset if necessary. The feature of the input voltage signal of FOG generated by photo detector is demonstrated in Fig. 2, where it is like a impulse train. Most of the time, the input voltage is kept at V_{LB}. The input voltage rises directly to the upper bound V_{UB} very soon and then drops immediately and exponentially. Apparently, we can take advantage of this feature to design an application-specific SAR with high sampling rate and low power dissipation.

Besides the required resoultion, the conversion speed for real time operation and the low power for mobile applications are another two critical specifications. Most of the existing ADC solutions are very hard to meet all these requirements. To meet the specific demand of ADC for FOG systems, the proposed adaptive reset strategy is demonstrated with 10-bit conventional differential monotonic capacitor SAR-ADC, as shown in Fig. 3, which is the SAR [8] integrated with an adaptive reset scheme. It is composed of two bootstrapped

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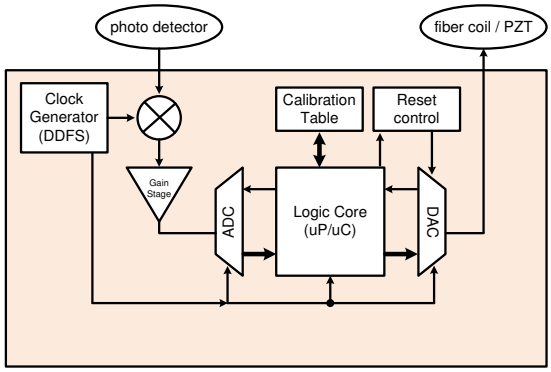

Fig. 1. Diagram of FOG baseband system

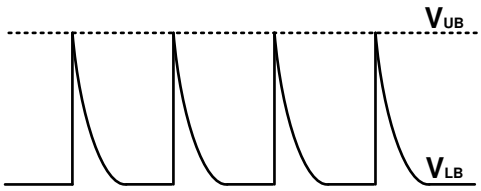

Fig. 2. Typical waveform generated by FOG's photo detectors

switches, two differential DAC arrays with switches, a high-speed high-resolution comparator, and an SAR logic circuit with adaptive reset control.

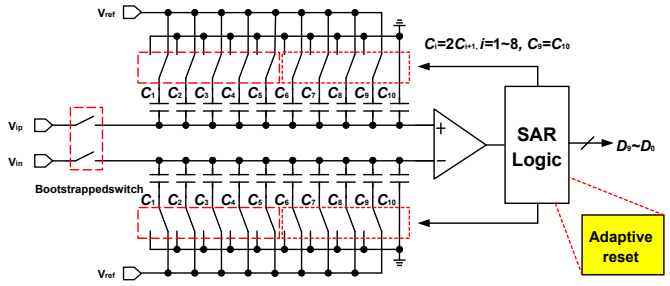

Fig. 3. SAR ADC with adaptive reset

To demonstarte the feature of the proposed method, Fig. 4 is an example which uses the ramp signal as an example. The x-axis represents the time and y-axis is the voltage. The conventional sample method takes exactly the same time interval T to convert every sample. By contrast, the proposed sampling method takes only T/2 under certain conditions. Therefore, with the same amount of time, the through rate, or sampling rate, of the proposed reset method is obviously higher. Fig. 5 shows the comparison of the proposed method and the conventional reset. Notably, after conversion 1, the proposed method will keep D9-D5 based on the condition that the these values are identical to the previous one such that the overall 3 conversions will be carried out at the 23rd clock cycle. By contrast, the conventional reset approach finish 3 conversions at the 33rd cycle. In fact, the worst sampling rate of the proposed reset method is the same as that of the conventional reset SAR.

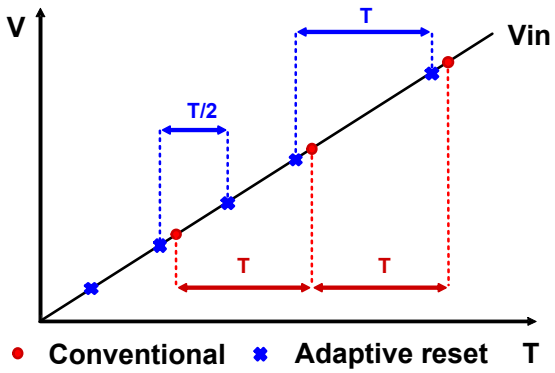

Fig. 4. An example of adaptive reset

	Conventional										
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
conversion1	1	2	3	4	5	6	7	8	9	10	11 (reset10)
conversion2	12	13	14	15	16	17	18	19	20	21	22 (reset10)
conversion3	23	24	25	26	27	28	29	30	31	32	33 (reset10)

	Proposed										
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
conversion1	1	2	3	4	5	6	7	8	9	10	11 (reset5)
conversion2	hold	hold	hold	hold	hold	12	13	14	15	16	17 (reset5)
conversion3	hold	hold	hold	hold	hold	18	19	20	21	22	23 (reset5)

Fig. 5. Comparison between the proposed adaptive reset and the conventional reset

A. SAR Logic Circuit with Adaptive Reset

In order to carry out the proposed adpative reset method in Fig. 4, the SAR logic with adaptive reset control is shown in 6, where 22 DFFs for a 10-bit logic design and an additional DFF to separate the reset strategy starts from [D9:D0] or only [D4:D0]. The clk counter will automatically make the reset decision when end-of-conversion (eoc) signal is asserted. The system will compare the new [D4:D0] with the previously stored [D4:D0] to see if they are the same. If not, as shown in Fig. 7, it resets only [D4:D0]. Otherwise, reset [D9:D0], i.e., all bits. Notably, some possible misjudgements are also tabulated in Table I to be analyzed below.

TABLE I
POSSIBLE MISJUDGE CONDITIONS

Scenario	previous [D9:D0]	new [D9:D0]	system execution	suggested execution
1)	00110-00011	00000-00001	reset5	reset10
2)	00110-00011	00110-00111	reset10	reset5 is better

1) The situation may happen when the input signal varies too fast between two conversion cycles. Therefore, despite [D4:D0] is not the same, the suggested execution is reset10. However, if such a scenario is detected, the ADC must have improper sampling rate and clock cycle.
2) This scenario occurs when input signal is a fixed voltage. Two [D9:D0] are identical, and the system will execute reset10. However, although reset5 is a better option in this case, the overall sampling rate still better than that of the conventional method.

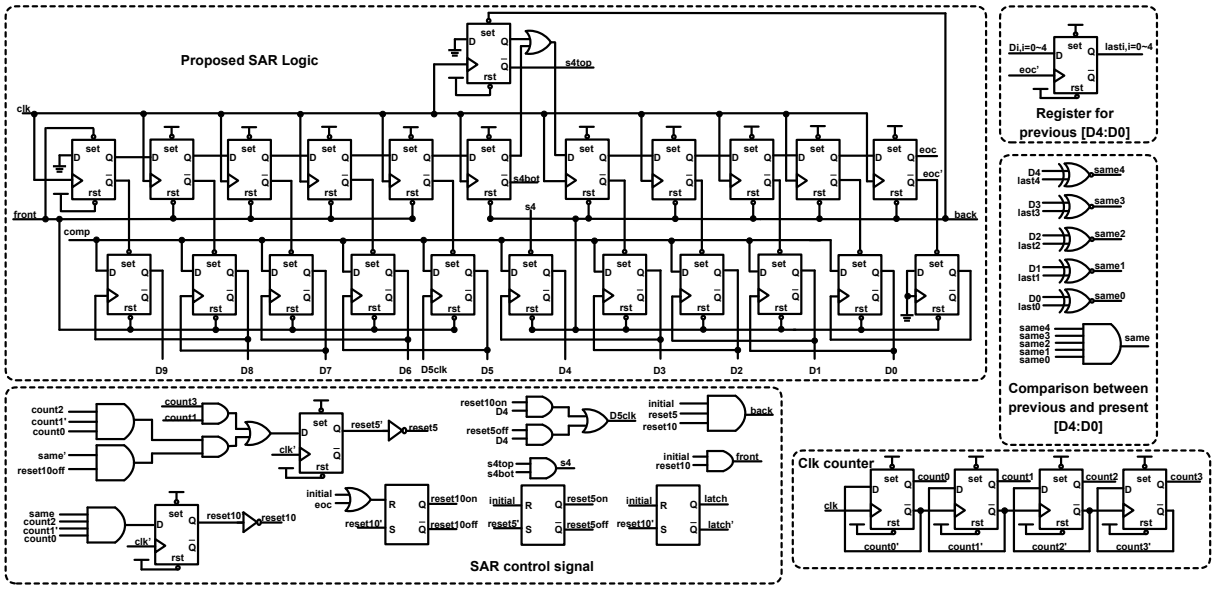

Fig. 6. SAR logic with adpative reset control

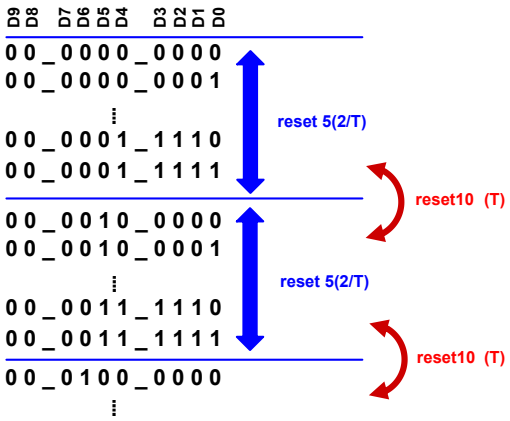

Fig. 7. Adaptive reset range.

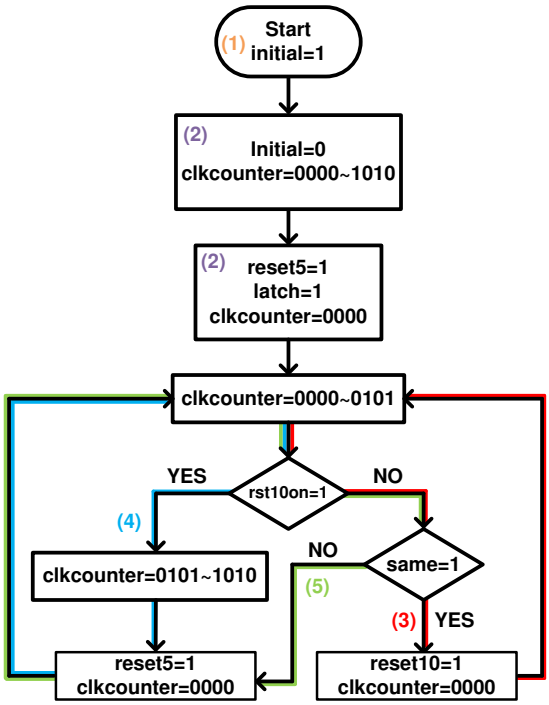

Fig. 8. Flow chart of the adpative reset method

B. Adaptive Reset Algorithm

In short, the conversion waveform using adaptive reset is summarized in Fig. 8, where 5 steps (1) to (5) are briefed as follows.

1) Initial signal resets all DFFs and RS latches.
2) This is the first 10-cycle conversion of ADC. It locks up latch signal to high, which ensures the status of ADC will go through steps 3), 4), or 5), repeatedly. Then, at the end of eoc, it is guaranteed to enable reset5 and store [D4:D0].
3) Clk counter counts to 00101. If rst10on=0, the previous [D9:D5] is locked up and continues to complete the recent conversion. Then, the new [D4:D0] are compared with the previously stored [D4:D0]. If they are the same, set reset10 and rst10on to high and clear clk counter. Otherwise, go to step 5).
4) Clk counter counts to 00101. If rst10on=1, it continues counting to 01010 and converts all [D9:D0]. The reset5 will be pulled up high at the end of eoc and flush the clk counter.
5) Clk counter counts to 00101. If rst10on=0 and the comparison is not the same, reset5 will be high and flush clk counter.

III. Simulation and Verification

The proposed SAR ADC with the proposed adpative reset method is realized using TSMC 40 nm CMOS process. Fig. 9 shows the layout of the proposed design, where the core are is 126×123 μm^2 and the entire chip area is 541×524 μm^2. With reference to Fig. 10, a timing waveform snapshot generated by post-layout simulations is demonstrated to justify the correctness of the proposed adpative reset method.

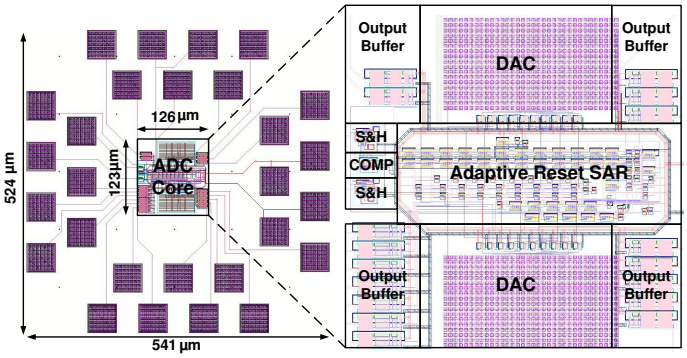

Fig. 9. Layout of the proposed design

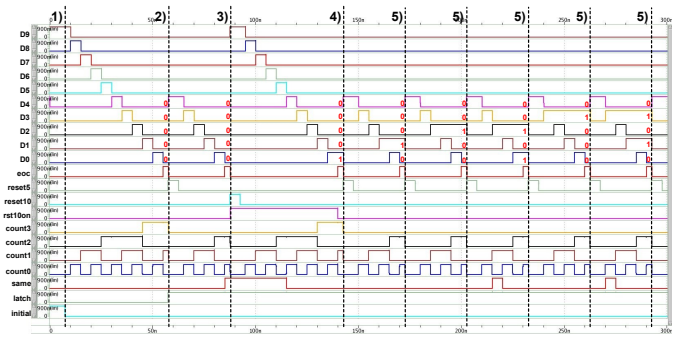

Fig. 10. Post-layout simultaion waveform

With reference to Fig. 10, it shows the simulation waveforms to demonstrate the feature of the proposed adaptive reset method. Besides the conversions at label 1) and 3), all the rest conversions are carried out with fixed [D9:D5]. Not only the conversions are all correct, the throughput is significantly raised.

Table II shows the comparison with several prior works. Although the proposed ADC is not as fast as [8], its sampling rate fits the demand of FOG applications. And the FOM (energy cost) is only half of this prior work. Notably, he main contribution of this work is the adpative reset strategy. It is the only one to demonstrate the reset strategy to enhance sampling rate. At the cost of 5.2% more power, the sampling rate can at least raise 57.1% in the worst case.

IV. Conclusion

This work presents a novel reset strategy which is demonstrated on a 10-bit SAR-ADC for applications in FOG systems. The proposed design is designed using TSMC 40 nm CMOS technology. Several different input signals are used for demonstration, inlcuding ramp, sine, fixed DC voltage, and three mixed sines, where the sampling rates are enhanced over 66.5%, 72.5%, 57.1%, and 83.5%, respectively. Notably, the proposed reset strategy can be adapted onto any kinds of SAR-ADC logic circuits.

TABLE II
Comparison Table

	[8]	[9]	[10]		This work	
Year	*JSSC* 2010	*ISCAS* 2016	*ISCAS* 2017		fixed 2019	adap. 2019
Process (nm)	90	130	40		40	
Resol. (bits)	10	12	12		10	
Fs (MS/s)	100	10	10	40	10	20
SNDR (dB)	56.6	N/A	67.3	63.5	57.1	56.0
SFDR (dB)	71.0	N/A	81.1	73.7	63.5	62.8
ENOB (bits)	9.1	11.7	11.3	10.8	9.2	9.01
FOM (fJ/step)	77.0	6.3	22.5	25.7	37.5	40.3

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