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# 2.5 GHz Data Rate 2×VDD Digital Output Buffer Design Realized by 16-nm FinFET CMOS

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***Abstract*—A 2×VDD output buffer equipped with SR (slew rate) self-adjustment mechanism driven by a PVT (process, voltage, temperature) detector is proposed in this investigation. Notably, the proposed buffer design is realized by 16-nm FinFET CMOS technology, where specical design constraints required by FinFET must be taken into consideration. In other words, design trade-off will be discussed and highlight. To enhance the output SR, awlays-on driving transistors in Output Stage must be realized with low Vth devices to boost the output current. For FinFET devices, The gate drives of these driving transistors must be stablized to prevent any possible noise interference. Nonoverlapping signaling control is directly realized in transistor level instead of conventional gate level designs such that the the speed is fastened. According to the all-PVT-corner simulations, the worst data rate is 2.5/2.5 GHz with 20 pF loading when the supply voltage is 0.8/1.6 V, respectively. The Δ SR improvement is at least 10%, when the proposed SR self-adjustment mechanism is activated.**

**Keywords—** FinFET, output buffer, PVT detection, mixed-voltage tolerant, slew rate self-adjustment

## I. Introduction

Ever since the first report for FinFET in 1999, this novel technology has been considered a major challenger of planar or bulk CMOS when the technology evolved into $< 20$ nm. The main principle behind FinFET is a thin body, around 10 nm or less, such that the gate capacitance is closer to the channel. Thus, there is no leakage path close the gate. FinFET devices attains numerous advantages over planar (bulk) CMOS, including higher drive current for a given transistor aspect, higher speed, lower leakage, lower power consumption, no random dopant fluctuation, hence better mobility and scaling feature for technology node better than 20 nm. However, many end products or systems still need chips fabricated using legacy processes using higher voltage supplies, e.g., 1.8 V or 3.3 V. Therefore, mixed-voltage I/O buffer for FinFET devices is considered as a solution to carry out data exchange with chips fabricated by different processes [1], [2], [3]. Otherwise, area-consuming and power-hungry voltage level translaters are needed.

Besides harsh design constraints of FinFETs, the slew rate is another major issue for digital transmission between FinFET and legacy technologies. The SR variation to violate interfacing standars is mainly caused by various PVT senarios aside from the significant leakage issue in advanced technologies. Prior researchers reported many different PVT detection methods for mixed-voltage I/O buffers to adjust the SR correspondingly, e.g., [4], [5]. The major problem is that most of these reports detected only 3 process corners, namely TT, FF, and SS. Besides, Many of these reported methods may cause long settling time and missing code resulting poor SR since these methods need multiple clock cycles to determine what the current scenario is [5]. As for digital-based process detectors, they were reported to provide a robust solution for the detection and fasten data rate with the penalty of power and area [6]. On top of these problems, none of the prior solutions were focused on the mixed-voltage digital buffers for FinFET CMOS.

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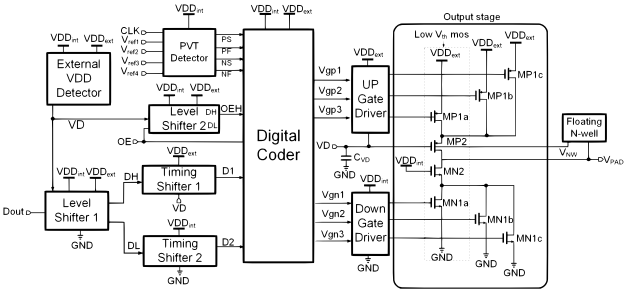


Fig. 1. Proposed 2×VDD digital output buffer using FinFET.

## II. 2×VDD Output Buffer Using FinFET Devices

The proposed digital buffer mainly comprises Floating N-well circuit, Level Shifter (LS), UP and DOWN Gate Drivers, PVT Detector, External VDD Detector, Timing Shifters, Digital Coder, and Output Stage comprising driving transistors, as shown in Fig. 1. CLK is the system clock, while $V_{PAD}$ denotes output port loaded with off-chip discretes. Dout is the digital signal given by the internal logic circuit or core to be transmitted outward. The operation of the proposed design is briefed as follows.

1). PVT detector is coupled with CLK to generate 4 digital signals, namely PS, PF, NS, and NF. Notably, 4 temperature-insensitive reference biases, i.e., $V_{ref1}, V_{ref2}, V_{ref3}, V_{ref4}$, are provided by a conventioal bandgap bias geneartor (not shown).
2). External VDD Detector decides what voltage level of the external device is so as to generate the VD to following Level Shifters (LS1, and LS2).
3). LS1 generates 2 signals, DH and DL, to trigger Timing Shifter 1 and 2, respectively. Two corre-

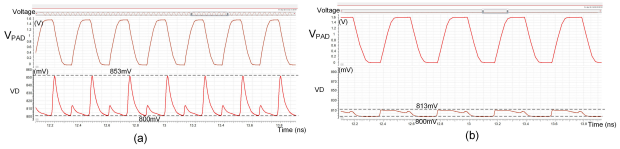


Fig. 2. Gate drive of $MP_2$ (a) without; (b) with $C_{\mathrm{VD}}$

sponding timing signals, D1 and D2, are then delivered to Digital Coder to carry out the generationg of timing control signals for Output Stage.

4). Digital Coder is the brain of the entire design, which is digital encoder to realize a function table between inputs, including PS, PF, NS, NF, OEH, OE, D1, D2, and outputs, including $\mathrm{V_{gp1}}, \mathrm{V_{gp2}}, \mathrm{V_{gp3}}, \mathrm{V_{gn1}}, \mathrm{V_{gn2}}, \mathrm{V_{gn3}}$.

Apparently, many blocks in Fig. 1 can be realized by existing circuits, e.g., UP and DOWN Gate Drivers, Digital Coder, and Floating N-well circuit, such that they will not be addressed due to the page limit required by the conference. By contrast, the details of driving transtors, Timing Shifter, and PVT detectors, will be disclosed.

### A. Selection of driving transistors

Referring to Fig. 1 again, a stacked MOS string is composed of $\mathrm{MP_{1a}}$, $\mathrm{MP_2}$, $\mathrm{MN_2}$, and $\mathrm{MN_{1a}}$ to spread the voltage overstress over the transistors on the same path when the external VDD is over the internal VDD, namely $2\times$VDD. $\mathrm{MP_{1b}}$, $\mathrm{MP_{1c}}$ are driving transistors to be turned on if necessary. That is, certain PVT corners are detected such that we need to increase the driving current as well as the rising edge's SR. By contrast, $\mathrm{MN_{1b}}$, $\mathrm{MN_{1c}}$ are those corresponding driving transistors for sinking more current to increase the falling edge's SR.

As mentioned earlier, FinFET device is phsyically different from planar devices. Particularly, the current is proportional to the number of FINs instead of arbitray channel width. Thus, it is found out that those devices in the stacked structure are better always on to prevent from severe fluctuation of output current magnitude. We propose to use FinFET with low Vth for those devices in this always-on path. In contrast, those auxiliary transistors are realized with high Vth devices to reduce the possible leakage when they are not activated.

Another long ignored issue is the stability of gate drives of those awlays-on devices. $\mathrm{MN_2}$ is kept on by Internal VDD, which is assumed to be highly stable. $\mathrm{MP_{1a}}$ and $\mathrm{MN_{1a}}$ are driven by UP Gate Drivers, respectively, which depends on the outcome of PVT detections. The only one left is $\mathrm{MP_2}$. The gate drive of this transistor depends on VD, which is the output of External VDD Detector. It highly depends on the stability of this sub-circuit. Thus, we tend to add a capacitor, $\mathrm{C_{VD}}$ to reject the noise coupled from External VDD Detector. With reference to Fig. 2 (a) and (b), the stability of $\mathrm{MP_2}$ gate drive is significantly enhanced.

### B. Timing Shifter

The reliability and robustness of the proposed design not only reply on the timing generation of those gate drives for PMOS and NMOS driving transistors, the delay on the cirtical path is also severely affected by the timing control. Since the external VDD could be either the same of internal VDD or 2 times higher, two Timing Shiferts are needed to generate nonoverlapping signals. One is for the voltage range from GND to internal VDD, while the other one is for VD to External VDD, where VD is the reference voltage genetared by External VDD Detector. Referring to Fig. 3, it is the mentioned Timing Shifters. The feature of this circuit is that it is fully designed in transistor level, not traditional gate level design. Fig. 4 demonstrates the delay reduction contributed by the proposed design. 44 ps delay reduction between the top stripe (transistor level) and the bottom strip (gate level) is found, which is almost 25% faster.

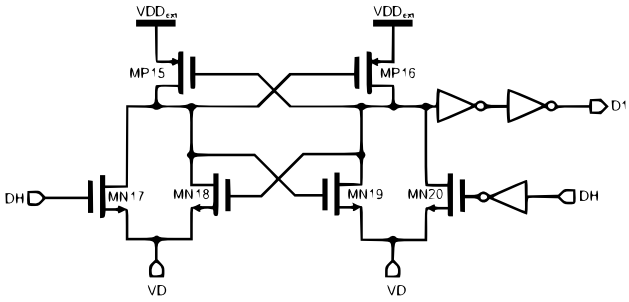


Fig. 3. Schematic of Timing Shifter

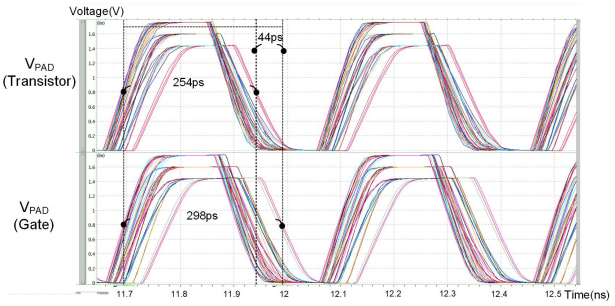


Fig. 4. Delay reduction by noneoverlapping signals

## III. Simulation and Verification

The proposed digital buffer is realized by TSMC 16 nm CMOS LOGIC Fin FET Compact (Shrink) LL ELK Cu 1P13M process. Fig. 5 shows the layout of an NMOS with multiple FINs. Referring to Fig. 6 (a) and (b), where the former is all-PVT-corner simulation outcome without PVT detection at 0.8 V power supply, where the SR is not adjusted at all. By contrast, the latter is the SR self-adjusted given that PVT detection is activated. As for the scenarios when external VDD = 1.6 V, SRs without and with PVT detection are demonstrated in Fig. 7 (a) and (b), respectively. The input load = 1 pF and the output load = 20 pF are used in all simulations. The all-PVT-corner simulations cover all the scenarios at the 75 corners composed of 5 process corners, 5 temperatures in the range of [0, 100]$^o$C, and 3 supply voltages from VDD$\times$0.9 to VDD$\times$1.1. The increase of the slew rate for External VDD = 0.8/1.6V is 18.0%(rising)/23.3%(falling)

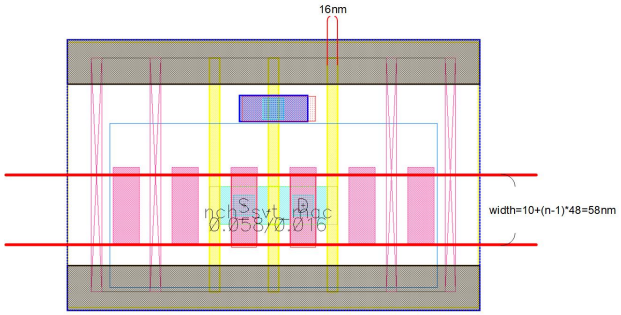


Fig. 5. Layout view of NMOS with multiple FINs

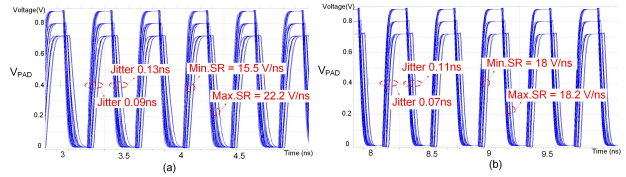


Fig. 6. Simulations given $VDD_{ext}$=0.8V (a) without ; (b) with PVT detection

and 10.0%(rising)/15.8%(falling), respectively, with and without the proposed PVT detection and self-adjustment are estimated. Regarding the maximum data rate, it is found to be 4.5/5.8 GHz given VDD=0.8/1.6V, respectively, with the activated proposed PVT detection and SR auto-adjustment. The slew rate is 18.0/19.0 V/ns given $VDD_{ext}$=0.8/1.6 V (worst case) and data rate = 2.5 GHz. Both the data rate and the slew rate are highly above the requirements of DDR4 specifications.

Table I summarizes the performance comparison with several existing works. Apparently, the proposed design provides an over 2.5 GHz all-corner-detected solution for 2×VDD data transmission with the best SR.

TABLE I
PERFORMANCE COMPARISON OF OUTPUT BUFFERS

| | [7] *ESSCIRC 2013* | [8] *ICICDT 2016* | [9] *TCAS-2 2017* | [10] *APCCAS 2018* | This work |
|---|---|---|---|---|---|
| CMOS (nm) | 28 | 28 | 40 | 40 | 16 |
| Verification | meas. | simu. | meas. | simu. | simu. |
| $VDD_{int}$(V) | 1.8 | 1.05 | 0.9 | 0.9 | 0.8 |
| $VDD_{ext}$(V) | 3.3-1.8 | 1.8/1.05 | 1.8/0.9 | 1.8/0.9 | 1.6/0.8 |
| Data (GHz) | 0.2 | 0.8 | 0.5 | 1.0 | 2.5 |
| SR (V/ns) | N/A | 3.9-4.9 | 1.54 | 6.0-6.5 | 18.0-19.1 |
| Loading (pF) | N/A | 20 | 20 | 20 | 20 |
| Power (mW) | 0.09 | N/A | 27 | 34.8 | 28 |
| @GHz | @ static | | 0.5 | 0.5 | 0.5 |

## IV. Conclusion

Aside from PVT detection, the proposed 2×VDD buffer featured with stabilizing gate drives of the driving transistors and transistor-level nonoverlapping signaling control is demonstrated. The SR improvement is estimated to be at least over 10% regardless in either voltage mode of data transmission mode. The most important of all is that this investigation demonstrates the wolrd first FinFET mixed-voltage output buffer design to achieve 2.5 GHz data rate.

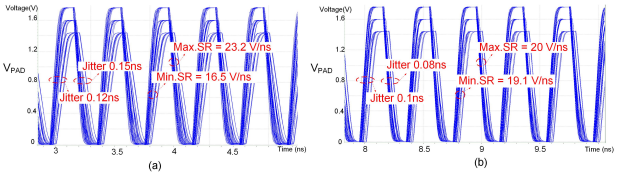


Fig. 7. Simulations given $VDD_{ext}$=1.6V (a) without ; (b) with PVT detection

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