A 1.5A 88.6% Li-ion Battery Charger Design Using Pulse Swallow Technique in Light Load

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***Abstract*—Traditional Li-ion battery chargers face a dilemma, which is the poor efficiency at a large charging current or vice versa. A pulse swallow technique is proposed in this investigation to resolve the mentioned problem. The proposed design carries out the automatic switching of PWM/PFM when the charging operation enters a light load scenario. When the battery voltage is close to the pre-defined full voltage, PFM strobes mask out the system clock to shut off power transistors to boost the efficiency. Post-layout simulations justify the proposed design generates 1.5 A current with 87.4% - 88.6% efficiency.**

Keywords— battery charger, PWM/PFM switching, constant current, constant voltage, high efficiency

I. Introduction

Batteries are an essential component of electrically-powered portable devices, e.g., tablets, cellular phones, etc. Besides reducing the power consumption to extend the operational time and life, the charging of the batteries is another critical issue. Fast charging of Li-ion batteries results in massive amount of heat and degradation of battery life owing to possibly poor efficiency, while slow charging is considered a waste of time. Li-ion batteries have been widely recognized as one of the best energy storage solutions to resolve the demand of light weight, long operation time, low cost for portable devices [1]. Thus, the charger solution for Li-ion batteries has attracted very intensive research efforts regardless in academia or in industry [2], [3], [4]. It is well known that the charger solutions are basically categorized into 2 types : LDO (low drop-out regulator), and switching mode. The former attains the advantages of simplicity at the penalty of poor efficiency. By contrast, the latter requires sophisticated circuit design to achieve high efficiency. Besides, the switching mode solution also provide very wide range of I/O voltage.

Given the high voltage (HV) CMOS processes, high voltage battery chargers capable of charging series connected batteries can be built using only integrated circuits and passive components. Basically, battery charger topologies used to charge series connected batteries can be classified in to three categories, including a bulk charger that charge all the batteries, a series of small chargers that independently charge their respective batteries, or a combination of both. To take full advantage of the wide voltage tolerance range offered by the available HV CMOS processes and the cost-effective feasibility, the bulk charger topology is selected as the major investigation of this research. This study is mainly focused on the design of the bulk charger, which is made capable of operating between constant current (CC) mode and constant voltage (CV) mode by pulse swallow method to achieve high efficiency in both light load and heavy load scenarios.

II. High Efficiency Charger Design Using Pulse Swallow Scheme

To achieve high efficiency and large output current, particularly balancing the efficiency between light load and heavy load during charging operation, the proposed charger consists of PWM (pulse width modulation) and PFM (pulse frequency modulation) schemes. The former is activated in the heavy load charging scenario, namely CC mode, while the later will be enabled in the light load scenario, i.e., CV mode. Notably, the switching of PWM and PFM is carried out by reliable logic circuitry to ensure the automatic selection such that the conversion loss is reduced and the average efficiency will be ensured.

With reference to Fig. 1, the proposed charger consists of CC Mode Control, CV Mode Control, Current Sensor, High/Low Level Shifter, Zero Current Detector (ZCD), Ramp & Clock Generator, and Nonoverlap circuits. The basic operation of the proposed charger is outlined by different modes : CC mode and CV mode.

a). CC mode : V_{sense} is generated by Current Sensor to compare with a pre-defined V_{limit} to drive the CC Mode Control path such that the constant charging is achieved. PWM is activated in this mode.

b). CV mode : By contrast, the CV Mode Control is activated by the comparison of battery voltage, V_{BAT}, and a pre-defined full voltage, V_{full}. PFM is then activated in this mode to maintain high efficiency.

A. CC mode operation

Referring to Fig. 2, the CC Mode Control in Fig. 1 is highlight in detail. An illustrative diagram is shown in Fig. 3, where the slew rate of V_{cc} is apparently changed by the cross of V_{sense} and V_{limit}.

(1). The comparison of V_{sense} and V_{limit} is carried out by Comp1 to generate a logic signal at the output.

(2). If $V_{sense} < V_{limit}$, the logic 1 at the output of Comp1 turns on sw1 such that I_B charges C_{cc}.

(3). V_{cc} at the top of C_{cc} ramps up slowly to compare with V_{ramp} by Comp2.

(4). If $V_{sense} > V_{limit}$, the logic 0 at the output of Comp1 turns on sw2 to discharge C_{cc}. Thus, the slew rate at V_{cc}

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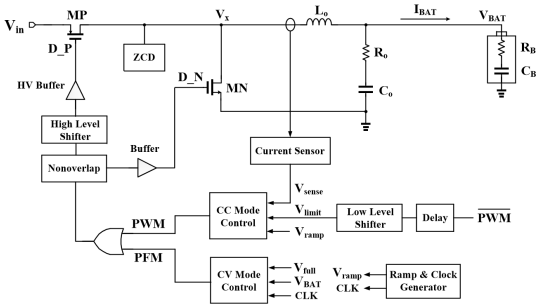

Fig. 1. System diagram of the proposed PWM/PFM charger design

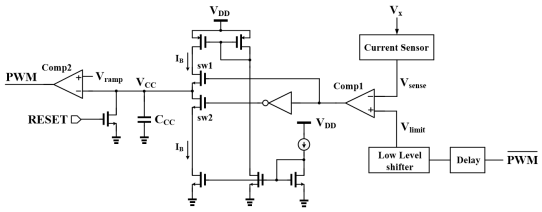

Fig. 2. CC mode control circuit

is reduced to change the duty cycle of PWM mode. The entire charger enters the CC mode.

B. CV mode operation

When the battery is charged close to the full voltage, the charger is considered to face a light load scenario. This is the reason why CV mode is widely used in such a scenario. However, the PWM will mask the CLK by the OR gate in Fig. 1 owing to that the duty cycle of CLK is very small in such a scenario. We need to mask out the PWM if the PFM is expected to be activated to keep the efficiency in the light load charging. Referring to Fig. 4, a simple solution is proposed to resolve the mentioned problem. Before V_{BAT} reaches V_{full}, Comp3 always generates logic low such that PFM = CLK. However, as soon as V_{BAT} = V_{full}, Comp3 sends a logic high to mask CLK by PFM. Thanks to the long duty cycle of high PFM

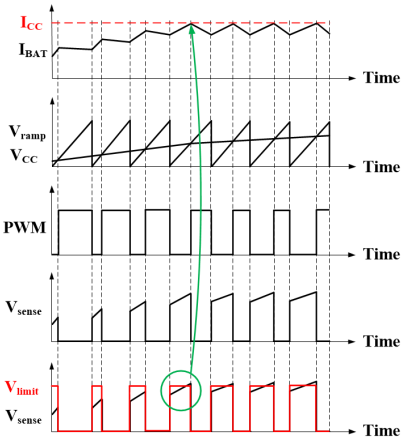

Fig. 3. Illustrative waveforms of CC mode control

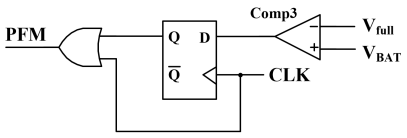

Fig. 4. CV mode control circuit

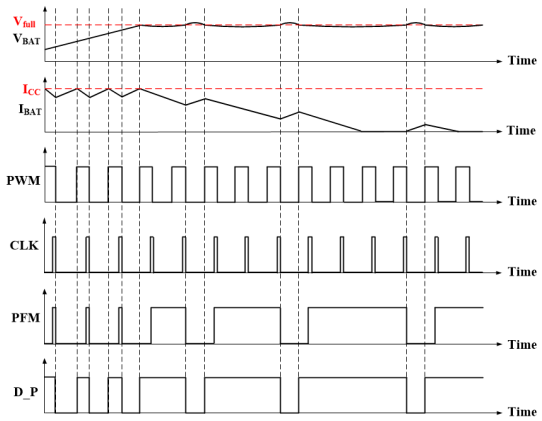

Fig. 5. Illustrative waveforms of CV mode control

signal, the power PMOS is shut off. Not only is CV mode entered, the loss is reduced to increase the efficiency. Fig. 5 demonstrates the CV timing diagram in this mode.

C. Supportive circuits

Besides the CC Model Control (PWM) and CV Mode Control (PFM), all of the supportive circuits in Fig. 1 are designed as follows.

1) current sensor: With reference to Fig. 6, even though a typical current mirror is used, the accuracy of current estimation is critical. M1, M2, M4 and MP, M3, M5 are matched current path except that the width ratio is K times for MP to M1. M1 and MP must be biased into linear region to equalize the voltage drop of S-D and S-G of the mirror pair. Meanwhile, I_{bias} must be very small with respect to I_L to prevent sinking too much current from the sensing path, namely MR and R_{sen}.

2) zero current detector, ZCD: To prevent any possible reverse current generated by the external inductor hitting the power NMOS resulting in the degradation of efficiency, a precise ZCD is required to detect the inductor current. That

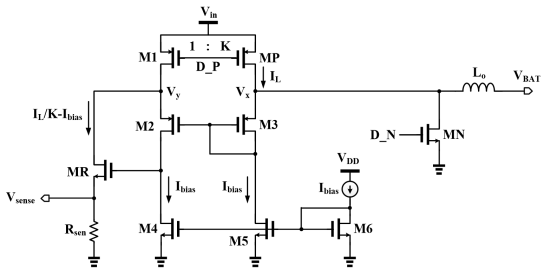

Fig. 6. Current sensor circuit

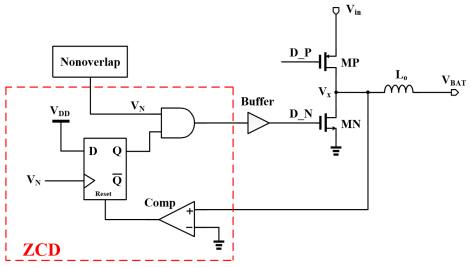

Fig. 7. Zero current detector

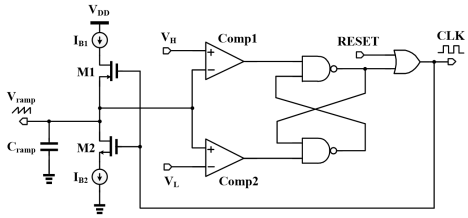

Fig. 8. Ramp & clock generator

is, as soon as the inductor current drops to zero, the power NMOS must be shut off immediately. Referring to Fig. 7, when V_x drops to ground, Comp generates a reset to clear the DFF in the lower left corner such that D_N is reset to turn off the power transistors. By contrast, if V_x stays above ground, D_N is normally activated.

3) ramp & clock generator: As stated earlier, a ramp signal is required for PWM/PFM control mechanism. Referring to Fig. 8, the current source, I_{B1}, charges C_{ramp} provided that M1 is initialized properly. As soon as V_{ramp} reaches V_H, namely a pre-defined high voltage, Comp1 generates logic low to pull up CLK. When CLK = 1, M2 is turned on to discharge C_{ramp}. When V_{ramp} at the top of C_{ramp} is as low as another pre-defined voltage level, V_L, Comp2 delivers a logic low to pull down CLK. The mentioned operation cycles are repeated to generate the ramp signal and CLK until the system is resent or stopped.

III. Simulation and Verification

The proposed design is realized by TSMC 500 nm HV (high voltage) CMOS process. The layout of the entire charger is shown in Fig. 9, where the core circuit area on silicon is 2332×3127 μm^2. Firstly, take the equivalent model of Li-ion battery, e.g., 18650 or 26650, as the load to run the simulation of the proposed charger design. Referring to Fig. 10, all of the TC, CC, CV modes are correctly switched such that the charging voltage of the battery, V_{BAT}, is very close to the ideal scenario.

The details of CC mode control is verified by Fig. 11, where PWM signal is generated by the voltage comparison of V_{CC} and V_{ramp}. Meanwhile, in the CC mode, D_P, which is the OR gate of PWM and PFM is the same as PWM signal such that the PWM control is selected as expected. Fig. 12 shows the scenario where V_{sense} crosses over V_{limit} to clamp the inductor current, I_{L0}.

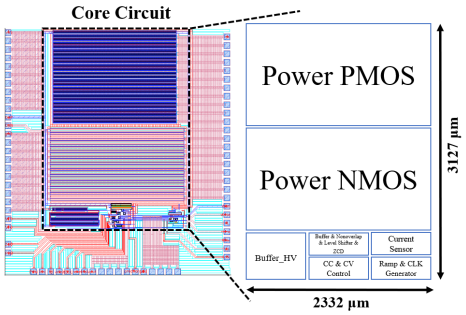

Fig. 9. Layout of the proposed charger design

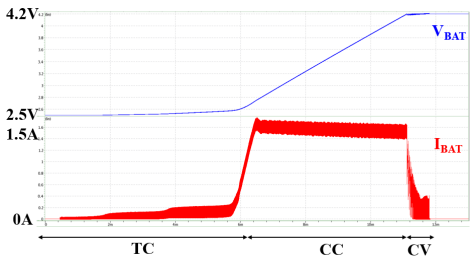

Fig. 10. Charging operation in 3 modes

When the battery voltage is close to V_{full}, the charger is expected to enter CV mode as addressed before. Fig. 13 shows the scenario when the charger enters the CV mode. Notably, since D_P is the OR function result of PWM and PFM, PWM is masked out as expected to achieve CV mode operation.

To ensure the functionality of the proposed charger in all possible situations, an all-PVT-corner simulation result is demonstrated in Fig. 14. Even in the worst SS case, the proposed charger still manages to provide over 1.5 A charging current.

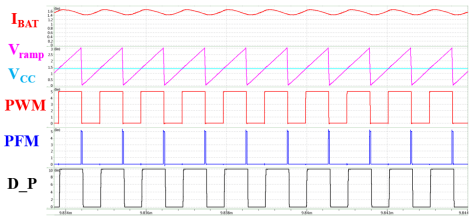

Fig. 11. CC mode simulation

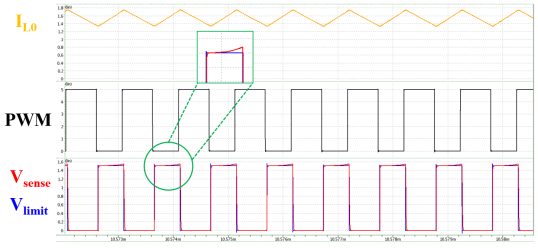

Fig. 12. Inductor current variation in CC mode

TABLE I
PERFORMANCE COMPARISON OF CHARGER DESIGNS

	[5] *MWCAS 2017*	[6] *JSSC 2014*	[7] *JSSC 2012*	[8] *EL 2017*	[9] *TCAS2 2017*	[10] *IE 2015*	This work
CMOS Tech. (μm)	0.35	0.25	0.18	0.18	0.13	0.18	0.5
charger type	switching	switching	switching	switching+LDO	LDO	LDO	switching
I/P range (V)	4.5-5.5	4.5-5.5	5.0-10.0	4.5-5.5	5.0	4.8-5.0	8.0-10.0
O/P range (V)	2.3-4.2	2.1-4.2	2.1-4.2	2.8-4.2	3.0-4.3	4.2	2.5-4.2
Max. I_{BAT} (A)	0.6	2	0.9	0.5	0.495	0.45	1.5
Peak eff. (%)	92.5	87 at 1A	86	87.6	83.9	83	87.4 (CC) 88.6 (CV)
Frequency (MHz)	0.7	0.5	2.2	2.5	N/A	N/A	1.0
FOM	55.5	87.0	77.4	43.8	41.53	37.35	131.1

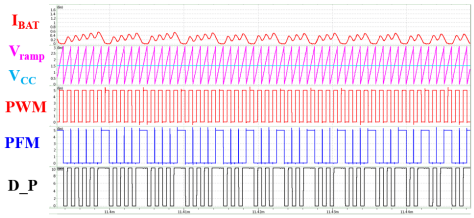

Fig. 13. CV mode simulation

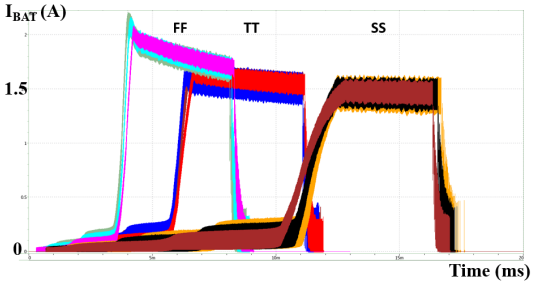

Fig. 14. All-PVT-corner simulation

Table I summarizes the comparison of our work with several recent CMOS charger designs. The major loss of the chargers is the conduction loss of power PMOS, which is defined by the following equation.

$$P_{cond,loss} = I_{rms}^2 \times R_{ds,on} \quad (1)$$

$$I_{rms} = \left[D \times (I_{BAT}^2 + \frac{I_{ripple}^2}{12}) \right]^{1/2} \quad (2)$$

Therefore, when the battery current increases, the conduction loss increases as well to decrease the efficiency. It is then easily to define an FOM (figure of merit) to tell the performance of the chargers as follows.

$$\text{FOM} = I_{BAT} \times \text{efficiency} \quad (3)$$

Apparently, our charger design attains the best FOM to date, since the largest current is provided at the second best efficiency.

IV. CONCLUSION

A novel pulse swallow technique is proposed in this investigation to carry out the automatic switching of PWM/PFM when the charging operation enters a light load scenario. Particularly, when the battery voltage is close to the pre-defined full voltage, PFM strobes mask out the system clock to shut off power transistors to boost the efficiency and still generate large charging current. Post-layout simulations justify that the proposed design is able to provide a solution of large charging current and high efficiency at the same time.

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