High Efficiency Buck Converter with Wide Load Current Range Using Dual-mode of PWM and PSM

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***Abstract*—This paper presents a high efficiency buck converter with wide load current range. To improve the efficiency in wide load current range, the dual-mode of PWM and PSM is utilized. The proposed design is implemented with a typical 0.35 μm CMOS process. The peak efficiency is simulated to be 96.76% at load current of 1000 mA. Moreover, the efficiency is higher than 94.80% at the wide load current range from 10 mA to 1000 mA. Besides, the proposed design is switched smoothly between PWM and PSM by effective and reliable control logic circuit.**

Keywords— buck converter, high efficiency, wide load current range, PWM, PSM

I. Introduction

With the arisen applications of IoT (Intelligence-of-things), portable devices, and Li-ion battery, DC/DC converter IC becomes very important. To save the energy, the high efficiency is required for DC/DC converter design in wide load current range. Due to the energy waste in the long conduction time, traditional PWM control does not have benefit in the light load scenario. Thus, dual-mode control is popular for the solution of high efficiency in wide range load current [1]- [9].

There are several modulation methods could save the energy in the light load, e.g., PFM (Pulse frequency modulation), COT (Constant on-time), and PSM (Pulse skip modulation). PFM are widely used for resolving the light-load efficiency problem in the dual-mode control [1], [2]. However, it requires the inductor current and the output voltage to control the switching, which needs complex control circuit. Besides, the frequency varies dramatically with the variation of the load current to cause EMI issue. COT has EMI issue as well.

PSM could reduce the conduction time of the power MOS transistor with a constant frequency. Thus, the efficiency problem in light load and the EMI issue are resolved. However, the control circuit is still complicated in the state-of-the-art [3]-[5].

Therefore, this study proposes a dual-mode PWM/PSM buck converter to achieve high efficiency in the wide load current range. Besides, the control circuit is carried out by logic circuit which is more reliable than the traditional designs.

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II. High Efficiency Buck Converter with Wide Load Current Range

Fig. 1 reveals the schematic of the proposed high efficiency buck converter, which is composed of a PSM Mode Controller, a PWM Mode Controller, a Soft-start Circuit, a Current Sensor, a Logic Control circuit, a zero current detector (ZCD), and a Driver. Soft-start Circuit provides a control signal, V_{SOFT}, to avoid the dramatic surge when the power is turned on initially. Thus, the overshoot is limited to the tolerant voltage, 5 V, to prevent damage. Current Sensor detects the inductor current by using a voltage drop of the small off-chip resistor, R_{SEN}. The terminal voltages of R_{SEN}, V_{SEN} and V_{OUT}, are sent to the Current Sensor. It generates the sensed signal, V_{SENI}, which is compared with a reference voltage, V_{SENREF}. The compared result, V_{ICMP}, is coupled to the Logic Control circuit. PWM and PSM Mode controllers generate the modulation signals, V_{PWM} and V_{PSM}, for heavy load and light load, respectively. Logic Control circuit generates the driving signal, V_{DRIVE}, according to the signals, ICSOFT, V_{SOFT}, V_{ICMP}, V_{PWM} and V_{PSM}. The Driver generates the control signals, V_H and V_L, for the on-chip power MOS transistors, M_P and M_N, respectively. V_H and V_L are nonoverlapping signals to enhance the efficiency. V_L would be pulled down to turn off M_N when the zero current is detected by the ZCD.

Fig. 2 shows the illustrative waveforms of the proposed PWM and PSM dual-mode buck converter. The compensated signal, V_{EA}, is compared with the ramp signal, V_{RAMP}, which is generated by the ramp generator (Ramp Gen.), referring to Fig. 1. When $V_{RAMP} > V_{EA}$, the logic high of V_{COMP} is obtained to reset Latch1. It generates the logic high of V_{PWM}, which is coupled to the Q_B node of Latch1. When the periodic pulse, CLK, is arrived, Latch1 is set such that V_{PWM} is pulled low. Thus, the width of V_{PWM} is varied according to the feedback signal, V_{FB}, and the output signal, V_{OUT}.

Referring to Fig. 1, the feedback signal, V_{FB} is also compared with the reference voltages V_{H1} and V_{L1} by the window comparators, CMP1 and CMP2. When $V_{FB} > V_{H1}$, the reset signal V_{R1} is high such that V_{Q1} and V_{Q2} are logic 1. The PSM signal keeps logic 1 by the V_{Q2} and the OR gate. Thus, the PSM signal, V_{PSM}, is skipped and the efficiency is improved provided that the output voltage is too high. The

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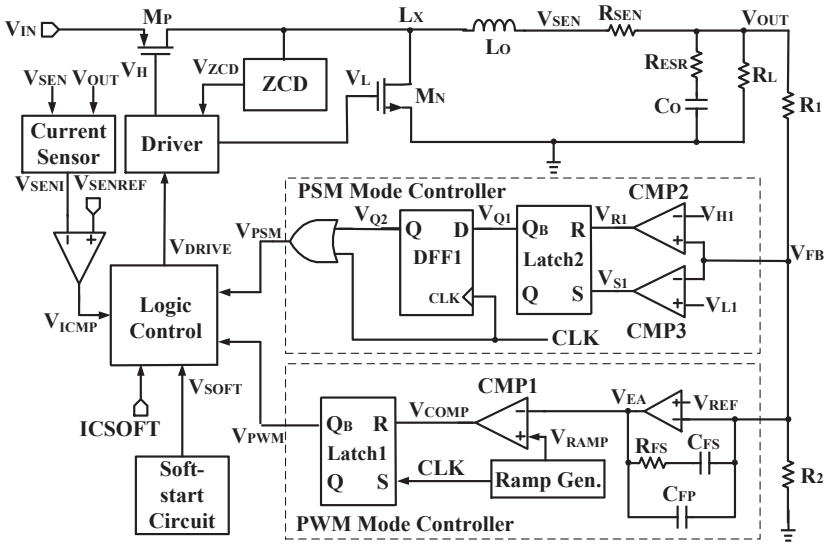

Fig. 1. Block diagram of the proposed buck converter.

operation sequence is expressed as follows.

$$V_{FB} > V_{H1} \rightarrow V_{R1} = \text{pulse 1 (Reset)} \rightarrow V_{Q1} = 1 \rightarrow V_{Q1} = 1 \rightarrow V_{PSM} = 1 \text{ (Skip)}. \quad (1)$$

When $V_{FB} < V_{L1}$, V_{Q2} are logic 0. Thus, V_{PSM} is equal to CLK by the OR gate to drive the power MOS transistors in light load.

$$V_{FB} < V_{L1} \rightarrow V_{S1} = \text{pulse 1 (Set)} \rightarrow V_{Q1} = 0 \rightarrow V_{Q1} = 0 \rightarrow V_{PSM} = \text{CLK}. \quad (2)$$

Fig. 3 shows the schematic of Logic Control circuit. The Logic Control circuit determine the driving signal, V_{DRIVE}, by using very simple logic of only 2 AND gates, 3 OR gates and 1 NOT gate. Referring to Table I, when ICSOFT is logic 0, the circuit is in the start-up mode. The driving signal, V_{DRIVE}, equals to the automatic soft-start signal, V_{SOFT}. When ICSOFT is logic 1, the circuit enters the normal mode. When $V_{SENI} > V_{SENREF}$, the buck converter faces the heavy load, V_{ICMP} is logic 0. V_{PWMO} and V_{DRIVE} equals to V_{PWM}, as shown in Fig. 2. When $V_{SENI} < V_{SENREF}$, the buck converter is in the light load, V_{PSMO} and V_{DRIVE} equals to V_{PSM}, Thus, the smooth switching between PWM and PSM modes are completed by comparing the current detecting signal, V_{SENI}, and the reference signal, V_{SENREF}, as shown in Fig. 2.

TABLE I
TRUTH TABLE OF THE PROPOSED LOGIC CONTROL CIRCUIT.

ICSOFT	Condition	V_{ICMP}	V_{G1}	V_{G2}	V_{DRIVE}
0	x	x	V_{SOFT}	0	V_{SOFT}
1	$V_{SENI} > V_{SENREF}$	0	V_{PWM}	0	V_{PWM}
1	$V_{SENI} < V_{SENREF}$	1	V_{PWM}	1	V_{PSM}

Fig. 4 shows the schematic of the ramp generator. C_R is charged and discharged by M_{PA} and M_{NB}, respectively. The

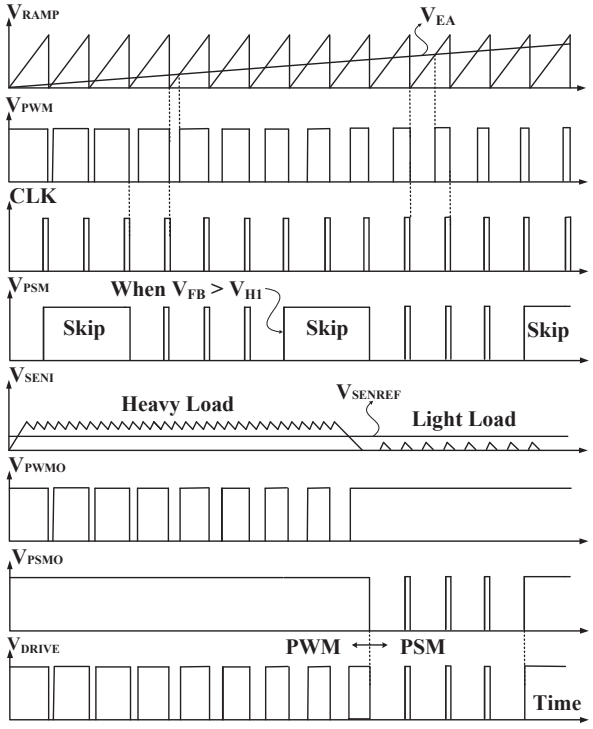

Fig. 2. Illustrative waveforms of the proposed high efficiency buck converter with dual-mode of PWM/PSM.

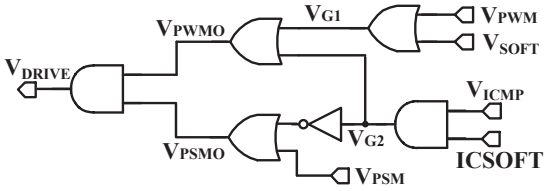

Fig. 3. Schematic of the Logic Control circuit.

ramp signal, V_{RAMP}, is compared by the window comparators, CMP4 and CMP5, to generate the set and reset signals for Latch3. Thus, the periodic pulse signal, CLK, is generated. Besides, CLK is feedback to control the charge and discharge paths for V_{RAMP}.

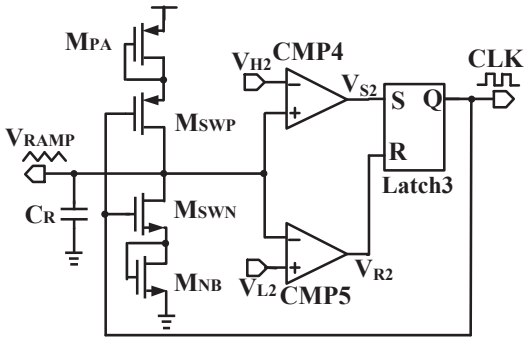

Fig. 4. Schematic of the ramp generator (Ramp Gen.).

Fig. 5 reveals the schematic of the ZCD and the Driver. When the inductor node signal, Lx, is smaller than 0 V, a CLR signal is generated to reset DFF2. Thus, V_{ZCD} becomes logic 0 to pull V_L down such that the power MOS, M_N, is turned off to avoid the large leakage current. Besides, V_L and V_H are nonoverlapping to improve the efficiency.

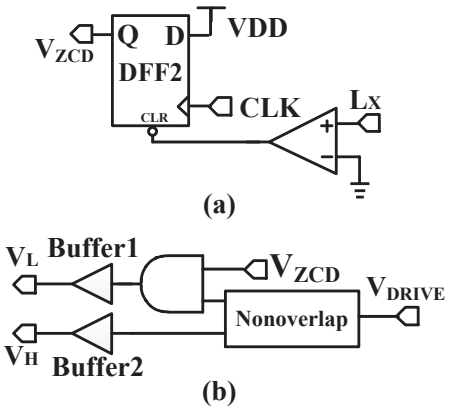

Fig. 5. Schematic of (a) the zero current detector (ZCD) and; (b) the Driver.

III. Implementation and Simulation Results

The proposed design is implemented using a typical 0.35 μm CMOS process. Fig. 6 shows the layout of the design, where the area is 1732 $\times$ 1415 μm^2. The threshold of the switching of PWM and PSM is set to 100 mA by choosing the value of V_{SENREF}. Fig. 7 and Fig. 8 show the worst-case simulation results of the load regulation for load current step of 100 mA and 990 mA, respectively. Referring to Fig. 7, when the load current is varied from 500 mA to 600 mA, the buck converter is operated in PWM mode and V_{OUT} is very stable against the variation of the load current. Referring

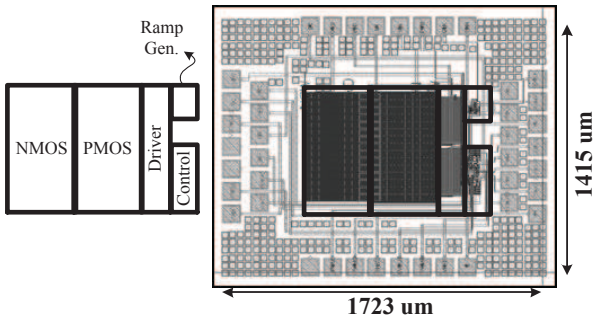

Fig. 6. Layout of the proposed design.

to Fig. 8 for the largest current change from 10 mA to 1 A of the load current, V_{ICMP} becomes from logic 1 to logic 0 to indicate the operation mode is moved from PSM to PWM mode, respectively. V_{OUT} is pulled back to the stable voltage in 380 μs. Fig. 9 shows the simulation results of the line regulation for V_{IN} from 4.5 V to 5 V. The overshoot and undershoot of V_{OUT} is 2.59 V and 2.35 V, respectively. Fig. 10 shows the simulated efficiency for V_{IN} of 3 V and 5 V. The peak efficiency is 96.76% for V_{IN} at 3 V at the load current of 1 A. Moreover, the efficiency is greater than 94.80% for the load current range from 10 mA to 1 A. Table II summarizes the performance comparison with several prior works. The proposed design possesses the best efficiency in the wide load current range.

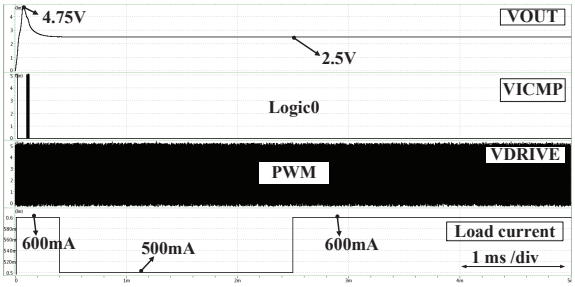

Fig. 7. Simulated waveforms of the load regulation with the load current varied from 500 mA to 600 mA.

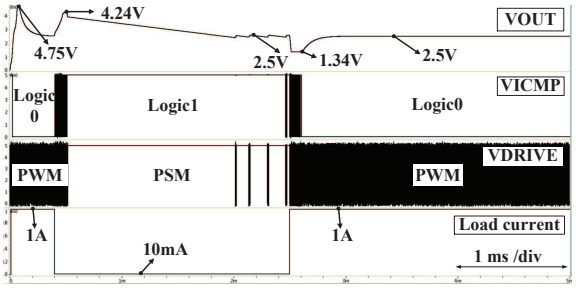

Fig. 8. Simulated waveforms of the load regulation with the load current varied from 10 mA to 1 A.

TABLE II
COMPARISON WITH SEVERAL PRIOR WORKS

	This work	[5]	[6]	[7]	[8]	[9]
Year	2018	2014	2014	2016	2014	2018
Publication	ISCAS	AICSP	TIE	ICICDT	JSSC	TVLSI
Process (nm)	350	180	500	65	40	350
Switching Freq. (MHz)	1.0	3	1.69	0.1-1.0	0.1	1.0
L (uH)	4.7	1	2.2	10	220	4.7
C (uF)	10	10	22	6.8	0.167	4.7
Input voltage (V)	3.0-5.0	2.8-5.5	2.7-5.5	1.5-3.6	0.6-1.1	0.55-1.8
Output voltage (V)	2.25-2.75	1.2	0.6-5.5	1.5	0.3-0.55	0.3-0.55
Max. Output current (A)	1.0	1.2	0.6	0.5	0.01	0.003
Output current range (mA)	10-1000	150-1200	5-600	2-500	0.05-10	0.001-3
Peak/worst efficiency	96.76%/94.8%	93%/76%	94%/79%	96%/85%	94%/50%	90.5%/67%
Core area (mm^2)	2.438	1.04	1.02	N/A	0.675	1.12
Modes	PWM/PSM	PWM/PSM	PWM/Standby	PWM/PFM	CCM/DCM	DPWM/PPFM
Control circuit	3OR,2AND, 1NOT	2Counter, 3DFF,3OR	N/A	Counter, Mux, Latch, logic	2Pulse Conv., Latch, 1NOT, 2Buf	2DFF, 2AND, 1NOT
FOM¶	948.2	887.3	514.7	450.7	7.2	2.4

Note: ¶ FOM = (Load current range)× [(Max. eff.+ min. eff.)/2].

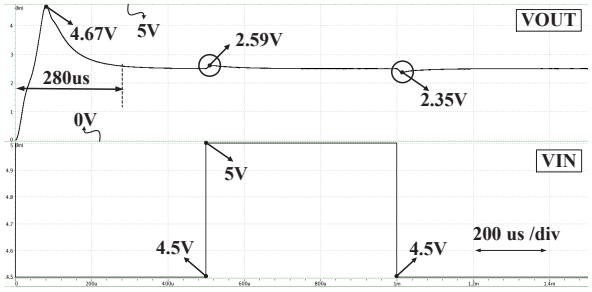

Fig. 9. Simulated waveforms of the line regulation with the input voltage varied from 4.5 V to 5 V.

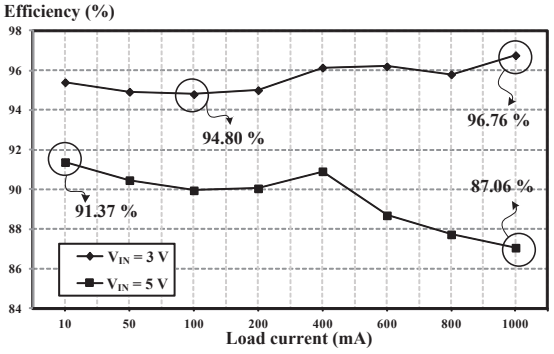

Fig. 10. Simulated efficiency of the proposed design with the input voltage at 3 V and 5 V, respectively.

IV. CONCLUSION

This paper proposes the high efficiency buck converter. Based on the simulation results, the converter possesses the high efficiency $> 94.8\%$ in the wide load current range from 10 mA to 1 A because of the effective PWM/PSM dual-mode control. Moreover, the peak efficiency is 96.76% at the maximum load current of 1 A. Compared to the prior works, which could not achieve the peak efficiency at the maximum load current, our design resolves this dilemma. Besides, the control circuit is much simpler than that of those prior works.

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