A Robust Time-to-Digital Converter Design with High Precision for Underwater Vehicle System Clock Synchronization and Sensing

Pang-Yen Lou, Kuan-Yu Chao, and Chua-Chin Wang† , *IEEE Senior Member*
Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

Abstract -- **This paper presents a robust time-to-digital converter (TDC) design insensitive to the hostile environment in underwater vehicles. Particularly, the proposed TDC is insensitive to process, voltage of supply, and temperature (PVT) variations existing in the noisy and unstable environment such that it is very critical to the synchronization of clocks among different electronic modules. Without a robust synchronized clock, the integrity of digital signals over the wireline for data communication and information exchange will be in danger. The proposed design is proved to attain the lowest power dissipation, <0.7 mW, and the least INL/DNL, < 0.5 LSB, even in the worst case according to all-corner simulation results.**

I. Introduction

System reliability as well as the safety are deemed as the top priority for any underwater vehicle (UWV), regardless manned-operated or autonomous types, e.g., ROV (Remotely Operated Vehicle), AUV (Autonomous Underwater Vehicle), FITS (Fiber optical Instrumentation Towed System), where an ROV developed by NSYSU and NCKU is shown in Fig. 1. Apparently, a reliable communication system with robust protocol is the key to the success of this kind of underwater systems. For example, with reference to Fig. 2, where a generic communication networking architecture is disclosed, the synchronization of the clocks of each block is the fundamental requirement for these blocks to exchange information, requests, and commands reliably. Thus, the receiver (Rx) of the connection port of each block needs to be equipped a circuit to find out the phase difference between the local clock and the global clock over the backbone. TDC (time-to-digital converter) is deemed as one of the best solutions for this demand, which converts the difference in time domain into digital codes such that the following CDR (clock and data recovery) circuit is able to adjust the phase and frequency to achieve synchronization.

Besides the synchronization of clocks among different blocks, TDC is also applied to the remote measurement of distance, e.g., altimeter and rangefinder, which are also critical sensors for UWVs. Another design constraint of TDC for UWVs is the power dissipation. Since the UWVs are all powered by batteries and all of the circuits are sealed in containers, the power dissipation must be as low as possible such that the battery operation time will not be reduced and the generation of unwanted heat will be diminished. However, these design considerations have not been seriously discussed in existing solutions.

In this study, we present a TDC design solution to resolve all of the mentioned problems without severe sacrifice of accuracy and complexity. By contrast, the simulations against the worst design conditions justify the robustness in the applications of UWVs.

Fig. 1. The photo of an ROV [1]

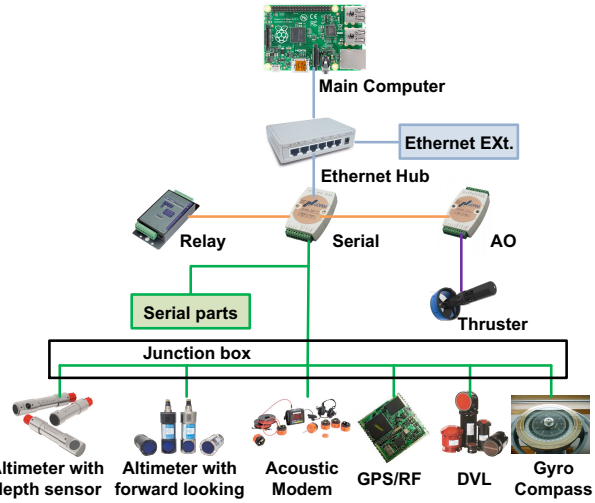

Fig. 2. Generic networking architecture in UWVs [2]

II. TDC Circuit Design

Traditional TDC is mainly composed of cascaded delay elements such that the resolution is 1 LSB (least significant bit) theoretically. However, the delay of these delay elements is seriously affected by many environment factors, particularly process, voltage supply, and temperature, namely PVT variations. The consequence of the delay drift caused by PVT variations poses impact on the accuracy of the delay between

† Prof. Chua -Chin Wang is the contact author.

two adjacent cells, which is also called phase shift. Thus, a TDC driven by a PVT Detector is proposed to resolve this problem as shown in Fig. 3.

A. Time-to-Digital Converter

The schematic of TDC in Fig. 3 is shown in Fig. 4. "start" is coupled to the input and then the rising edge thereof will be delayed to approach "stop". As soon as "start" passes or catches up with "stop", the output of the corresponding DFF is pulled up "1". If not, the output stays as "0". Therefore, the outputs of all the DFFs consist of a thermometer code, which will be converted into a binary code of the following encoder in Fig. 3. An illustrative timing diagram is revealed in Fig. 5.

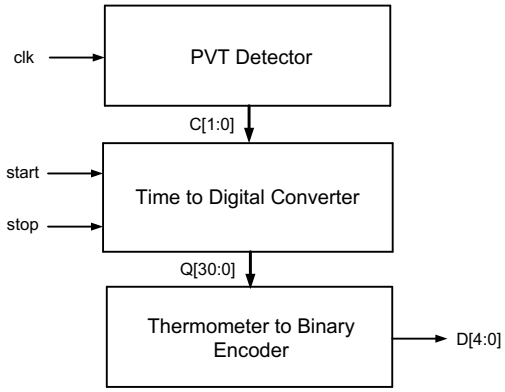

Fig. 3. The proposed TDC design

Assume the resolution of each delay element is τ_1. If the interval between "start" and "stop" is T. The length of the thermometer code is N.

$$T = N\tau_1 + \varepsilon \quad (1)$$

where ε is the quantization error. If there is a total of *n* delay elements, the dynamic range, DR = n τ_1. In this investigation, τ_1 = 18.7 ps, *n* = 31, DR = 579.7 ps, and the binary output code length is 5.

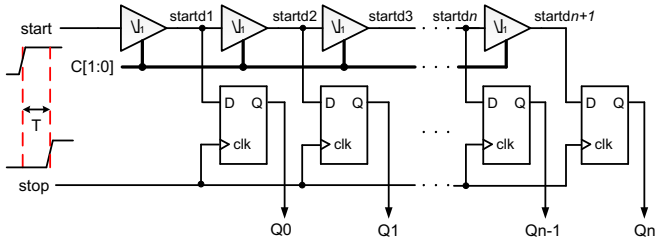

Fig. 4. The schematic of the TDC block.

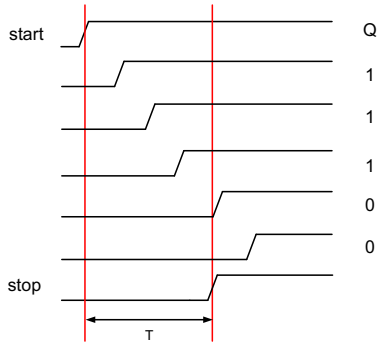

Fig. 5. Illustrative timing diagram of the TDC block..

B. PVT Detector

Referring to Fig. 6, the PVT detector looks very similar to a TDC. However, the difference is that PVT detector take advantage of the clock falling edge to trigger and lock the DFFs such that the "delayed" rising edge will be caught in certain DFFs, as shown in Fig. 7. Since the PVT detector is also unavoidably affected by PVT variations, the rising edge would be locked in different situations. For instance, the rising edge will be latched earlier in "Fast" scenarios, and later in "Slow" scenarios, as shown in Fig. 8. In this study, a total o 31 stages are used, where the 24th stage and 29th stage are respectively selected as the generated PVT codes. The reason is that they are the head and tail of the last quarter of the entire delay chain so that they have the most possible diversion spread in time domain.

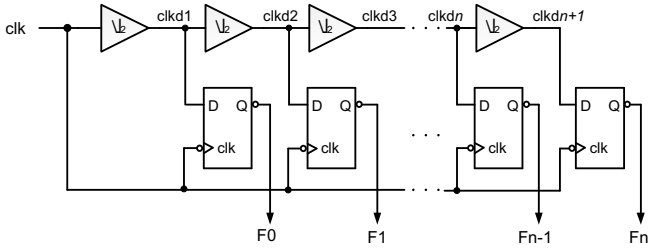

Fig. 6. PVT detector

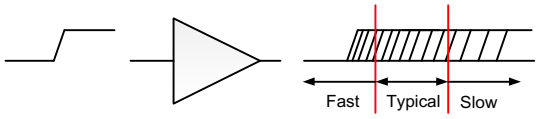

Fig. 7. Possible delay scenarios of a single delay element

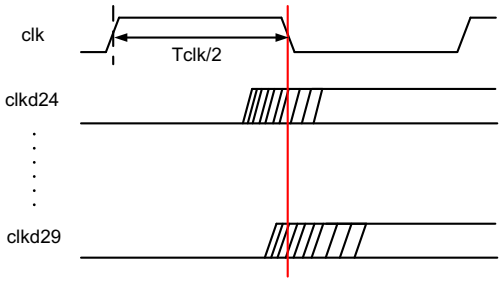

Fig. 8. Locking of the 24th and 29th rising edges

As a consequence, the PVT condition can be determined by the following outcome in Table 1.

Table 1 : Code Table of The PVT Detector

PVT code	O/P of 29th stage = C[1]	O/P of 24th stage = C[0]
Slow	1	1
Typical	1	0
Fast	0	0

The generated PVT code, namely C[1] and C[0], are coupled to the delay elements in Fig. 4. The PVT code then adjusts the current sinking capability in Fig. 9.

- Slow (C[1], C[0]) = (1, 1) : Mn3 and Mn4 are both turned on to assist Mn5 and fasten the current sinking such that the delay will be reduced.
- Typical (C[1], C[0]) = (1, 0) : Only Mn4 is on to help

Mn5 for the current sinking.

- Fast (C[1], C[0]) = (0, 0) : Mn5 is the only one left to sink the current such that the delay will be extended.

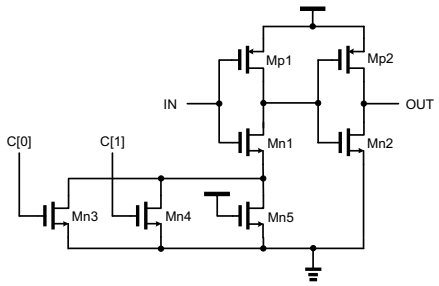

Fig. 9. Delay element in Fig. 4 with PVT code control

III. Implementation and Simulations

The proposed TDC is carried out by TSMC 90 nm CMOS technology. Fig. 10 demonstrated the transfer function of time vs. digital output code. Fig. 11 and Fig. 12 are the INL (integral non-linearity) and DNL (differential non-linearity) of the transfer functions, respectively, to justify the non-linearity error is very small, INL and DNL < 0.2 LSB.

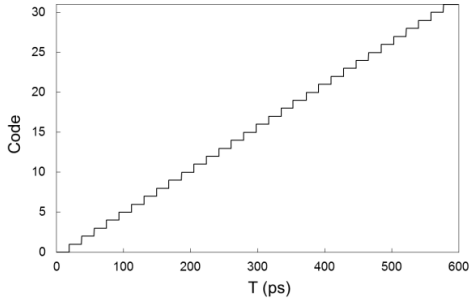

Fig. 10. Simulated transfer function : Time vs. Digital

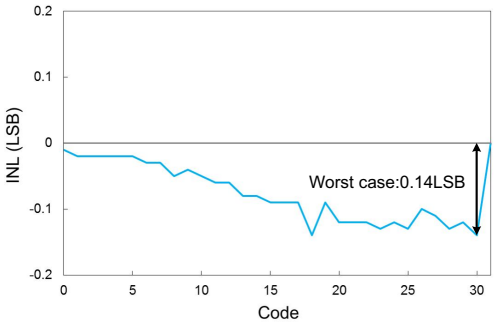

Fig. 11. INL of the proposed design

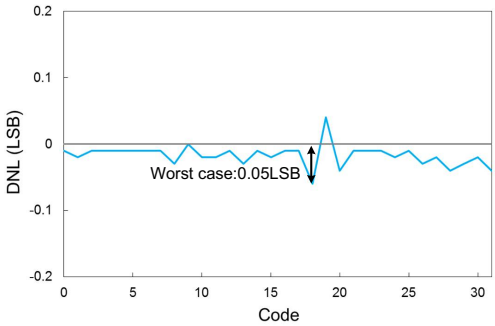

Fig. 12. DNL of the proposed design

The performance provided by the PVT detector is demonstrated by Fig. 13 and 14, where the difference between without PVT code adjustment and with PVT adjustment is very significant. The variation of the edge jitter is reduced from 11.4 ps to 5.91 ps, which ensures higher accuracy of clock synchronization and device sensing.

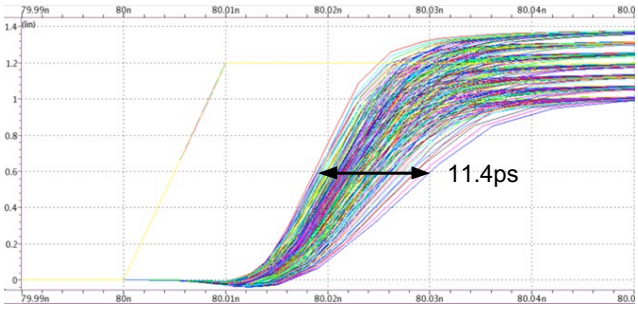

Fig. 13. Edge timing variation without PVT code control

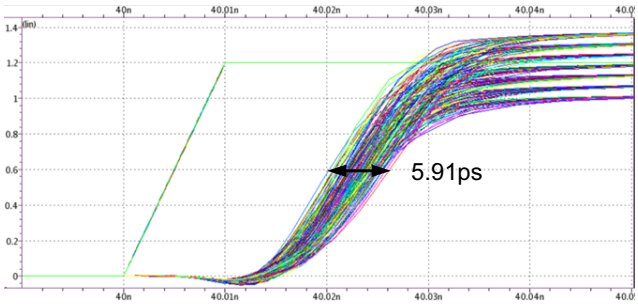

Fig. 9. Edge timing variation with PVT code control

To highlight the performance of the proposed TDC design, a comparison table between our design and several recent related works is tabulated in Table 2. The overall performance can be evaluated by the following FOM (figure of merit) . Not only our design attains the least error, but also demonstrates the best FOM among all of the TDC designs to date.

$$\text{FOM} = (|INL| + |DNL|) \times \text{power} \times \text{resolution} \qquad (2)$$

IV. Acknowledgement

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Table 2 : Performance Comparison

	2015 DDECS[3]	2015 ISSCS[4]	2016 ICCE[5]	2018 TCAS-II[6]	2018 MEJ[7]	This work
Architecture	PLL	2-Level Vernier	DLL	Ring OSC	Dual DLL	Tapper delay line
Process	180 nm	65 nm	65 nm	130 nm	180 nm	90 nm
Resolution	7.1 ps	6.15 ps	2 ps	43.2 ps	15 ps *	18.7 ps
Dynamic range	56.2 ns	1260 ps	1 us	n/a	500 ns	598.4 ps
Clock frequency	1.1 GHz	40 MHz	n/a	100 MHz	100 MHz	100 MHz
Power	120 mW	2.5 mW	69.7 mW	1.716mW *	75 mW	0.695 mW
INL	n/a	2 LSB	1 LSB	-2.5 LSB *	4 LSB *	0.14 LSB
DNL	n/a	1.2 LSB	1 LSB	-1 LSB *	1.7 LSB *	0.05 LSB
Delay variation	n/a	4 ps (0.65 LSB)	n/a	6.4 ps ^ (0.15 LSB)	10 ps (0.67 LSB)	5.91 ps (0.32 LSB)
FOM	n/a	0.049	0.279	0.26	6.413	0.003

$\text{FOM} = (|INL| + |DNL|) \times \text{power} \times \text{resolution}$

* Measurement

^ Measurement : $\frac{0.064\text{ps}}{℃} \times 100℃ = 6.4\ \text{ps}$