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40-nm 2×VDD Digital Output Buffer Design With DDR4-Compliant Slew Rate

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***Abstract*—A 2×VDD I/O buffer featured with PVT (process, voltage, temperature) corner detection and SR (slew rate) auto-compensation is proposed. Besides, a nonoverlap timing control is added to the gate drives of those large devices in the output stage such that the appearance of possible DC current spikes caused by simultaneous turn-on driving MOS transistors is prevented. Not only is the SR enhanced, the power dissipation is also reduced. The maximum data rate is 2.5/1.6 GHz given 0.9/1.8 V supply voltage with 20 pF load, respectively, by all-PVT-corner simulations. The Δ SR improvement is 31.9%(rising)/48.9%(falling) and 26.0%(rising)/41.0%(falling) for 1×VDD and 2×VDD, respectively, when the proposed PVT auto-compensation design is activated.**

Keywords— I/O buffer, PVT variation, mixed-voltage tolerant, slew rate compensation, nonoverlap timing control

I. Introduction

The benefits of the advanced CMOS technologies are low supply voltage, low fabrication cost per area, low power consumption, and high speed. However, many PCB-based applications still need high-power or high voltage drivers. Therefore, mixed-voltage I/O buffer is welcomed to carry out data exchange with different voltage between separate chips [1]- [4], since these chips are not ensured to be fabricated by the same CMOS process. That is, when a PCB-based system is equipped with chips fabricated by different generations of CMOS process, which might use different digital voltage levels, e.g., 1.8 V vs. 3.3 V. Notably, the slew rate (SR) becomes the major issue for digital transmission. For instance, the DDR4 protocol demands the range of SR is min. = 4 V/ns to max. = 9 V/ns given 1.6 GHz data rate. If the SR is too large, the SSN (simultaneous switching noise) will be very serious to jeopardize the signal integrity. By contrast, if the SR is too small, the time margin will become an issue to latch digital signals [5]. Such a harsh SR requirement is now recognized as one of the critical bottlenecks of mixed-voltage I/O buffer design. Apparently, the reason is the severe SR variation caused by various PVT (process, supply voltage, temperature) scenarios. What even make the SR requirement hard to be compliant is the leakage issue when advanced nanometer CMOS process is used for mixed-voltage I/O buffer design, which is also referred as PVTL variation in many prior reports. Although many researchers have proposed PVT compensation methods for the mixed-voltage I/O buffers to auto-adjust the SR corresponding to the PVT corners, e.g., [6], [7], most of these PVT detection circuits detect only three process corners, namely typical-typical (TT), fast-fast (FF), and slow-slow (SS) [6]. Another reported method may cause long settling time and missing code resulting poor SR in high frequency operations due to the request of multiple clock cycles [7]. In short, most of the proposed solutions were mainly based on stacked architecture and variation detectors to compensate SR and increase reliability, respectively, [8] - [13]. Another improved digital-based process detector was also reported to simplify the detection mechanism and increase the detection speed [14].

One of the long-ignored issues in the design of mixed-voltage I/O is the large DC current spike generated by the simultaneous turn-on scenario of those large driving MOS transistors in the output stage. Even though it is a short interval, the power and leakage are significant owing to the size of these transistor, which might be over 10,000 μm to provide a large current. Not only these current spikes waste lots of power, they also bring impact to the signal integrity. The delay approach proposed in [15] might be helpful in certain cases, e.g., TT. However, the delay generated by those buffers is also affected by PVT variations as well. We, thus, propose a robust method to resolve this problem.

II. 2×VDD Output Buffer with Non-overlapping Timing Control

Referring to Fig. 1, the proposed output buffer consists of PVT detector, Floating N-well circuit, Voltage Level Converter (VLC), Pre-drivers, VDDIO detector, Nonoverlap generator, Digital logic circuit, Output stage, and Input stage. Notably, clock is the system clock, PAD is the I/O port coupled with the off-chip discrete, Din is the signal port coupled to the core logic of the chip, and Dout is the digital signal given by the internal core logic to be transmitted outward. The operation of the proposed design is outlined as follows.

1). clock drives PVT detector to generate P_{code}[2:1] and N_{code}[2:1] denoting the current PMOS and NMOS corners, respectively.
2). VDDIO detector is in charge of telling what voltage level VDDIO is now and then generate the VD to the following VLC and an output driving PMOS.
3). VLC generates 2 signals, D_H and D_L, to trigger Nonoverlap circuit 1 and 2, respectively. Consequently, 2 corresponding timing signals, D_1 and D_2, are delivered

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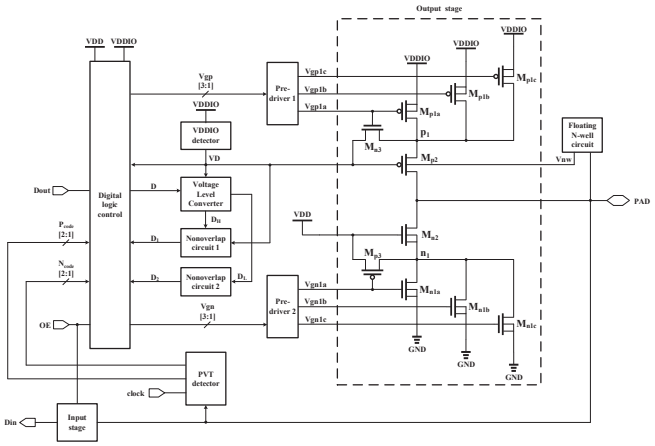

Fig. 1. Block diagram of the proposed 2×VDD digital output buffer.

to Digital logic circuit for the sake of driving transistors timing control.

4). The swing of the digital output is allowed to be 1×VDD or 2×VDD depending on the VDDIO in Output stage. Meanwhile, the on-off status of 6 driving PMOS transistors and 6 driving NMOS transistors is respectively determined by the digital outputs of Digital logic circuit and Pre-drivers such that the slew rate variation caused by various PVT corners is reduced significantly.

Many of the blocks in Fig. 1 are realized by well-known circuits, e.g., Digital logic circuit, VDDIO detector, VLC, Input stage, and Floating N-well circuit, which will not be addressed clearly in this investigation, since there is a page limitation. By contrast, the details of Nonoverlap generator with timing control, Output stage and PVT detector will be highlight in the following text.

A. Output stage

Referring to Fig. 1, a stacked MOS string is composed of M_{p1a}, M_{p2}, M_{n2}, and M_{n1a} to avoid the overstress problem when VDDIO is very high, namely 2×VDD. M_{p1b}, M_{p1c} are auxiliary PMOS driving transistors, which will be turned on if certain PVT corners are detected to increase the driving current as well is the SR of the rising edge. By contrast, M_{n1b}, M_{n1c} are those driving transistors for sinking more current and increasing the SR of the falling edge. To prevent the overstress during signal transitions provided that VDDIO = 2×VDD, the functionality of precharging devices, M_{p3} and M_{n3}, is very critical as follows.

• Dout = low → high : M_{n1a}, M_{n1b}, and M_{n1c} are all off. M_{p3} should be turned on firstly to precharge node n_1 to VDD such that the overstress hazard of M_{n2}, when voltage at PAD = 2×VDD and voltage at n_1 < VDD, is prevented. Meanwhile, PAD will be pre-charged to VDD-Vth such that the SR will be enhanced. After the precharging of M_{p3}, the three PMOS driving transistors, i.e., M_{p1a}, M_{p1b}, M_{p1c}, are then turned on to boost the voltage at PAD from VDD-Vth to 2×VDD.

• Dout = high → low : It is the opposite to the previous case. M_{p1a}, M_{p1b}, and M_{p1c} are all off in this case. Then, M_{n3} should be turned on firstly to discharge node p_1 to VDD. Therefore, M_{p2} will not be suffered from overstress even though PAD is ground and voltage at node p_1 is higher than VDD.

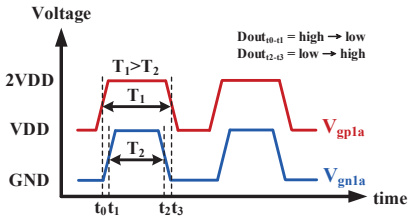

Fig. 2. Timing control of M_{p1a} and M_{n1a} gate drives

In summary, the required timing control of M_{p1a} and M_{n1a} gate drives to achieve that aforementioned operation is illustrated in Fig. 2

B. Nonoverlap generator circuit

As addressed in the previous section, the reliability of the proposed control scheme replies on the timing generation of those gate drives for the driving transistors. Since VDDIO could be either VDD or 2×VDD, 2 nonoverlapping signal generators as shown in Fig. 3. Notably, D_H and D_L are generated by VLC in Fig. 1, and coupled with the inputs of two identical nonoverlapping signal generators to generate D_1 and D_2, respectively. The only difference of these two nonoverlapping signal generators is the supply voltages, where the former is VDDIO, and the latter is VDD.

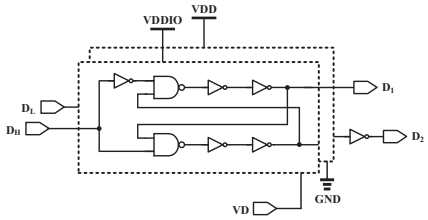

Fig. 3. Schematic of nonoverlapping signals generator

C. PVT detector

To find out all the five process corners, i.e., SF, SS, TT, FS, and FF, the detection of P-device and N-device must be separately carried out. Thus, P-corner detector and N-corner detector are demonstrated in Fig. 4 and 5. Both detectors consists of a low-skew inverter, a capacitor, two comparators, and D-type flip-flops (DFF). Notably, the pull-up transistor of the low-skew inverters is a long channel device such that the charging therein is much slower than the discharging.

Take the P-corner detector as the example to explain how it works. ”clock” is a pulse train with 50% duty cycle. At the falling edge of clock, the P-device starts to charge the capacitor. Since M_{p29} is a long-channel device, the P device variation

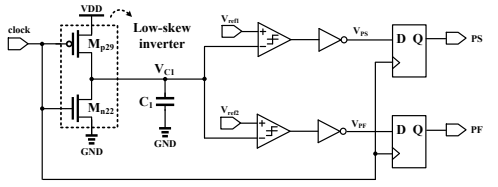

Fig. 4. Schematic of P-corner detector

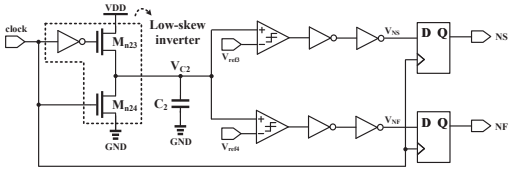

Fig. 5. Schematic of N-corner detector

will significantly impact the relative small charging current. Thus, V_{C1} will vary with the charging speed given a fixed time interval. The stabilized V_{C1} is then compared with V_{ref1} and V_{ref2}, where the outcomes are registered by DFFs as PF (P fast) and PS (P slow), respectively.

- If P device is at fast corner, the resistance of M_{p29} is dropped to fasten the charging and boost V_{C1}.
- If P device is at slow corner, the resistance becomes larger and V_{C1} drops consequently.

The above detection scenarios are demonstrated in Fig. 6. Apparently, the detection of N-device process corners is very similar to the above procedure. In short, the above scenarios are summarized in the following Table I.

TABLE I
FUNCTION TABLE OF PROCESS DETECTORS

P process detector			
	Vc1	PS	PF
Fast	Vc1 > V_{ref1}	Logic 1	Logic 1
Typical	V_{ref1} > Vc1 > V_{ref2}	Logic 0	Logic 1
Slow	V_{ref2} > Vc1	Logic 0	Logic 0
N process detector			
	Vc2	NS	NF
Fast	Vc2 > V_{ref3}	Logic 1	Logic 1
Typical	V_{ref3} > Vc2 > V_{ref4}	Logic 0	Logic 1
Slow	V_{ref4} > Vc2	Logic 0	Logic 0

Another important application of the P-corner detector and N-corner detector circuits can be used to detect high, normal, and low temperatures, as well as high VDD (10% VDD higher), VDD and low VDD (10% VDD lower). Therefore, the PVT detection is feasible by the proposed design.

III. Simulation and Verification

The proposed design is realized by TSMC 40 nm CMOS process. Referring to Fig. 7 and 8, where the former is all-corner simulation result without PVT compensation at VDDIO = 1.8 V and the latter is with compensation. Notably, the input load is 1 pF and the output load is 20 pF. The all-corner simulations are carried out at the 75 corners of [TT, SS, FF, SF, FS], [0, 25, 50, 75, 100]^{o}C, [VDD×0.9, VDD, VDD×1.1]. Fig. 9 and 10, by contrast, are the results of simulations at VDDIO = 0.9 V. Based upon these thorough simulations, the slew rate enhancement for VDDIO = 0.9/1.8 V is 31.9%(rising)/48.9%(falling) and 26.0%(rising)/41.0%(falling), respectively, with and without the proposed PVT compensation. The maximum data rate of the proposed design is measured to be 2.5/1.6 GHz given VDDIO=0.9/1.8 V, respectively, with the activated PVT compensation. The slew rate is estimated to be 6.91/7.85 V/ns at 20 pF loading given VDDIO=0.9/1.8 V. Both the data rate and the slew rate are compliant with the requirement of DDR4.

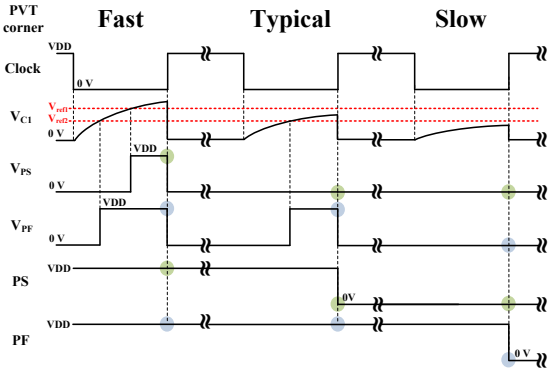

Fig. 6. Illustration of P-device process detection

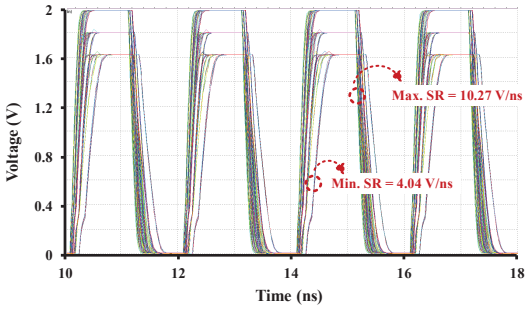

Fig. 7. All-PVT-corner simulations given 1.8 V without compensation

Table II summarizes the comparison of our work with several prior works. Apparently, the proposed design provides a high-speed all-corner-detected solution for 2×VDD data transmission with the best improvement on SR. Besides, the SR and the data rate of the proposed design meet the demand of DDR4.

IV. Conclusion

Besides PVT corner detection, the 2×VDD I/O buffer featured with nonoverlap timing control upon gate drives of the driving transistors is reported in this investigation. The SR improvement is proved to be at least over 26% regardless in VDD or 2×VDD data transmission mode. The power consumption is 33.71 mW at 500 MHz. Most important of all, the hazard of DC current spikes caused by simultaneous turn-on driving MOS transistors is prevented.

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TABLE II
PERFORMANCE COMPARISON OF OUTPUT BUFFERS

	[11] *TCAS-I 2013*	[12] *ISCAS 2013*	[13] *EDSSC 2014*	[14] *ISCAS 2016*	This work
Process (nm)	90	40	90	90	40
Implementation	measurement	measurement	simulation	simulation	simulation
VDD (V)	1.2	0.9	1.0	1.0	0.9
VDDIO (V)	2.5	0.9/1.8	1.0/1.8	1.0/2.0	0.9/1.8
Process Corner Detected	Only TT FF SS	All	All	All	All
Lock Time	One cycle	Tens of cycle	$\geq$ One cycle	One cycle	One cycle
Maximum Date Rate (MHz)	N/A	500/460	500/330	800/500	2500/1600
SR Range (V/ns)	2.2-3.4 (est.)	0.52-0.53	1.89-2.32	N/A	6.91-7.85
Loading (pF)	15	20	20	20	20
SR Variation Improvement (%)	37.5	8/6	24.5	33.9	37 (Average)
Core Area (mm^2)	N/A	0.052×0.254	0.056×0.439	0.052×0.388	0.063×0.232

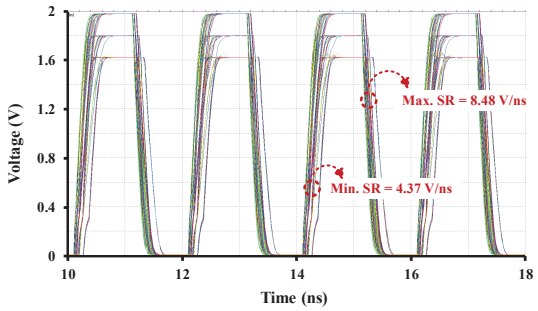

Fig. 8. All-PVT-corner simulations given 1.8 V with compensation

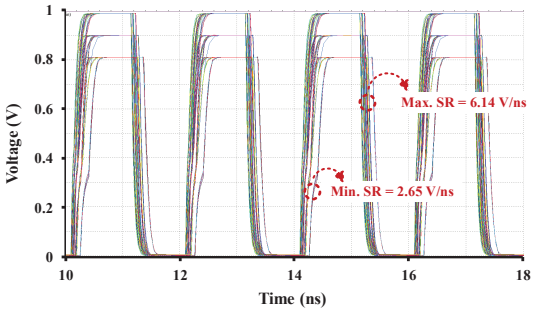

Fig. 10. All-PVT-corner simulations given 0.9 V with compensation

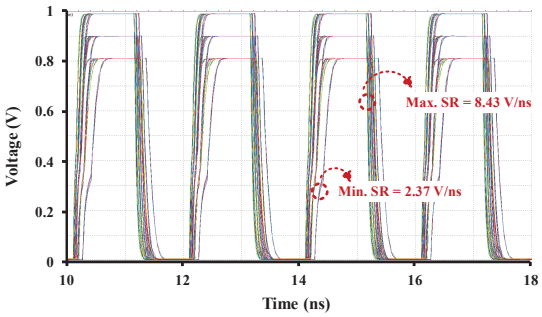

Fig. 9. All-PVT-corner simulations given 0.9 V without compensation

E-110-004- and MOST 107-2218-E-110-016-. The authors would like to express our deepest appreciation to CIC (Chip Implementation Center) in NARL (Nation Applied Research Laboratories), Taiwan, for the assistance of thoughtful chip fabrication.

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