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An On-Chip PWM-Based DC-DC Buck Converter Design with High-Efficiency Light Load Mode Operation

Chua-Chin Wang [+], and Chung-Jye Hsu

Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan 8042

Abstract. This paper demonstrates a DC-DC buck converter with a PWM (pulse width modulation) feedback control loop, which can accommodate the range of power supply voltage from VDD to 2.5xVDD. By utilizing HV (high voltage) MOSFETs provided by HV CMOS technologies, a PWM feedback loop, a Dead-time detector, HV driving transistors and a control circuit are all realized on a single chip. The chip area of the proposed design is less than 1.379x0.813 mm^2, while the power supply range is as wide as 5-14 V. The proposed design is featured with very high conversion efficiency by shutting off an optimal number of power MOSFETs when detecting the light load to prolong the life time of battery-powered devices. Therefore, it can be integrated in a SOC (system-on-chip) to provide multiple supply voltage sources.

Keywords: buck converter, switch numbers, PWM, light load.

1. Introduction

Thanks to the fast evolution of semiconductor technologies, transistors as well as devices are downsized constantly and rapidly. The operation voltage of transistors is also dropped from 5 V to 3.3, 1.8 V, or even lower. Nevertheless, the operation voltage of prior or existing systems might be still 5 V, 12 V or even higher, particularly those in car electronics. Therefore, DC-DC voltage converters are often required in many systems and applications to supply and support lower operation voltage for devices fabricated by advanced processes. The function of DC-DC converter is to convert an input voltage into an adaptive output voltage regardless heavy load or light load. That is, the output voltage of the converter should be independent with the variation of input voltage and output load. Nowadays, there are two popular types of voltage converters, the "Low Drop-Out Linear Regulator (LDO)" type [1] and the "Switching Mode Power Supply (SMPS)" type [2]. Traditionally, two SMPS methods have been reported to implement the controller mechanism, i.e., ``Pulse-Width Modulator (PWM)" and ``Pulse-Frequency Modulator (PFM)". Each has its own features and problems [3].

A long well-known problem is that the on-chip PWM-based SMPS DC-DC converter has poor efficiency when the load is light [4]. Although PFM-based DC-DC converter is proved to have a better efficiency in the same scenario, it results in serious high ripple at the output voltage, which is unacceptable in many sophisticated applications, such as CPU/GPU control. In this investigation, we propose a simple but effective approach to resolve the poor efficiency problem of PWM-based DC-DC converter given the light load. The optimal division method of power MMOSFETs is theoretically analyzed and proved. Meanwhile, the loss in the scenario of heavy load is not affected.

2. PWM-Based DC-DC Converter with High-Efficiency Light Load Mode

2.1. Definition and analysis of efficiency

[+] Corresponding author. Tel.: +886-7-5252000 ext. 4144; fax: +886-7-5254199.
E-mail address: ccwang@ee.nsysu.edu.tw.

Assume the power loss of those discrete components besides transistors is negligible. With the same output current, when the resistance is equal to the load resistance, the efficiency is close to 50%. If the efficiency is expected to be greater than 90%, the turn-on resistance R_{on} must be at least one-tenth of the load resistance R_{load} [4]. Thus, to get a better efficiency, the first thing to carry out is to reduce the turn-on resistance of the power MOSFETs. In the light load scenario, we need to particularly consider the power consumption caused by dynamic switching and the static current. The dynamic power consumption is proportional to the number of transitions, which means the switching frequency. Therefore, reducing operation frequency by the control circuit will provide a better efficiency in the light load scenario.

$$\text{Efficiency} = \eta = \frac{R_{load}}{R_{load}+R_{on}} = \frac{1}{1+R_{on}/R_{load}} \tag{1}$$

Prior methods for such a design purpose include the PFM control circuit, Pulse Skip, and Burst Mode. However, all the prior methods were proved to reduce the frequency of switching and the static current at the expense of large ripples generated on the output voltage.

2.2. Proposed DC-DC converter

Referring to Fig. 1, the proposed PWM-based DC-DC converter is disclosed, consisting of 5 blocks, i.e., buck converter core, error amplifier (EA), PWM, Dead-time circuit, and light load control circuit. Notably, power MOSFET groups, including PMOS1(HVP1), PMOS2(HVP2), NMOS1(HVN1), and NMOS2(HVN2), are all HV devices provided by the foundry process, which can be integrated on silicon with other circuits.

The buck converter part of Fig. 1 is composed of many power MOSFETs and those off-chip discretes, including L_{big} and C_{big}. When Vc_p and Vc_n are both low to turn on PMOS and shut off NMOS, MOS_out equals to Vin to charge the off-chip inductor, L_{big}. As soon as those two control signals flip the state of PMOS and NMOS, inductor L_{big} starts discharging to pull down MOS_out to ground. Therefore, by modulating the turn-on time of these power MOSFETs, namely duty cycle D, the output voltage is predictable as follows.

$$V_{out} = V_{in} \times \frac{D}{1-D} \tag{2}$$

Besides, EA (Error amplifier) is used to keep tracking the output voltage. As a consequence, PWM [5] block plays the role of negative feedback control to stabilize the output voltage and even reduce the ripple thereof. The Dead-time circuit ensures that power PMOS and power NMOS won't be turned on at the same time such that the unwanted DC power dissipation is reduced and the over efficiency is boosted, since the timing control of the power MOSFET gate drives is critical.

2.3. Light load control circuit

This block is the feature of the proposed converter design. Before going to the details of the circuit design, we need to address why the conventional PWM approach has a poor efficiency when the load is light. The energy losses are formulated as follows [6].

$$\textbf{Conduction Loss} = [I_o{}^2 + \frac{[d_{mp}(1-d_{mp})V_{in}]^2}{12L^2F_{sw}{}^2}]R_{on} \tag{3}$$

$$\textbf{Switch Loss} = (C_{g,eq}V_{in}{}^2F_{sw}) + I_oF_{sw}[(V_{in} + 2V_{DN})t_{over} + 2V_{DN}t_{DT}] \tag{4}$$

$$\textbf{R}_{on} = \frac{L}{u_pC_{ox}WV_{od}}, \ \textbf{C}_{g,eq} = WLC_g \tag{5}$$

where W and L are the width and length of the MOSFETs, respectively, C_{ox} is the gate oxide capacitance, Fsw is the switching frequency, d_{mp} is the duty cycle of PMOS, V_{DN} is the diode voltage, t_{over} is the overlap time, t_{DT} is the dead time, and V_{od} is the overdrive voltage. Apparently, the loss of the DC-DC buck converter given light load is dominated by Switch Loss. Therefore, one strategy is to reduce the frequency in such a scenario to cut the loss, which is known as PFM .

Another approach is to reduce $C_{g,eq}$. Our design adopts the latter one. That is, when the converter detects the light load operation mode, certain power MOSFETs are shut off to decrease $C_{g,eq}$ and consequently reduce the switching loss.

$$\because t_{over}, t_{DT}, V_{DN} \text{ are small, Switch Loss} \cong C_{g,eq}V_{in}{}^2F_{sw}$$

$$\therefore \text{ Power Loss = Conduction Loss (in Eqn.(4)) + Switch Loss (in Eqn.(5))}$$

$$= [I_o{}^2 + \frac{[d_{mp}(1-d_{mp})V_{in}]^2}{12L^2F_{sw}{}^2}]R_{on} + C_{g,eq}V_{in}{}^2F_{sw}$$

$$\Rightarrow \text{Power Loss} = P_{Loss,tot} = [I_o{}^2 + \frac{[d_{mp}(1-d_{mp})V_{in}]^2}{12L^2F_{sw}{}^2}]\frac{L}{\mu_p C_{ox} W V_{od}} + WLC_gV_{in}{}^2F_{sw}$$

Simplification $\Rightarrow$

$$P_{Loss,tot} = \alpha\frac{1}{W} + \beta W$$

where

$$\alpha = I_o{}^2 + \frac{[d_{mp}(1-d_{mp})V_{in}]^2 L}{12L^2F_{sw}{}^2\mu_p C_{ox}V_{od}} \quad , \quad \beta = LC_gV_{in}{}^2F_{sw} \tag{6}$$

$\because$ The power loss will be the minimum where the slope of $P_{Loss,tot}$ equals to zero.

$$\therefore \frac{d}{dW}P_{Loss,tot} = 0, \Rightarrow \alpha\frac{-1}{W^2} + \beta = 0, \quad \mathbf{W} = \sqrt{\frac{\alpha}{\beta}} \tag{7}$$

This W is where the minimum power loss is. Based on this thought, the Light Load Control Circuit of the proposed converter is revealed in Fig. 2, where Vll (voltage of light load) is the light load threshold voltage determined by thorough simulations.

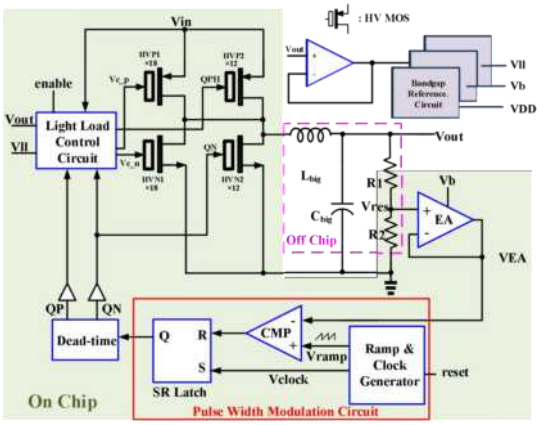

Fig. 1: Proposed PWM-based DC-DC converter.

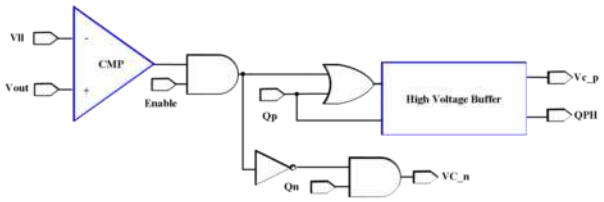

Fig. 2: Light Load Control Circuit.

3. Implementation and Simulation

3.1. Implementation

The proposed PWM-based DC-DC converter is realized on silicon using TSMC UVH 0.5 um CMOS process, as shown in Fig. 3. The chip size is 2873.075x2852.497 um^2.

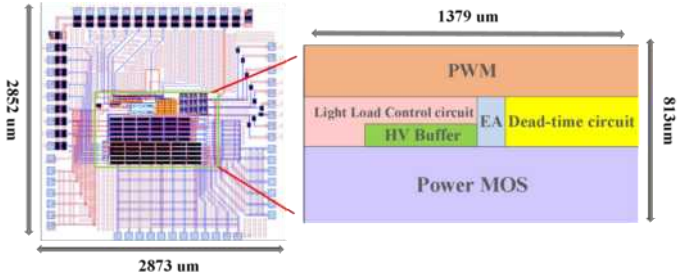

Fig. 3: Layout of the proposed converter.

3.2. Simulation and analysis

Referring to Fig. 4, both pre-layout and post-layout simulations are demonstrated. Vout is stabilized after 1 ms at 5.0 V given Vin = 13 V.

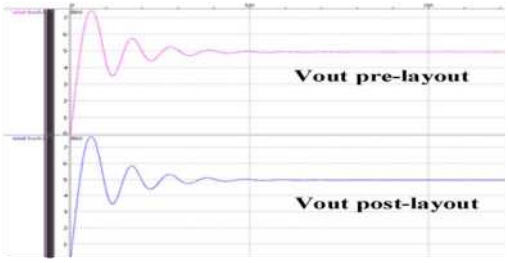

Fig. 4: Simulation results of Vout.

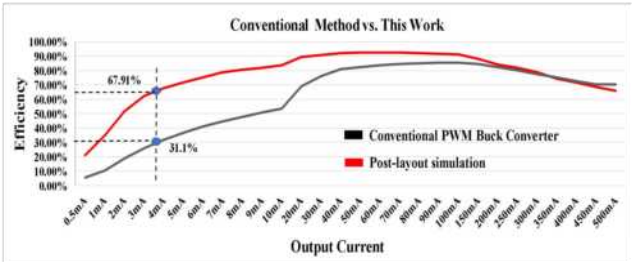

Fig. 5: Efficiency comparison.

As we addressed at the very beginning, the efficiency is the most important performance index to be enhanced. Fig. 5 shows the efficiency comparison of the proposed design vs. traditional DC-DC converters. When the load becomes 4 mA, our design still maintains 67.9% efficiency, while the conventional counterpart drops to 31.1%. The power dissipation is 110 mW at 60 KHz clock rate.

Referring to Fig. 6, the number of turn-on MOSFETs is found to affect the efficiency significantly. Apparently, an optimal number of 11 will give the highest efficiency. By the derivation of Eqn. (3) ~ (7), the optimal number for different output currents can be found. For instance, given the number of 30 power MOSFETs with the same size, the optimal low loss will occur at 12. Based on the derivation and Fig. 6, the total 30 power MOSFETs are divided into 2 groups, where 18 MOSTFETs are driven by the output of Light Load Control Circuit. They will be shut off if the light load is detected. The other 12 MOSFETs are directly driven by the outputs of Dead-time circuit, which means they will be on regardless the load situation. Fig. 6 confirms that the analytic solution matches the prediction by simulations.

Fig. 6: Efficiency & Power loss vs. total number of power MOSFETs.

3.3. Performance comparison

Table 1 tabulates the overall performance comparison with several recent DC-DC converters. Our design has the edge of the largest input high voltage range and the best efficiency.

TABLE I: COMPARISON WITH PRIOR DC-DC CONVERTERS

	This work	VLSI'15 [7]	CICC'17 [8]	PEDES'12 [9]
Year	2017	2015	2017	2012
Process	0.5 um CMOS	0.18um CMOS	0.18 um CMOS	PCB
Input Voltage	10 ~14 V	3 V	2.4 ~ 3.3 V	15 V
Output Voltage	5 V	1 V	1.5 ~ 1.6 V	5 V
Max. Output Current	0.5A	1uA	10mA	1.4A
Settling time	<500us	N/A	N/A	<250us
Efficiency	91.58%	87%	90.4%	80%
Core area	1.287mm^2	2.42mm^2	0.71mm^2	N/A

4. Conclusion

This investigation presents a novel DC-DC buck converter design featured with the shutdown of optimal number of power MOSFETs when the light load operation is detected. Thanks to the reduction of the gate capacitance, the switching loss is reduced such that the efficiency is enhanced. Most importantly, the optimal light load efficiency is found by the derivation of analytic equations, and then justifies by post-layout simulations to achieve the best efficiency in the given wide input voltage range.

5. Acknowledgments

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