A Frequency-shift Readout System with Offset Cancellation OPA for Portable Devices of Marijuana Detection

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***Abstract*—This paper presents a novel frequency-shift readout system with offset cancellation OPA (operational amplifier) for biosensing applications. The chopper technique is used to up-modulate the offset voltage to a higher frequency for noise shaping. A low pass filter is then utilized to filter out the noise caused by offset. A FPW (flexural plate wave) biosensor to sense the THC (Tetrahydrocannabinol), the signature ingredient of marijuana, concentration in urine. The linearity of the proposed system is proved to be 0.959 based on physical experiments where the THC concentration is 0 $\sim$ 160 ng/mL.**

***Index Terms*—resonant frequency, power detector, peak detector, frequency-shift readout circuit**

I. Introduction

Pathogen detection is an important technology for many applications. Three most popular methods of pathogen detection are PCR (polymerase chain reaction), colony count, and ELISA (enzyme-linked immunosorbent assay) [1]. However, these methods are not really suitable for emerging point-of-care demand due to high equipment cost and long operating time. Therefore, biosensors have attracted lots of attention because of better mobility recently, e.g., the portable urine meter of TANITA Corporation produced in Fig. 1 [2]. By the same thought of portable detection devices, a novel readout system for THC (the signature ingredient of marijuana) detection is disclosed in this work.

To detect the resonant frequency shift of the biosensors like FPW and FBAR (film bulk acoustic resonator) whose frequency response acts as a band-pass filter, we have demonstrated a frequency-shift readout system correspondingly [3]. However, the problem of prior readout systems is the limited bandwidth of the first stage of the peak detector, namely OPA, which might not be able to meet the operating frequency of the biosensor, e.g., FPW is around 2 $\sim$ 10 MHz and FBAR is around 2.19 GHz [4] - [5]. To resolve this problem, we present a novel frequency-shift readout system in Fig. 2. The operation procedure is outlined as follows.

- step 1 : After reset the system, the control circuit triggers the scanning-signal generator to generate a scanning-signal of which frequency increases with time until the cycle is over.
- step 2 : When the frequency of the scanning-signal equals to the sensor's resonant frequency, the sensor will deliver the maximum power.
- step 3 : The power detector sends a flag signal to the control circuit when it detects the maximum power.
- step 4 : The control circuit calculates the resonant frequency shift amount of the sensor and displays the result.

In this paper, we present a power detector which includes a wide input range AVC and an offset cancellation OPA.

Fig. 1. The photo of a portable urine meter [2].

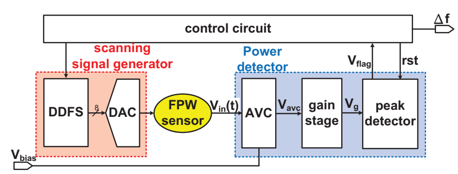

Fig. 2. The proposed frequency-shift readout system.

II. Circuit Design and System Analysis

Referencing to Fig. 2, the proposed power detector is composed of three stages: AVC, gain stage, and peak detector. AVC, shown as Fig. 3 (a), is used to convert the input signal into a DC voltage proportional to the input amplitude. The gain stage amplifies the AVC's output to increase the sensitivity of the readout system. Finally, the peak detector, shown as Fig. 3 (b), will deliver a flag signal when it detects the maximum voltage.

A. AVC

Referring to Fig. 3 (a), the input signal of AVC is isolated from the DC input voltage, V_{bais}, by a capacitor and an inductance. The DC voltage, V_{bais}, drives the M_{201} into the saturation region. The output capacitor is used to filter out the

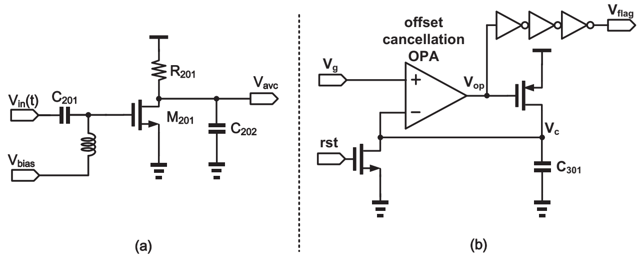

Fig. 3. The schematic of the proposed (a) AVC and (b) peak detecotr.

high frequency components coupled in V_{avc}. Therefore, the output voltage of the AVC is derived as follows.

$$V_{avc} = VDD - \frac{\beta_n}{2} \cdot R_{201} \cdot \left[V_a + \left(V_{bais} - V_{Tn} \right)^2 \right] \quad (1)$$

where VDD is the system voltage, $\beta_n = \mu_n C_{ox} \left(W_{201}/L_{201} \right)$ is the MOSFET transconductance parameter, V_a is the amplitude of the $V_{in}(t)$, and V_{Tn} is the NMOS threshold voltage.

B. Peak detector

Referring to Fig. 3 (b), the peak detector is expected to generate a flag signal when it detects the maximum input voltage. However, the input offset voltage of the OPA is a serious problem thereof. The input offset is mainly caused by the mismatch of the differential amplifier, including the different input and bias voltages. The peak detector needs to trace the output voltage of the gain stage such that the offset problem always exists when the peak detector is working. The offset cancellation OPA shown in Fig. 4 consists of two choppers. The first chopper, ch1, is used to up-modulate the input signal to a higher chopper frequency. The second chopper is used to up-modulate the offset of the gm1 to another chopper frequency and down-modulate the input signal to the original frequency. Finally, the following low pass filter rejects the components whose frequency equal to or higher than the chopper frequency. According to the simulation results, the offset voltage is reduced to 50 μV to increase the sensitivity of the entire system over 10% at the expense of only 7% power consumption increase.

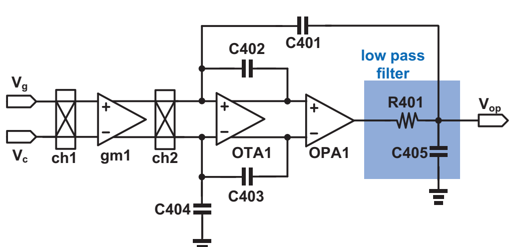

Fig. 4. The schematic of the proposed offset cancellation OPA.

III. Implementation and Measurement

Fig. 5 (a) shows the photo of the proposed readout system composed of three levels. The bottom level of the proposed system is a PCB board integrating the proposed power detector and the DAC. The middle level is an FPGA mini board to carry out the programmable DDFS and the control circuit. Finally, an ARM board, LPC1114, displays the detection result on the top level. The volume of the proposed readout system is about $10 \times 9 \times 5.5$ cm^3.

Fig. 5 (b) shows the measurement results, where the linearity is $\mathrm{R}^2 = 0.9592$. Table I tabulates the comparison with previous works. The proposed frequency-shift readout system only needs two OPAs (one in gain stage, another in the proposed peak detector). More importantly, since the AVC converts the sensor's output into a DC voltage, there is no need of any high-bandwidth OPAs.

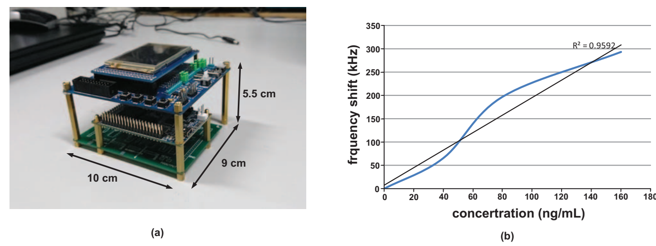

Fig. 5. (a) Photo of the proposed system and (b) measurement results

TABLE I
Comparison with Prior Works

	[6]	[3]	this work
year	2013	2014	2016
technology	FPGA & chip	FPGA & chip	FPGA & discretes
linearity	None	0.9772	0.9592
number of OPA	4 (at least)	4 (at least)	2

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