Dynamic Power Estimation for ROM-less DDFS Designs Using Switching Activity Analysis

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***Abstract*— A pre-realization dynamic power estimation approach for ROM-less direct digital frequency synthesizer (DDFS) designs is proposed, which carries out the analysis of switching activity of all the major logic blocks utilized in the synthesis of ROM-less DDFS. As soon as the partitions of the $\frac{\pi}{2}$ and the characteristic equations for polynomial interpolation are given, the proposed approach is able to assess the overall switching activities such that the power profile of different combination of partitions and equations can be derived before any physical implementation.**

***Keywords*—ROM-less DDFS, polynomial interpolation, power estimation, switching activity, spurious free dynamic range (SFDR)**

I. Introduction

Frequency synthesizer is a well-known sub-system block to generate signals with a selective frequency in a variety of applications, e.g., digital radios, mobile telephones, GPSs (Global Positioning Systems), etc. Fig. 1 shows the conventional ROM-based DDFS, where the phase accumulator is used to generate the digital phase as well as the frequency. Apparently, this kind of DDFS is suffered from all the problems with ROM, e.g., large chip area, long access time, and huge power dissipation.

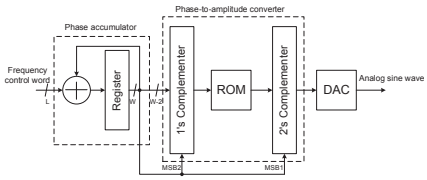

Fig. 1. Conventional DDFS structure

By contrast, the ROM-less DDFS demonstrates many advantages, including high spurious free dynamic range (SFDR) and low area cost [1]- [2]. This kind of DDFS designs utilizes high-order polynomial algorithms instead of the ROM-based look-up tables to realize the phase-to-amplitude converters (PAC). However, according to the prior works [3], any polynomial with order larger than 3 may be inefficient to improve SFDR. Besides SFDR, power consumption has become the major concern for many portable applications. Therefore, we tend to evaluate the power consumption profile before any ROM-less DDFS is realized, as long as the polynomials and the partitions of the phase range are given.

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II. Dynamic Power Prediction of ROM-less DDFS

A. Switching activity assumption

Referring to Fig. 2, ROM-less DDFS is usually realized with 1st order polynomials, namely linear equation, close to phase 0, and 2nd order polynomials close to $\frac{\pi}{2}$ due to the curvature. To attain high SFDR, M_1 segments are used in the near-linear range, while M_2 segments are employed in the high-curvature range. Not only the selection of M_1 and M_2 determines the SFDR, it also posts impact on power consumption. Moreover, the overall hardware (logic circuitry) cost to carry out 1st and 2nd order polynomials will also be determined by the selection of M_1 and M_2.

The major power consumption of the logic circuitry is dominated by dynamic power, which is governed by $P_{dyn} = \alpha \cdot f \cdot C \cdot V^2$, where f is the system clock, C is the area or capacitance, V is the system supply voltage, and α denotes the switching activity of $0 \rightarrow 1$. Since the system clock and supply voltage can be assumed the same for any DDFS implementation and C is basically a random variable hard to be formulated, α becomes the only factor for dynmaic power estimation. Therefore, we propose to assess the power consumption by calculating the number of bit switching, i.e., (bit length) $\times$ (probability of $0 \rightarrow 1$). All of the major logic circuits for DDFS realization are derived as follows provided that the DDFS word length is n.

B. Switching analysis of polynomials

All of the DDFS designs need a counter for frequency control word (FCW), an adder, a register, 1's complementer and 2's complementer in the entire architecture such that a full sinusoidal cycle, $\{0,\ 2\pi\}$, can be implemented by the conversion of $\{0,\ \frac{\pi}{2}\}$ thanks to the symmetry. Assume the bit length of FCW is 32. The overall bit switching of this part is derived as follows.

$$s_0 = 8 + 32 + 8 + \frac{n}{4} + \frac{n}{2} = 48 + \frac{3n}{4} \qquad (1)$$

TABLE I

BIT SWITCH OF LOGIC CIRCUITS

	# bit switch
counter	$1 - \frac{1}{2^n}$
adder	n
multiplier	$n + \frac{3n^2}{16} + \frac{5}{16} + \frac{2^n-(n+1)}{2^{n+1}} + 2\sum_{i=3}^{n-1} \frac{2^i-(i+1)}{2^{i+1}}$
shifter	$\frac{n-1}{4}$
1's complementer	$\frac{n}{4}$
2's complementer	$\frac{n}{2}$
k-to-1 MUX loading q bits	$\frac{(k+1)\cdot n+q}{4}$

As mentioned earlier, high-order polynomials (> 3) are hard to attain high speed and good SFDR. Thus, most of phase-to-amplitude converter (PAC) in the ROM-less DDFS are realized by the following polynomials.

$$f_1 \quad : \quad y_i = a_i \cdot x + c_i \tag{2}$$

$$f_2 \quad : \quad y_j = a_j(x + b_j)^2 + c_j \tag{3}$$

where x is the phase, y_i, y_j is the mapping output, a_i, c_i, a_j, b_j, c_j are constants, and i, j are the index of the polynomials, $0 \leq i \leq M_1$, $0 \leq j \leq M_2$. Notably, M_1 is the number of partitions in the left-hand side of $\{0, \frac{\pi}{2}\}$, while M_2 is that of the right-hand side, as shown in Fig. 2. According to Table I, the bit switching of $x + b_j$ is $n + \frac{n(M_1+M_2+1)+\log_2(M_1+M_2)}{4}$. Then, the total of bit switching is expressed as follows.

$$\begin{aligned} s_{PAC} \quad = \quad & (M_1 + M_2 + 2)\frac{n(M_1 + M_2 + 1) + \log_2(M_1 + M_2)}{4} \\ & + n(M_1 + M_2 + 1) + \frac{n-1}{4}(M_1 + M_2)^2 \\ & + \frac{n(M_1 + M_2)}{4} + s_{multiplier} \end{aligned} \tag{4}$$

where $s_{multiplier}$ is the bit switching of the multiplier in Table I. Finally, the overall bit switching of the ROM-less DDFS becomes $s_{DDFS} = s_{PAC} + s_0$.

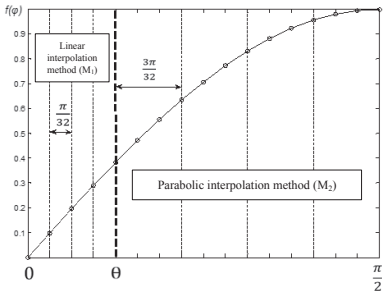

Fig. 2. Approximation of $\frac{1}{4}$ sine wave

III. Experiment and Analysis

To verify the performance of the proposed approach, a ROM-less DDFS with FCW = 32 bits is carried out, as the phase-to-amplitude converter (PAC) part shown in Fig. 3. The power performace compared with the prior work [4] is tabulated in Table II. Notably, all of the DDFS designs are download onto Altera FPGA Cyclone EP 2C35F672C6 platform and tested with identical system clock and benchmark test patterns. The reduction ratio predicted by the proposed approach is 34.2%, which is lower than the average of reduction ratio of 63.29% given by the FPGA reprots. However, as highlight by [5], dynamic power occupies around 70-80% of the total power for 0.35 μm CMOS process. If this factor is taken into consideration, the reduction of dynamic power on FPGA board will become around 44%, which is close to what we have predicted. This fact justifies the validity of our approach.

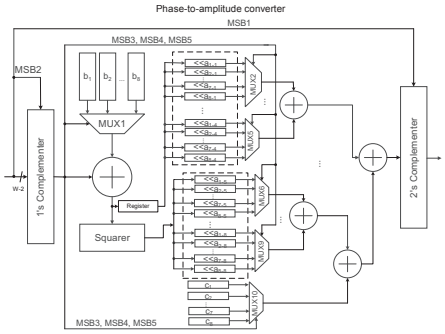

Fig. 3. PAC in the proposed DDFS with FCW = 32 bits

TABLE II

POWER ESTIMATION OF ROM-LESS DDFS

	[4]	this work	reduction
bit switching	3008	1030	34.20%
FPGA (50 MHz)	35.92 mW	24.39 mW	67.90%
FPGA (100 MHz)	70.66 mW	45.31 mW	64.12%
FPGA (150 MHz)	105.91 mW	64.64 mW	61.03%
FPGA (200 MHz)	147.13 mW	88.46 mW	60.12%

IV. Conclusion

A simple approach to analyze the dynmaic power dissipation before the ROM-less DDFS realized on silicon is proposed in this investigation. The proposed approach will facilitate the low-power DDFS design as soon as the partitions and the polynomia equations are given.

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