A Pipeline ROM-less DDFS Using Equal-Division Interpolation

Tsung-Yi Tsai, Hsiang-Yu Shih, and Chua-Chin Wang†, *Senior Member, IEEE*

Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

***Abstract*—A pipeline ROM-less direct digital frequency synthesizer (DDFS) with equal division interpolation is proposed in this investigation. In order to get higher SFDR and faster clock rate, different segments with various interpolation equations are analyzed. 2nd-order parabolic equations with proper selection of coefficients based on hardware cost is utilized to transcend the limitation of SFDR. Thus, a 4-stage pipeline architecture is realized to achieve better clock speed. This work demonstrates the maximum SFDR for 102 dBc and the output frequency for 50 MHz using TSMC 0.18μm CMOS technology cell library.**

***Index Terms*—frequency synthesizer, DDFS, parabolic polynomial interpolation, SFDR, FCW**

I. Introduction

Frequency synthesizers play an important role in many communication systems, e.g., wireless communications, mobile phones, or global positioning system (GPS). It can be used to generate signals with various frequencies. Conventionally, phase-locked loop (PLL) [1] is widely used to generate a signal with a selected frequency, where disadvantages, such as poor phase noise performance, high power consumption per frequency, slow switching speed, etc., have been found. To transcend the limitation of PLL, the first direct digital frequency synthesizer (DDFS) was proposed in 1971's [2]. The amplitude data is stored in ROM-based look-up table, which later becomes the major drawback of this architecture.

Recently, ROM-less DDFS [3] - [5] has been developed to avoid power, area, and speed problems caused by the large ROM table. High-order (more than three) polynomials are utilized to replace the large ROM table and realize the phase-to-sin mapper. However, according to the prior work [6], the order of the polynomial can't larger than three. Otherwise, the spurious free dynamic range (SFDR) of sine wave will be limited. In order to increase SFDR and maximum output frequency than the prior works, e.g., [7], 2nd order polynomial with equal division in a pipeline architecture is proposed in this design.

†: Prof. C.-C. Wang is the contact author.

Acknowledgement: This proposed design was partially supported by National Science Council, Taiwan, under grant MOST 104-2622-E-006-040-CC2, MOST 105-2218-E-110-006-, MOST 105-2221-E-110-058-, and the authors would like to express our deepest appreciation to CIC (Chip Implementation Center) in NARL (Nation Applied Research Laboratories), Taiwan, for the assistance of thoughtful chip fabrication.

II. Pipeline DDFS Design With Equal-Division Interpolation

A. Interpolation scheme selection

Usually, a quarter of the full sine wave is equally divided into several parts, where each part is approximated by equations. Then, by taking advantage of the symmetry of the sine wave, the other three quarters can be synthesized into a complete full cycle waveform. Therefore, the selectivity of interpolation scheme will directly affect the maximum error and SFDR. Three common interpolation methods, e.g., linear interpolation, quasi-linear interpolation, and parabolic interpolation, with different segmentation scenarios is compared by MATLAB simulation and summarized in Table I. The SFDR and maximum error results of parabolic interpolation with 8 segments is better than that of quasi-linear interpolation with 32 segments. Besides, if the design complexity, area overhead, and switching speed are taken into consideration, the parabolic interpolation with 8 segments is a better option.

TABLE I
Performance with different segment and interpolation

	Parabolic interpolation		Quasi-linear interpolation		Linear interpolation	
Segment	Max. Error	SFDR	Max. Error	SFDR	Max. Error	SFDR
4	4.97×10^{-4}	86	3.00×10^{-3}	71	6.29×10^{-3}	53
8	$\mathbf{6.30 \times 10^{-5}}$	**106**	9.91×10^{-4}	81	1.59×10^{-3}	65
16	7.92×10^{-6}	123	2.78×10^{-4}	93	4.01×10^{-4}	78
32	9.97×10^{-7}	142	7.31×10^{-5}	105	1.00×10^{-4}	90

B. Characteristic equation and pipeline selection

As mentioned in the previous subsection, the complexity can be reduced by selecting proper 2nd-order characteristic equation even though the parabolic interpolation scheme is used. Table II summarized the result of 4 different 2nd-order parabolic equations by MATLAB simulations. From the viewpoint for SFDR, the missing coefficient "b" in equation #2 makes coefficient "a" hard to fit both curvature and slope at the same time. On the other hand, equation #2 has the least complexity, while equation #1 is the most complicated one because one more multiplexer is needed. Last but not least, according to the specification of 32-bit frequency control word

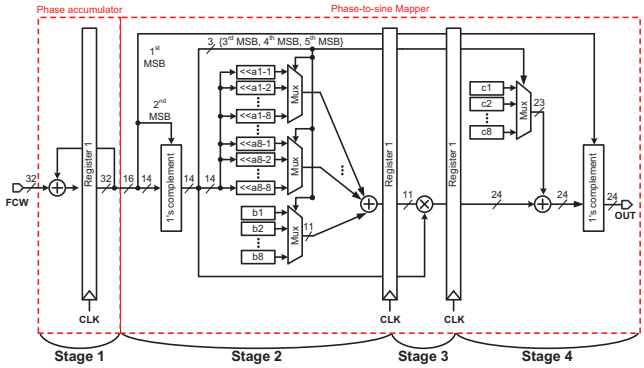

Fig. 1. Schematic of the proposed pipeline DDFS.

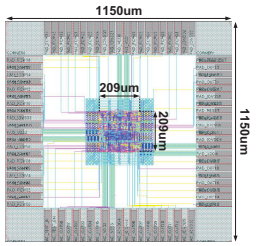

Fig. 2. Layout of the proposed pipeline DDFS.

(FCW) and 24-bit output resolution, we choose equation #4 to realize our design.

According to the previous analysis, the schematic of our 4-stage pipeline DDFS is shown in Fig. 1. If only Register 1 is inserted after the adder, this pipeline 2-stage system achieves only 62 MHz of the maximum clock rate. The reason is that the data processing after Register 1 takes a long time to complete. Besides, the multiplexer is found to be the bottleneck of the speed such that Register 2 and 3 are inserted before and after the multiplexer, respectively, to boost the clock rate up to 100 MHz. The speed has been increased 60% for only 12% area overhead by this design.

III. Simulation Results

This work is realized by TSMC 0.18μm Mixed signal CMOS process. Fig. 2 shows the layout of this work, where the core area is only 0.209×0.209 mm^2, and the overall chip size is 1.15×1.15 mm^2. Table III is the performance comparison with prior ROM-less DDFS designs. Our design attains the highest SFDR. Although the clock rate is limited by output resolution, the FOM justifies that our design is very competitive among all the DDFS circuits to date.

IV. Conclusion

This paper has demonstrated a pipeline ROM-less DDFS with optimally selected segments and 2nd-order parabolic interpolation equations. Given limited specification of FCW (32 bits) and output resolution (24 bits), our work attains the significant SFDR 102 (dBc) and achieve the highest FOM.

TABLE II
Different Parabolic Equation Comparison

	#1	#2	#3	#4
Equation	ax^2+bx+c	ax^2+c	$a(x+b)^2+c$	$(ax+b)x+c$
Hardware cost	24-bit ADD 25-bit ADD 14×14 MUL 11×14 MUL	24-bit ADD 14×14 MUL	21-bit ADD 26-bit ADD 17×17 MUL	11-bit ADD 24-bit ADD 11×14 MUL
Comparison	SFDR	#1 = #3 = #4 > #2		
	Complexity	#1 > #3 > #4 > #2		

*Control factor is 32-bit FCW and 24-bit output resolution
*ADD=adder, MUL=multiplexer

TABLE III
Performance Comparison of DDFS

	[7]	[3]	[4]	[5]	This work
year	*ISIC 2011*	*EMICC 2013*	*ICEE 2014*	*IFCS 2016*	2017
Process (μm)	0.35	0.13	0.35	0.18	0.18
FCW	32 bits	32 bits	9 bits	17 bits	32 bits
Output Resolution	24 bits	12 bits	8 bits	10 bits	24 bits
Power (mW/MHz)	0.31	1.07	0.186	0.027	0.12
Normalized Area ($\times 10^6 mm^2$)	11.85	18.93	1.20	0.52	1.35
SFDR (dBc)	68	60	55	52.47	102
Verification	Sim.	Meas.	Sim.	Meas.	Sim.
Clock (MHz)	50	650	1000	100	100
Max. Output Freq. (MHz)	25	N/A	N/A	N/A	50
FOM	8324	957	3090	15891	1092267

*Sim.=Simulation, Meas.=Measurement
†FOM = $\frac{2^{\frac{\text{SFDR}}{6}}}{\text{Power}}$ [8]

References

[1] Y. Sun, X. Yu, W. Rhee, D. Wang, and Z. Wang, "A fast settling dual-path fractional-N PLL with hybrid-mode dynamic bandwidth control," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 8, pp. 462-464, Aug. 2010.

[2] J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," *IEEE Trans. on Audio and Electroacoustics*, vol. 19, no. 1, pp. 48-57, Mar. 1971.

[3] J. Cali, X. Geng, F. Zhao, M. Pukish, F. Dai, and A. Aklian, "A 650 MHz DDFS for stretch processing radar in 130nm BiCMOS process," in *Proc. European Microwave Integrated Circuit Conference (EMICC)*, pp. 33-36, Oct. 2013.

[4] M. Padash, S. Toofan, and M. Yargholi, "A 9-bit, 1-giga samples per second sine and cosine direct digital frequency synthesizer," in *Proc. Iranian Conf. on Electrical Engineering (ICEE)*, pp. 438-442, May 2014.

[5] P. R. B. de Carvalho, J. A. A. Palacio, and W. Van Noije, "Area optimized CORDIC-based numerically controlled oscillator for electrical bio-impedance spectroscopy," in *Proc. IEEE Int. Freq. Control Symposium (IFCS)*, pp. 1-6, May 2016.

[6] C.-C. Wang, C.-H. Hsu, C.-C. Lee, and J.-M. Huang, "A ROM-less DDFS based on a parabolic polynomial interpolation method with an offset," *Journal of Signal Processing Systems*, vol. 61, pp.1-9, May 2010.

[7] C.-H. Hsu, Y.-C. Chen, and C.-C. Wang, "ROM-less DDFS using non-equal division parabolic polynomial interpolation method," in *Proc. Int. Symp. on Integrated Circuits (ISIC)*, pp. 59-62, Dec. 2011.

[8] X. Geng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "An 11-Bit 8.6 GHz direct digital synthesizer MMIC with 10-Bit segmented sine-weighted DAC," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 45, no. 2, pp. 300-313, Feb. 2010.