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2×VDD 28-nm CMOS Digital Output Buffer Using Low-Vth Transistors for Slew Rate Adjustment

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***Abstract*—A 2×VDD output buffer with process, voltage and leakage compensation technique is proposed to keep slew rate (SR) self-adjusted within predefined ranges regardless PV variations. Low Vth (threshdold voltage) transistors are employed in the stacked driving transistor strings to boost the driving current. On the other hand, a leakage detection loop is added at the gate drives of these low Vth transistors to clamp the leakage when the output stage is not activated such that the power dissipation is reduced. Another feature of the proposed buffer is the gate-oxide leakage is also reduced by lenthening the transistors in the string. The reason of temperature variation is not considered is that it is found to be relatively low correlated to slew rate for 90 nm and better CMOS processes. Besides, all bias voltages in process and voltage variation detectors are generated from bandgap circuits to reduce the variations caused by temperature drifting. The proposed output buffer is carried out using a typical 28-nm CMOS process. The date rate measured on silicon is proved to be 2.0 GHz given 1.05/1.8V supply voltage, namely 1xVDD/2xVDD for 28-nm process, when the proposed compensation design is activated.**

Keywords— output buffer, PV variation, leakage detection, slew rate adjustment, gate-oxide reliability

I. Introduction

CMOS technologies have been developed rapidly with advantages, including low supply voltage, low fabrication cost per area, and low power consumption. However, many recent PCB-based applications still needs chips fabricated by legacy processes to achive certain functions, e.g., drivers. Therefore, when a PCB-based system is equipped with chips fabricated by different generations of CMOS process, which use different digital voltage levels, e.g., 1.8 V vs. 3.3 V, data exchange become an issue, where the slew rate is the major issue for digital transmission. Additional chips were utilized to resolve this problem, e.g., level converters. Extra area and power are demanded if they are physically applied. To reduce the number of level converters as well as the size of PCB, mixed-voltage buffers become required to translate digital signals from different chips with different supply voltages.

Regarding the harsh requirement of I/O interfaces, take the up-to-date DRAM product standard DDR4 (Double Data Rate Fourth Generation) as an example, which arises to satisfy HPC (High Performance Computing system). The minimum SR limitation is 4 V/ns. If the SR is too large, the SSN (simultaneous swicthing noise) will be very serious to jeopardize the signal integrity [9]. By contrasy, if the SR is too small, the time margin will become an issue to lacth digital signals [7]. Many researches in the past few years have been proposed to resolve problems given such a harsh SR condition such as over-stress problems, PVTL variations, which were mainly based on stacked architecture and variation detectors to compensate SR and increase reliability, respectively [1] - [6]. Besides, an improved digital-based process detector was also reported to simplify the detection mechanism and increase the detection speed [7]. Although so many researchers have noticed the demand of mixed-voltage output buffers and proposedvarious solutions to resolve slew rate (SR) deterioration problems caused by PVT variations, it will be the major foe to beat in the deep nano-scale CMOS technology nodes.

However, if the temperature impact on SR variation is compared with those of process and voltage impact, as shown in Table I, the result by a Monte-Carlo simulation (100 times) shows that given 1V, TT, 25°C as a typical circumstance, where each simulation change one variable (P, V, or T) a time to see the difference caused by each variation. When the impact of each variation is assumed as the ratios both at rising and falling edges, the impact of voltage and process variations is 3 times larger than that of the temperature. Therefore, the temperature detection can be ignored from I/O design, if the area cost is one of the major consideration factors.

TABLE I
Comparison of Variation Factors to Slew Rate

VDD (V)	Corners	Temp. (°C)	ΔRise (V/ns)	ΔFall (V/ns)	Correlation Ratio (Rise/Fall)
0.9-1.1×VDD	TT	25	2.08	1.93	4.1/3.64
1×VDD	All	25	1.78	1.74	3.63/3.28
1×VDD	TT	0-100	0.49	0.53	1/1

Based on the above simulation and observation, we propose to mainly focus on elimination approach againt process and voltage variations to compensate the SR. Besides the PVT variation, another serious issue for those I/O buffers using nano-scale CMOS process is the leakage. Not only the leakage causes unwanted power dissipation, it also results in poor slew rate for the buffer to drive large output loads. Therefore, a novel output buffer for nano-scale CMOS processes is proposed in this investigation, where low Vth transistors integrated with leakage detection loop to enhance the driving current and reduce the leakage current simultaneously such that the mentioned

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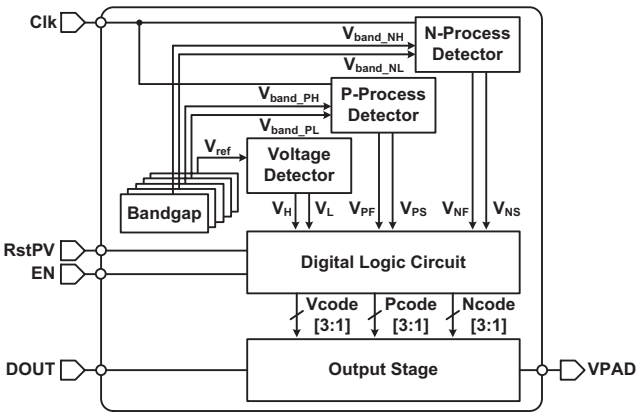

Fig. 1. Block diagram of the proposed 2×VDD digital output buffer.

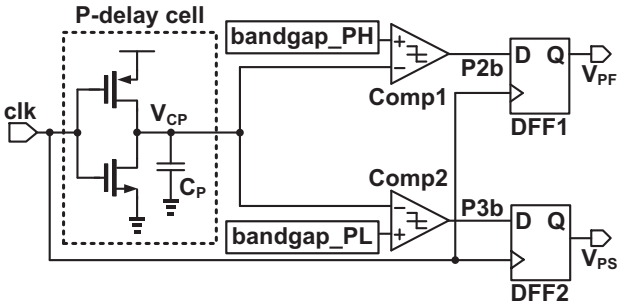

Fig. 2. Schematic of P-Process Detector.

problems exsisting in prior I/O buffer designs are resolved.

II. Nano-scale 2×VDD Output Buffer

Referring to Fig. 1, the proposed output buffer consists of N-Proccess Detector, P-Process Detector, Voltage Detector, Bandgap circuits, Digital Logic Circuit, and an Output Stage. Notably, Clk is the system clock, and DOUT is the digital signal given by the internal digital core to be transmitted outward. RstPV, RstL, and EN are 3 control signals for Digital Logic Circuit. The operation of the proposed design is outlined as follows.

1). Clk drives P-Process Detector and N-Process Detector at the same time. Each detector generates a ramping voltage to be compared with the output voltage of the corresponding bandgap circuit such that the delay of each detector will be measured simultaneously and independtly. V_{PS} and V_{PF} are then generated by the PMOS detection path, while V_{NS} and V_{NF} are generated by the NMOS ounterpart.

2). The voltage detection is carried out by comparing two voltages generated by a PMOS string with a pre-defined voltage generated by another bandgap circuit. V_H and V_L will then be generated and devlievered to the following Digital Logic Circuit.

3). Digital Logic Circuit is basically an encoder to encode the mentioned output signals, namely, V_{PS}, V_{PF}, V_{NS}, V_{NF}, V_H, and V_L into 3 groups of digital signals, Pcode [3:1], Ncode [3:1], and V[3:1] to drive those large transistors correespondingly in the Output Stage.

4). Notably, RstPV and EN are external control signals, which are used to either activate or de-activate the proposed compensation mechanism such that the performance of the proposed design would be correclty analyzed. RstL is another control signal in charge of leakage detection and compensation. If RstL = logic 1, the leakage compensation mechanism is closed.

5). The swing of the digital output is allowed to be 1×VDD or 2×VDD depending on the VDDIO in Output Stage. 6 driving PMOS transistors and 6 driving NMOS transistors are into 2 groups. One group consisits of 3 PMOS and 3 NMOS driving transistors corresponding to the process detection outputs, while the other group containing another 3 PMOS and 3 NMOS driving transistors in response to the voltage variation.

A. Process variation detector

As mentioned earlier, the core of the proposed design is to detect what process corner the die resides such that the compensation of the associated process variation is feasible. Referring to Fig. 2, P-Process Detector comprises a P-delay cell, 2 comparators (namely Comp1 and Comp2), , and 2 DFFs (D flip flop). To maginfy the process variation impact upon the signal timing, the aspect ratio (W/L) of the PMOS in the P-delay cell is relatively smaller than that of a regular inverter, while the aspect ratio of the NMOS therein in relatively large. Therefore, due to the long length of the pull-up and the large width of the pull-down, V_{C_P} at C_P, will turn out to be a slow ramping but fast droping waveform. V_{C_P} is then compared with two pre-defined voltages, namely V_{band_PH} and V_{band_PL}, using Comp1 and Comp2, respetively. Notably, since Clk is an external clock with 50% duty cycle, it will sample the inverted outputs of the 2 comparators (V_{PF} and V_{PS}) and latch them into DFF1 and DFF2, respectively.

If the PMOS resides in the Slow corner, V_{C_P} will be charged slower such that V_{C_P} can not be rasied over V_{band_PH} and V_{band_PL}. Therefore, V_{PF} and V_{PS} will sampled as low at the rising edge of Clk. If the PMOS is in the Typical corner, V_{C_P} will be raised between V_{band_PH} and V_{band_PL} such that the outputs of DFF1 and DFF2, namely, V_{PF} and V_{PS}, are respectively latched with low (GND) and high (VDD). Finally, if the PMOS is "Fast", V_{C_P} will be charged over V_{band_PH} and V_{band_PL} to make V_{PF} and V_{PS} both registered with logic 1. As soon as the above detection is done, which means Clk becomes high, the pull-down NMOS in the P-delay cell will be turned on to ground V_{C_P}. An illustrative timing waveform is demonstrated in Fig. 3 to show how the process corner is detected by the mentioned method.

The counterpart of the P-Process Detector is the N-Process Detector, as shown in Fig. 4, consisting of an N-delay cell, 2 comparators (namely Comp3 and Comp4), 2 inverters, and 2 DFFs. The NMOS Sensor is a high-skew inverter composed of 2 NMOS transistors and a capacitor, C_N. The operation of the N-Process Detector is very similar to that of the P-Process

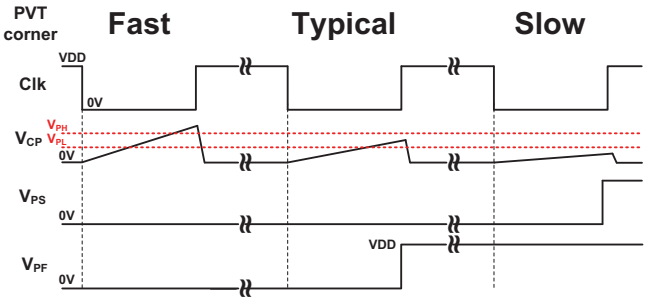

Fig. 3. Illustrative waveform for P-Process Detector operation.

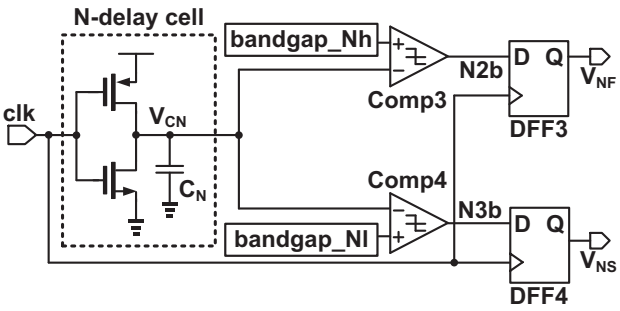

Fig. 4. Schematic of N-Process Detector.

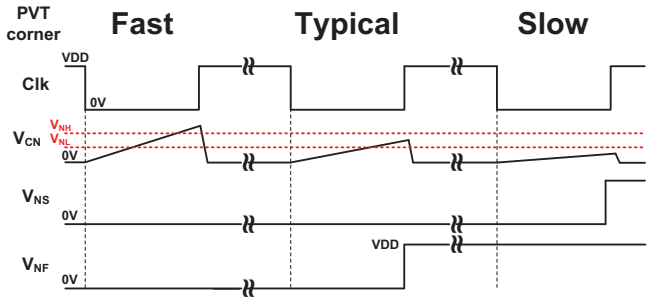

Fig. 5. Illustrative waveform for N-Process Detector operation.

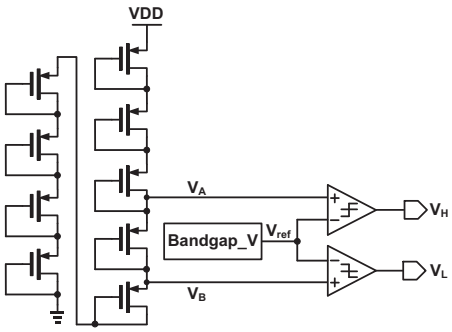

Fig. 6. Schematic of Voltage Detector [8]

Detector. As soon as the falling edge of Clk appears, the pull-up NMOS of the N-delay cell is turned on to charge C_N. That is, V_{C_N} at C_N is charged from GND gradually. If the NMOS resides in the Slow corner, the charging will be slow. When Clk transits from GND to VDD, namely rising edge, DFFs will be triggered to sample V_{NF} and V_{NS}, respectively. Since NMOS is assumed to be Slow, V_{C_N} can not be charged over 2 pre-defined bias voltages, i.e., V_{band_NH} and V_{band_NL} such that V_{NF} and V_{NS} are both 0. If it is in the Typical corner, V_{C_N} will stay between V_{band_NH} and V_{band_NL}such that V_{NF} and V_{NS} become 0 and logic 1, respectively. The last case is that when it is in th Fast corner, both of V_{NF} and V_{NS} are registered with 1. When the detection is done, the pull-down NMOS of the N-delay cell will be asserted to ground V_{C_N} and wait for the next falling edge to start another cylce of detection. The illustrative timing waveform for N-Process Detector is demonstrated in Fig. 5. In short, the above senarios are summarized in the following Table II.

TABLE II
FUNCTION TABLE OF PROCESS DETECTORS

P corner			
	V_{C_P}	V_{PF}	V_{PS}
Fast	$V_{C_P} > V_{band\_PH} > V_{band\_PL}$	Logic 0	Logic 0
Typical	$V_{band\_PH} > V_{C_P} > V_{band\_PL}$	Logic 1	Logic 0
Slow	$V_{band\_PH} > V_{band\_PL} > V_{CP}$	Logic 1	Logic 1
N corner			
	V_{C_N}	V_{NF}	V_{NS}
Fast	$V_{C_N} > V_{band\_NH} > V_{band\_NL}$	Logic 0	Logic 0
Typical	$V_{band\_NH} > V_{C_N} > V_{band\_NL}$	Logic 1	Logic 0
Slow	$V_{band\_NH} > V_{band\_NL} > V_{C_N}$	Logic 1	Logic 1

B. Voltage detector

Referring to Fig. 6, the schematic of Voltage Detector is disclosed. A string of 9 diode-connected PMOS transistors are divided into 3 groups correspding to 3 subranges from VDD to GND : VDD $\sim$ V_H, V_H $\sim$ V_L, V_L $\sim$ GND [8]. It is easy to tell what the voltage variation is by such a configuration, since the variation of VDD between $\pm$10% VDD can be directly sensed. The 9 PMOS transistors have the same size to auto-cancel the effect caused by process and temperature variations. That is, although the resistance of diode-connected MOS under different variations will drift, the voltages, V_H and V_L, are equally drifted as well. Therefore, when it comes to $\pm$10% VDD variations, the output voltage of the bandgap circuit will be fluctuated between +1.49% and -1.26%. Detailed function is summarized in Table III.

TABLE III
FUNCTION TABLE OF VOLTAGE DETECTOR

Voltage Level	V_H	V_L
+10% VDD	Logic 1	Logic 1
VDD	Logic 1	Logic 0
-10% VDD	Logic 0	Logic 0

C. Digital logic

Process Detector and Voltage Detector deliver compensation signals, namely V_{PF}, V_{PS}, V_{NF}, V_{NS}, V_H, and V_L, to Digital Logic Circuit. EN=1 forces Output Buffer to turn on all driving current paths. Notably, the priority of signal EN is higher than

that of RstPV. RstPV = 0 will be in charge of turning on compensation mechanism. Then, Pcode [3:1], Ncode [3:1], and Vcode[3:1] are generated by hard-wired logic circuitry to drive different current paths of Output Buffer. By contrast, when RstPV = 1, Pcode [3:1], Ncode [3:1], and Vcode[3:1] are all set to (0 1 1) regardless whatever the outcome of Process Detector and Voltage Detector is. The truth table of Digital Logic Circuit is tabulated as Table IV.

TABLE IV
FUNCTION TABLE OF DIGITAL LOGIC CIRCUIT

EN	RstPV	V_{PF}	V_{PS}	Pcode[3]	Pcode[2]	Pcode[1]
1	x	x	x	0	0	0
0	1	x	x	0	0	1
0	0	1	1	0	0	0
0	0	1	0	0	0	1
0	0	0	0	0	1	1
EN	RstPV	V_{NF}	V_{NS}	Ncode[3]	Ncode[2]	Ncode[1]
1	x	x	x	1	1	1
0	1	x	x	1	1	0
0	0	1	1	1	1	1
0	0	1	0	1	1	0
0	0	0	0	1	0	0
EN	RstPV	V_H	V_L	Vcode[3]	Vcode[2]	Vcode[1]
1	x	x	x	1	1	1
0	1	x	x	1	1	0
0	0	1	1	1	1	1
0	0	1	0	1	1	0
0	0	0	0	1	0	0

D. Output stage

The schematic of Output Stage is shown in Fig. 7, mainly consisting of Pre-Driver, Vg1 generator, Vg2 genrator, and Driving Transistors. Pre-Driver receives the input signal DOUT, Pcode [3:1], Ncode [3:1], and Vcode[3:1] and utilizes a hard-wired encoder to generate a total of 12 signals, where $V_{pa1}, V_{pb1}, V_{pc1}$ and $V_{pa2}, V_{pb2}, V_{pc2}$ are coupled to Vg1 generator, while $V_{n301a}, V_{n301b}, V_{n301c}$ and $V_{n302a}, V_{n302b}, V_{n302c}$ are directly used as gate drives, respectively, to N301a, N301b, N301c, N302a, N302b, and N302c. Notably, P301a, P301b, P301c and N301a, N301b, N301c are in charge of generating a driving current in response to the process variation. By contrast, P302a, P302b, P302c and N302a, N302b, N302c are used to generating a driving current upon the voltage varation. Table V revealed the internal voltage levels in Output Stage.

TABLE V
VOLTAGE LEVELS OF DRIVING SIGNALS

VDDIO(V)	V_{p301x},V_{p302x}(V)	V_{g2}(V)	V_{n301x},V_{n302x}(V)
1.05	1.05/1.8	1.05	1.05/1.8
1.8	0.0/1.05	0.0	0.0/1.05

1) leakage detection and reduction: A long ignored problem is that if nano-scale CMOS process, e.g., 28-nm process, is used to carry out an output buffer, the basic driving current would be relatively small. The slew rate then becomes very poor. Therefore, low Vth transistors are used to replace those transistors in the basic current paths, which are P301a, P303, N303, N301a, and P302a, P303, N303, N302a, as shown in Fig. 7, since these two paths are always on. The reason is low

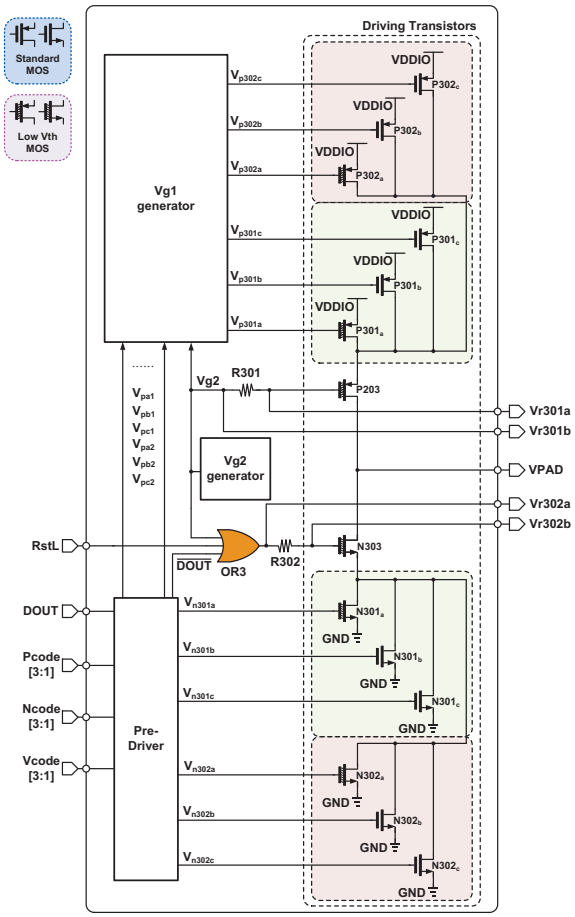

Fig. 7. Schematic of Output Stage in Fig. 1.

Vth transistor is able to supply a higher current given the same aspect ratio.

However, the overhead of using low Vth transistors is the increase of gate oxide leakage, particularly the low Vth NMOS. What even worse is that most of the logic CMOS processes might not have a thick oxide layer to prevent this drawback. As addressed earlier, N303 is an always-on low Vth device such that it causes the largest leakage. Therefore, to alleviate the leakage threat, a 3-input OR gate is added at the gate driving path of N303, which has the largest leakage currennt. The inputs of the OR gate are V_{g2} from Vg2 generator, RstL, and $\overline{\text{DOUT}}$. When the external RstL = 1, the leakage compensation is off. If RstL = 0 and the output of Vg2 generator is also low indicating that VDDIO is $1\times$ VDD by the function of Vg2 generator, V302a will attain the same logic valur with DOUT. Thus, if DOUT is low, N303 is off to cut off the leakage path. By this extra leakage detection and control design, the leakage power will be reduced at least $\frac{1}{4}$ statistically. Meanwhile, to justify the leakage compensation performance externally, R301 and R302, respectively, are added at the gates of P303 and N303. These 2 resistors are small enough not to cause any voltage drop at the gate drives, but large enough to generate measurable voltage drops over (VR301a, VR301b) and (VR302a, VR302b).

2) Vg1 generator: Vg1 generator is basically a voltage level shifter in this design, which is an enhanced version of that in [4], as shown in Fig. 6. A total of 6 identical voltage level shifters consist of Vg1 generator to generate $V_{p301a}, V_{p301b}, V_{p301c}$ and $V_{p302a}, V_{p302b}, V_{p302c}$. When the output of Vg2 generator, e.g. V_{g2}, is high, all of the 6 generated output are boosted to [1.05V, 1.8V] from [0V, 1.05V], (namely $V_{pa1}, V_{pb1}, V_{pc1}$ and $V_{pa2}, V_{pb2}, V_{pc2}$). Otherwise, the voltagelevel remains the same.

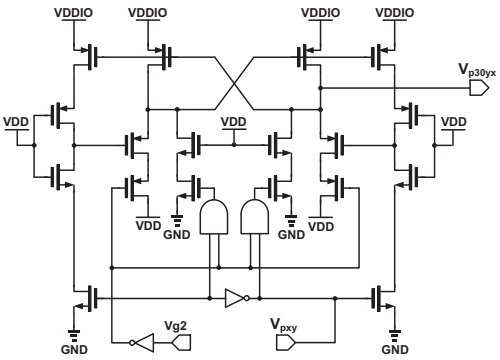

Fig. 8. Vg1 generator

3) Vg2 generator: Referring to Fig. 9, Vg2 generator is in charge of 2 functions, i.e., VDDIO detection and V_{g2} generation. The details are as follows.

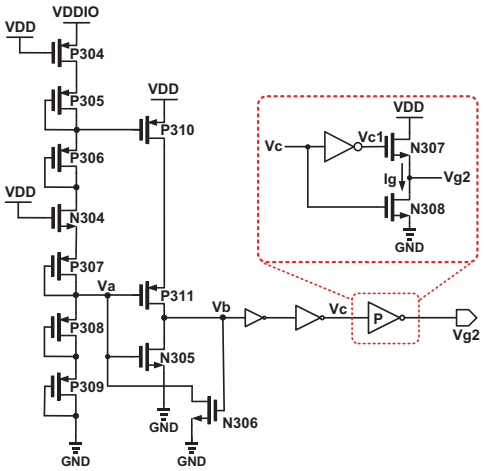

Fig. 9. Vg2 generator

• VDDIO detection : the transistor string at the lefthand side is a voltage divider to generate the gate drives of P310 and P311. Note that P304 and N304 are not G-D-shorted devices. On the way around, they are driven by VDD directly as active current sources. If VDDIO is high enough to turn on P310 and P311, Vb will be pulled high to turn on N306 such that Va is grounded to shut off N305 and latch on P311 for good. Meanwhile, Vb is reshaped as Vc by 2 tappered inverters.

• V_{g2} generation : When it comes to buffer designs using nanoscale CMOS processes, one of the biggest challenges is the poor driving current. Since V_{g2} is used as an improtant bias in the entire circuit, the output stage can not be a simple inverter which usually delivers a small driving current. To resolve this problem, we propose a NMOS-based power inverter as shown in the righthand side of Fig. 6. Both the pull-up and the pull-down devices are NMOS to generate high currents if activated.

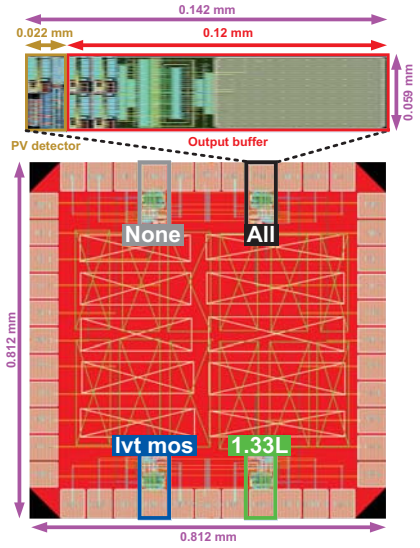

Fig. 10. Layout of the proposed output buffer.

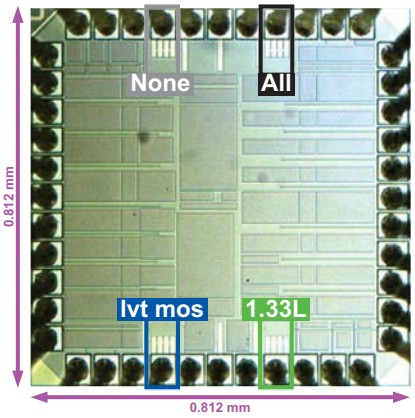

Fig. 11. Die photo of the proposed output buffer.

III. Implementation and Measurement

The proposed design is realized by TSMC 28 nm CMOS LOGIC Low Power ELK Cu 1P10M 1.05 & 2.5 V. Fig. 10 and Fig. 11 show the layout and the die photo of the prototype on silicon, respectively, where a single I/O buffer circuit is only 0.142×0.059 mm^2. The maximum data rate of the proposed design is measured to be 2.0 GHz given VDDIO=1.05/1.8V, respevtively, with the activated PV ccompensation, as shown in Fig. 12 and Fig. 13. Table VI summarizes the comparison of our work with several prior works. Apparently, the proposed design provides a very high speed all-corner-detected solution for 2×VDD data transmission on silicon with least chip area.

TABLE VI
PERFORMANCE COMPARISON OF OUTPUT BUFFERS

	[3] *TCAS-I 2013*	[5] *ISCAS 2013*	[6] *EDSSC 2014*	[8] *ISCAS 2016*	This work
Process (nm)	90	40	90	90	28
Implementation	measurement	simulation	simulation	simulation	measurement
VDD (V)	1.2	0.9	1.0	1.0	1.05
VDDIO (V)	2.5	0.9/1.8	1.0/1.8	1.0/2.0	1.05/1.8
Process Corner Detected	Only TT FF SS	All	All	All	All
Lock Time	One cycle	Tens of cycle	$\geq$ One cycle	One cycle	One cycle
Maximum Date Rate (MHz)	N/A	460	330/500	800/500	2000/2000
SR Variation Improvement (%)	37.5	6	N/A	33.9	33/36 (1.05V) , 31/39 (1.8V) (rise/fall, post-layout simulation)
Encoded compensation	NO	NO	YES	YES	YES
Core area (mm^2)	N/A	0.013	0.024	0.020	0.0084

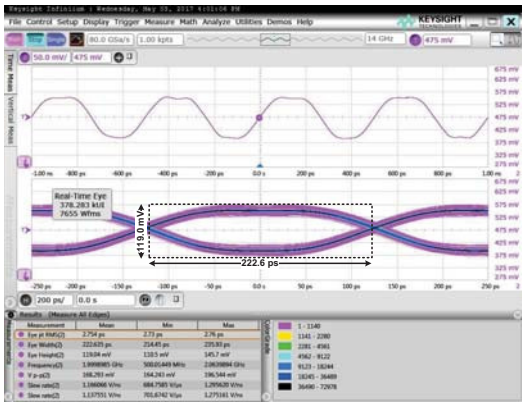

Fig. 12. Eye diagram with PV compensation given 1× VDD.

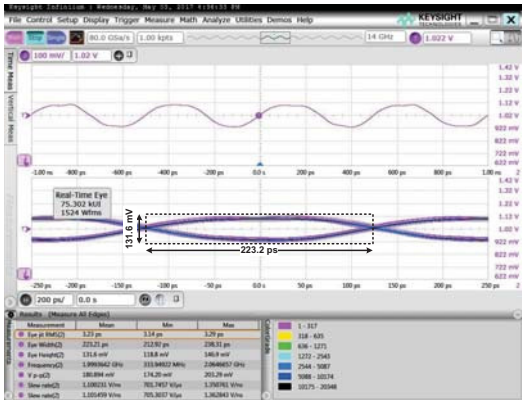

Fig. 13. Eye diagram with PV compensation given 2× VDD.

IV. CONCLUSION

A 2×VDD output buffer realized using 28 nm CMOS process is reported in this work. Note only is the slew rate varaiton reduced, the data rate is also dratically ehanced to GHz level. The data rate is measured on silicon as 2.0 GHz when VDDIO = 1.05/1.08 V, respectively, which is fastest mixed-voltage digital output buffer to date. The SR improvement is proved to be at least over 30% regardless in VDD or 2×VDD data transmission mode.

ACKNOWLEDGMENT

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