Disturb-free 5T Loadless SRAM Cell Design with Multi-Vth Transistors Using 28 nm CMOS Process

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Abstract—**A single-ended load SRAM cell composed of multi-Vth transistors is proposed in this study. Particularly, the PDP (power-delay product) performance of the loadless SRAM cell is enhanced by a write assistant loop and an isolated wordline-controlled transistor (WLC). Additionally, a shared bitline inverter is added on the column-wise bitline to boost the read access speed at the minimal expense of area cost. The energy dissipation per write/read operation is found to be 96.624/8.104 fJ provided that the SRAM cells is driven a 0.8 V VDD power supply using a typical 28 nm CMOS technology.**

***Keywords*—single-ended SRAM cell, loadless, power-delay product (PDP), multi-Vth transistor, disturb-free**

I. INTRODUCTION

As well noted, memory devices have long been the core of digital systems next to CPUs. Particularly, the cache of CPUs is usually composed of SRAMs to ensure high throughput. Thus, they have undoubtfully consumed a great portion of overall power consumption. 4-T loadless SRAM has been recognized as a possible solution for the lower power demanding SRAM [1], where low-V_{th} transistors are used as bit line drivers and high-V_{th} transistors are the data latch components. However, the read/write disturbance is queationable in such a cell due to lack of bitline isloation mechanism. The degration of the SNM (static noise margin) pointed out by [2] has verified such a potential hazard. In this study, a loadless SRAM with a write-assist loop to decouple the noise from bitlines during write operation to achieve disturbance free is analyzed. Furthermore, a shared read inverter is used to reject the potential bitline voltage variation so as to enhance the disturb-free feature. Notably, the SRAM cell itself is a 5-T design with a pair of ultra-high-V_{th} PMOS transistors to serve as the latch-like storage.

II. DISTURB-FREE 5T SRAM CELL

We propose a novel loadless SRAM cell in this study to resolve the R/W disturbance predicament in loadless SRAMs. Referring to Fig. 1, to reject the potential disturbance from the bitlines, we propose to insert one WL-controlled transistor (≈WLC), namely N3, between BLB and the cell. Besides, the sources of N1 and N2 are coupled to become the "write-assist loop", where the common mode noise coupled from GND will likely be rejected. Notably, N1 and N2 are driven by WA (word access) and WAB (word access bar), respectively.

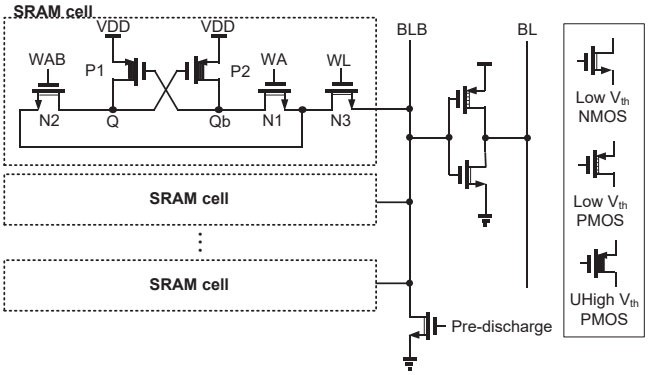

Fig. 1. Proposed disturb-free loadless SRAM cell

· **Read access** : The read operation timing diagrams are very much similar to those of 4T loadless SRAM [1] As soon as the address lines are valid, WL is asserted to turn on N3. Meanwhile, WA is high and WAB is low. The state at Qb will be passed to BLB via N1 and N3 to generate valid Data_out. Notably, a shared inverter is inserted between BLB and BL to reject the nose coupled in BL. Besides, the shutoff N2 will ensure Q is free from the disturbance of BLB.

· **Write access** : By contrast, the write operation timing diagrams are shown in Fig. 2. When "1" is to be writen, WL and WA are asserted to turn on N1, and N3, respectively. BLB is pre-discharged to ground such that a "0" is stored at Qb, which in turn switch on P1 to charge Q to high. By contrast, When "0" is writen, WL and WAB are pulled on to turn on N2 and N3, resptively, and BLB is also pre-discharged at the same time such that Q is pulled low.

Therefore, the proposed loadless 5T SRAM cell is a single-ended disturb-free design. Besides the R/W noise margins can be enhanced, the area cost is also drastically reduced compared with the known disturb-free design approaches. Notably, the inverter bewteen BLB and BL is shared by many SRAM cells, since only one cell in a single column is allowed to access the bitline pair in any single R/W cycle. The area overhead is obscure.

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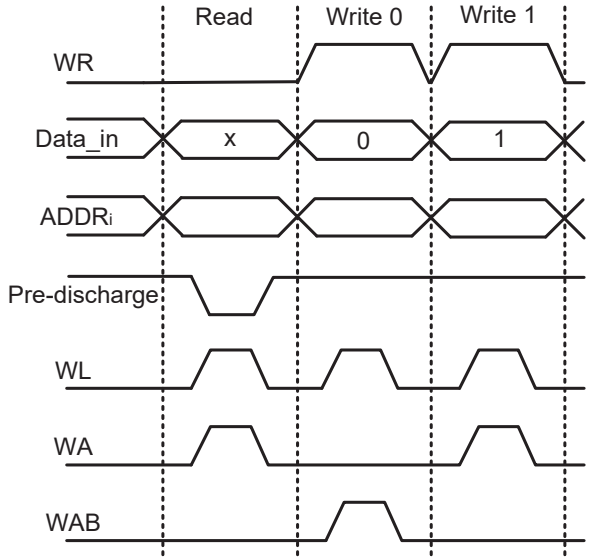

Fig. 2. Write timing diagram of the proposed loadless SRAM cell

III. Implementation and Simulation

Referring to Fig. 3, the area of the proposed cell is $0.52\times1.63\ um^2$ using a typical 28 nm CMOS process (TSMC).

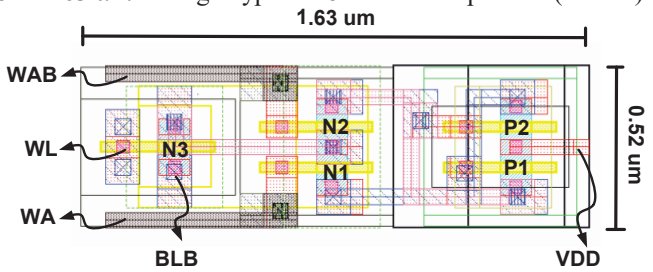

Fig. 3. Layout of the proposed SRAM cell

The worst-case read SNM of the proposed cell are shown in Fig. 4. Since one of the WAB and WA will be low to shut off one of the access NMOS, either Q or Qb will remain the same during the read operation, which is different from the conventional 6T-based SRAM cells. The worst-case SNM is found to be 363.60 mV (read), 800.31 mV (write), and 445.21 mV (hold), by all-PVT corner simulations, which is far better than the other single-ended SRAM update date. Most important of all, the write operation of the proposed cell is disturb-free in any case. The comparison with prior works based on all-PVT-corner post-layout simulations with VDD=0.8 V is tabulated in Table I. Notably, FOM is estimated by the following equation,

$$\mathrm{FOM} = \frac{\frac{SNM}{VDD}}{\frac{Write\ PDP}{VDD}\times\frac{Read\ PDP}{VDD}\times normalized\ CA} \qquad (1)$$

where CA denotes cell area. The proposed design outperforms the others with respect to the SNM, cell area, and write disturb-free. Besides, our design also attains the edge of quite balanced PDP in read/write operations.

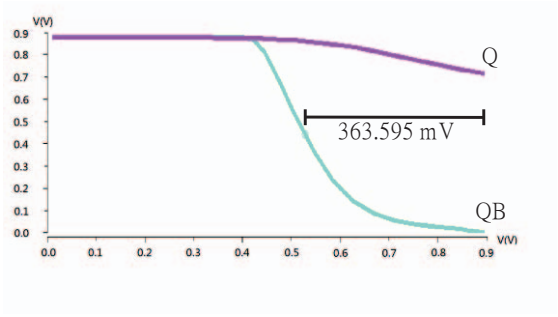

Fig. 4. Worst-case read SNM of the proposed SRAM cell

TABLE I

COMPARISON WITH PRIOR WORKS

	[3]	[4]	[6]	This work
Transistors	8T	9T	5T	5T
SNM (mV)	283.54	267.85	326.90	363.60
WM (mV)	281.90	N/A	N/A	N/A
Write PDP (fJ)	1.08	4.37	0.187	0.124
Read PDP (fJ)	0.248	0.039	0.130	0.0638
Cell Area (um^2)	3.96 ×0.8	3.625 ×1.18	2.05 ×1.12	1.63 ×0.52
VDD (V)	0.6	0.35	0.6	0.8
FOM	1.62	1.84	28.46	34.19
Year	2010	2011	2014	2016

Acknowledgment

This investigation is partially supported by Ministry of Science and Technology under grant MOST 104-2622-E-006-040-CC2. The authors would like to express their deepest gratefulness to Chip Implementation Center of National Applied Research Laboratories, Taiwan, for their thoughtful chip fabrication service and EDA tool support.

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