A Method Of Leakage Reduction And Slew-Rate Adjustment in 2×VDD Output Buffer For 28 nm CMOS Technology And Above

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***Abstract*—As the CMOS technology advancing rapidly, it becomes urgent to find a solution toward the suppress of rising leakage current. In recent researches, the optimization of MOS length was reported to decrease 30% subthreshold leakage current at the sacrifice of only several percent dynamic power and active area. Besides, Dual-Vth method was proposed to compromise the leakage current and the slew-rate (SR) performance. In this paper, the proposed 2×VDD output buffer with a novel PVTL (Process, Voltage, Temperature, Leakage) compensation circuit takes advantage of combining the two methods mentioned above to achieve 75% subthreshold current reduction in cutoff region, and better SR with the gate leakage trade-off. The proposed design is all-corner simulated at 800 MHz data rate and a 20 pF load given 1.05 V/1.8 V supply voltage using in a typical 28 nm CMOS process to justify the performance of the proposed compensation circuit.**

***Index Terms*—I/O buffer, PVTL variation, mixed-voltage tolerant, slew rate compensation, gate-oxide reliability, dual-vth**

I. Introduction

Advanced nano-scale CMOS technology has been widely applied in many types of chips over the last decade. The benefits of these nano-scale CMOS technologies have been recognized, including smaller power consumption, more transistors per area, lower supply voltage, and higher operation speed. However, many chips fabricated by legacy technologies are still in use such that it's very hard to couple them with nano-scale chips directly due to the voltage difference of logic signals. Therefore, an output buffer with mixed voltage levels are needed essentially to translate signals between these chips.

Several recent works have identified many critical problems of the mixed-voltage buffers such as SR self-adjusting [1]- [3], PVT variations [4], gate-oxide reliability [5], multiple voltage level [6]- [7], and leakage current. These problems are surely degrading the performance of nano-scale I/O buffers. This investigation is focused on the leakage current reduction and integration of prior design methods to compromise between leakage current reduction and SR improvement.

Referring to [8], an optimization method of subthreshold leakage current reduction was reported for 90 and 65 nm CMOS processes. It lengthens the MOS to attain 35% leakage reduction with 10% of active area and delay penalties. Another method to improve the SR performance suggested to take advantage of the dual-vth feature [9]- [12]. That is, certain transistors are realized with low-vt transistors to suppress static DC currents, which significantly reduces power consumption up to 70%, and enhances the speed up to 78% after comparing with previously well-known level converters [13].

A 2×VDD output buffer using the dual-vth feature to compromise leakage current and SR performance is disclosed in this study, where MOS's length is stretched analytically to reduce subthreshold leakage current such that the power saving is achieved.

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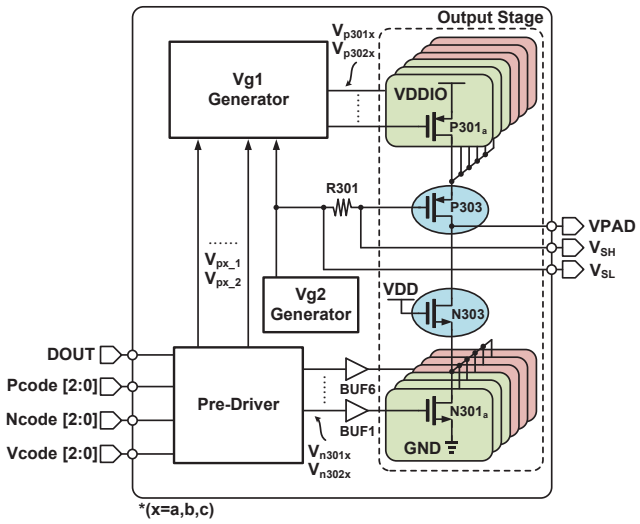

Fig. 1. The block diagram of the proposed output buffer.

II. Mixed-voltage Buffer Circuit Design

Fig. 1 shows the block diagram of the proposed 2×VDD output buffer comprising Pre-Driver, Vg1 Generator, a sensing

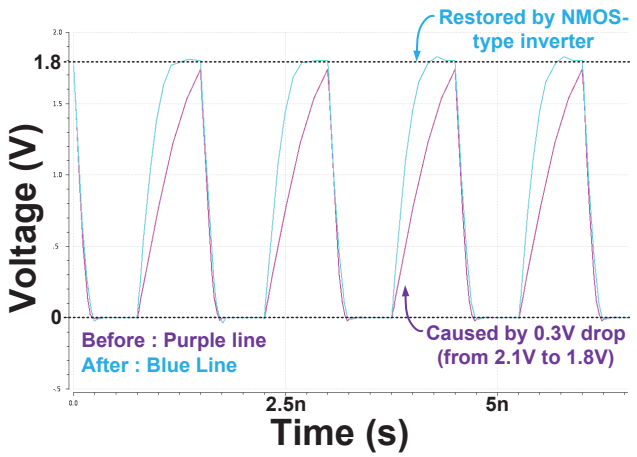

Fig. 2. Simulation of VPAD before and after the replacement of inverter.

resistor, Vg2 Generator, and Output Stage. Notably, the sensing resistor is added to monitor the leakage current of P303. The former 2 blocks will be briefly discussed, and the latter 2 blocks will be discussed detailedly in the following text.

A. Pre-Driver

Pre-Driver is a combinational logic circuit, which generates control signals corresponding to Dout, Pcode [2:0], Ncode [2:0], and Vcode [2:0] to compensate SR. Notably, DOUT is the signal from the digital core. Pcode [2:0], Ncode [2:0], and Vcode [2:0] are 3-bit codes from Process and Voltage sensor (not shown) [14]. When DOUT is logic 0, V_{p301x} and V_{p302x} will determine the discharging current paths. On the contrary, when DOUT is logic 1, V_{px_1} and V_{px_2} will determine the charging current paths. Notably, x denotes a, b, or c for corresponding MOS transistors.

B. Vg1 Generator

Vg1 Generator is used to boost up voltage when VDDIO equals 2×VDD. Notably, the boosted voltages must meet the G-S, D-S voltage drop requirements to avoid gate-oxide over-voltage hazards. By contrast, the voltage of the generated signals will remain the same when VDDIO equals 1×VDD.

C. Vg2 Generator

As shown in Table I, the output voltage V_{SL} of Vg2 Generator will be determined by the VDDIO voltage. In other words, when VDDIO = 1×VDD, V_{SL} is hold to the ground. Otherwise, V_{SL} is boosted to 1×VDD when VDDIO = 2×VDD. However, it is not practical for the real scenario when 2×VDD equals 2.1 V in low-voltage nano-scale CMOS design due to the possible over-voltage stress. Therefore, we set 2×VDD to 1.8 V instead of 2.1 V.

However, the 0.3 V voltage drop (from 2.1 V to 1.8 V) will lead to poor SR performance as shown in Fig. 2 (purple line). We propose a novel inverter composed of two NMOS transistors to be added at the V_{SL} as shown in Fig. 3 (a).

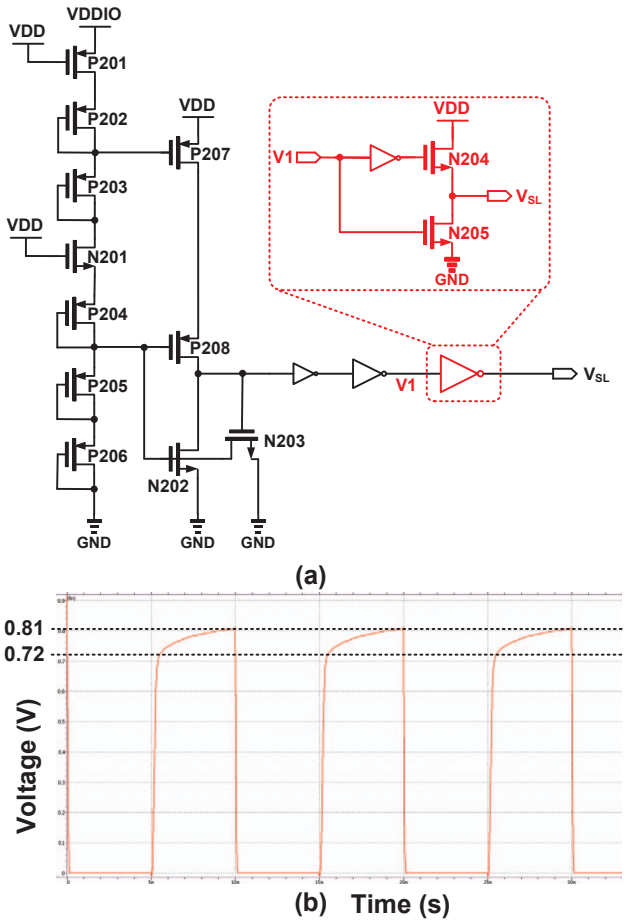

Fig. 3. (a) Schematic of Vg2 Generator ; (b) Simulation of NMOS type inverter.

TABLE I
VOLTAGE LEVELS OF VG2 GENERATOR

VDD	VDDIO	V_{SL}
1.05 V	1.05 V	0 V
1.05 V	1.80 V	0.75 ∼ 1.05 V
1.05 V	2.10 V	1.05 V

The poor SR is then fully restored as shown in Fig. 2 (blue line). Notably, Fig. 3 (b) shows the voltage of the NMOS-type inverter is kept within 0.72 V to 0.81 V when the output voltage is logic 1.

TABLE II
LEAKAGE OF DIFFERENT MOS STATUS

MOS status	Gate leakage current	Subthreshold leakage current	Leakage reduction
Standard	2.16 (nA)	480 (nA)	
Standard +20%	2.16 (nA)	125.5 (nA)	74%
Low-vt	2.16 (nA)	5.12 (μA)	
Low-vt +20%	2.16 (nA)	1.28 (μA)	75%

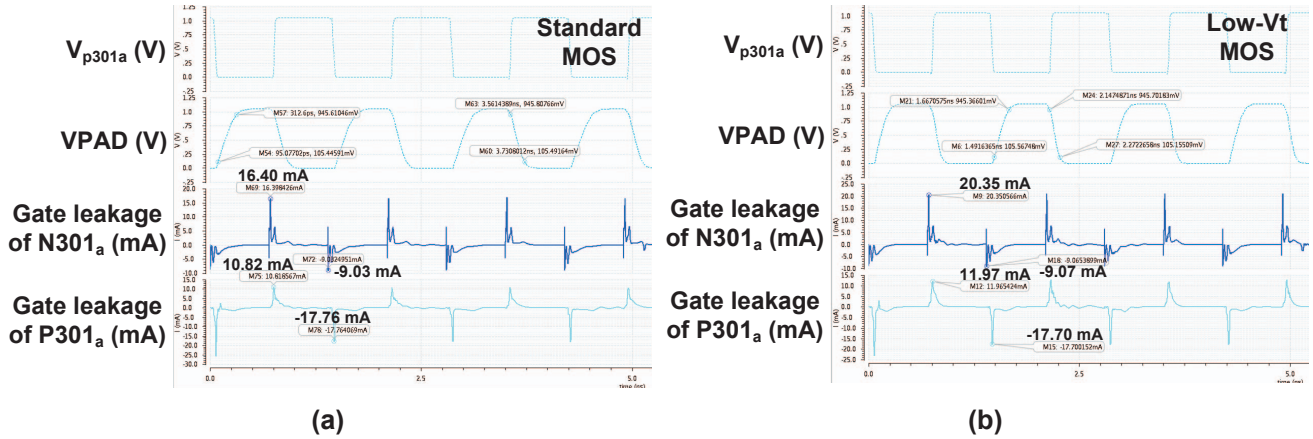

Fig. 4. Gate leakages of standard or low-vt MOS.

D. Output Stage

Those PMOS transistors in the output stage are very wide ($\sim$1200 μm) for the sake of generating large output driving current. Thus, large leakage current is inevitable. Table II summarizes the leakage current of standard and low-vt PMOS with or without 20% more MOS length. Notably, even if the PMOS transistor is biased to completely shut down, the gate leakages remain the same. Since the large transistors in the output stage will be turned off frequently, the length of these MOSs should be stretched 20% long to reduce subthreshold leakage current.

According to the simulation results in Fig. 4 (a) and (b), the gate leakage current will be gigantic when MOS is in the transition between turning on and off regardless of MOS types. The gate leakage current, however, is relatively small when VPAD stays at logic 1 or 0.

Referring to the Output Stage in Fig. 1 again, the transistors in blue region, namely P303 and N303, in our design are always turned on. Because their transition time is shorter than that of the transistors in green and red region, P303 and N303 should be replaced with low-vt MOS to fasten the SR.

III. Simulation and Discussion

This work is designed and fully simulated at all PVT corners using 28 nm CMOS LOGIC Low Power ELK Cu 1P10M technology. Table III shows the comparison SR performance of different combinations in Output Stage at normal corner (TT, 25°C, 1×VDD). It turns out to prove that the combination usage of standard and low-vt MOS is feasible and probably an optimal solution to compromise SR performance and the leakage.

Referring to Fig. 5, when VDDIO = 1.05 V, the SR variation improvement is 48.1%/42.8% of the rising/falling edge, respectively. On the other hand, when VDDIO = 1.80 V in Fig. 6, the SR variation improvement is 39.3%/32.3% of the rising/falling edge, respectively.

TABLE III
SR Impact of Different MOS Combinations

	All Standard	Standard+low-vt	All low-vt
SR_{rise}	3.87 (V/ns)	5.35 (V/ns)	4.94 (V/ns)
SR_{fall}	4.94 (V/ns)	5.91 (V/ns)	6.46 (V/ns)

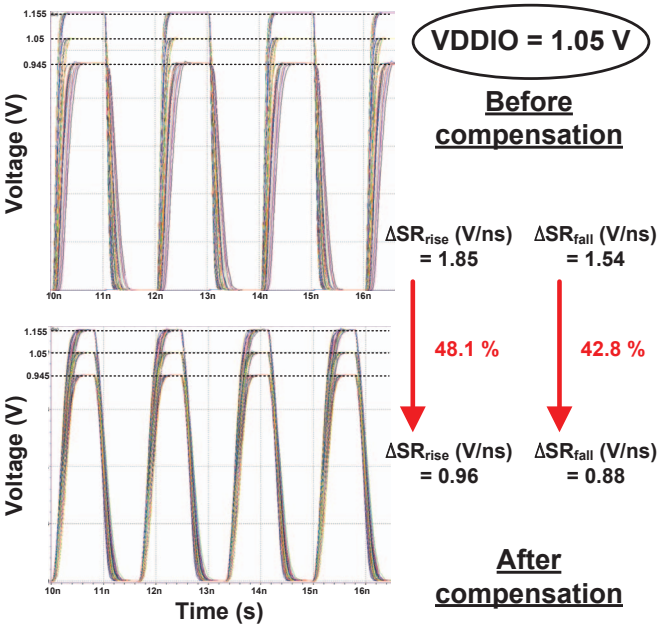

Fig. 5. The all-corner simulations of VPAD with VDDIO = 1.05 V.

Table IV tabulates the comparison of this study with several prior works. The proposed design is the only one to utilize dual-vth transistors and MOS's length extension as a solution to achieve better SR performance.

TABLE IV
PERFORMANCE COMPARISON OF OUTPUT BUFFER

	[5] *TCAS-I 2013*	[6] *ISCAS 2013*	[7] *EDSSC 2014*	[10] *ISCAS 2016*	This work
Process (nm)	90	40	90	90	28
VDD (V)	1.2	0.9	1.0	1.0	1.05
VDDIO (V)	2.5	0.9/1.8	1.0/1.8	1.0/2.0	1.05/1.8
Maximum Date Rate (MHz)	N/A	460	330/500	800/500	800/800
SR Variation Improvement (%)	37.5	6	N/A	24.8 (Worst case)	42.8/32.3 (Worst case)
Encoded compensation	NO	NO	YES	YES	YES
Core area (mm^2)	N/A	0.013	0.024	0.020	N/A

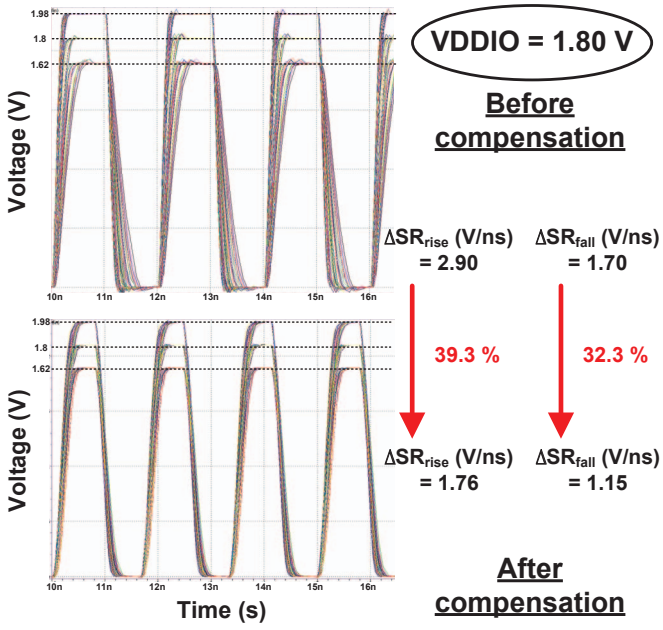

Fig. 6. The all-corner simulations VPAD with VDDIO = 1.80 V.

IV. CONCLUSION

In recent studies, stretching MOS length has been considered as a good solution to suppress the subthreshold leakage current. Besides, the dual-vth transistor usage method is an option to reduce static DC current. Therefore, based on these two methods, a 2×VDD output buffer using dual-vth transistors to compromise leakage currents and SR performance is disclosed hereby where MOS's length is stretched to reduce subthreshold leakage current. The data rate is found to be 800/800 MHz with the 20 pF load at the pad when VDDIO = 1.05/1.80 V, respectively. The maximum SR variation improvement is 48.1% at rising edge when VDDIO = 1.05 V.

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