On-chip Accurate Primary-side Output Current Estimator for Flyback LED Driver Control

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***Abstract*—A flyback control circuit with a primary side output current estimator is designed on chip and analyzed in this investigation. The flyback control circuit plays a key role of lighting systems, where the LED current estimator and the diode conduction period detector are proposed for the accuracy of LED driver control. The LED current estimator generates a voltage proportional to the LED current. The diode conduction period detector is in charge of estimating correct conducting period to prevent misjudgment of the cycle period. Detailed analysis, including prediction voltage of the LED current and period of the diode, is reported. The post-layout simulations of the proposed current estimator demonstrate the maximum error $\leq$ 3.08 %, and the efficiency is 89.45 %.**

***Index Terms*—primary side, current estimator, flyback LED driver, diode conduction period, PWM**

I. Introduction

In recent years, white LED (WLED) is gradually and widely used in residential lighting, automobile lighting, portable lighting, street lighting, etc. The LED drivers need to keep pace with advancement of the LED technology, including the power management, such as pulse width modulation (PWM) controllers. For instance, to achieve higher lightness, WLED demands a higher current with higher voltage drop, with respect to conventional LEDs. The LED or WLED driver is critical to supply a stable current.

Kleebchampee *et al.* proposed a flyback LED driver [1]. An optocoupler isolates the secondary side from the primary side, which generates a stable voltage. However, this flyback driver system consumes a large current such that the switching components are suffered from high voltage stress. High peak current is another critical problem for this flyback driver in discontinuous conduction mode (DCM) and boundary conduction mode (BCM). Lin *et al.* proposed a primary side control IC, including a sampling feedback voltage loop circuit and a knee point detector, to keep duty cycle as constant as possible [2]. However, when the output voltage of the bridge rectifier (Vin) is close to zero, the current of the primary winding and the drain to source voltage of the power MOS switch will vary drastically. Thus, the control IC must be reacted quickly enough to detect the valleys of the feedback signal. Otherwise, the control IC will miss the valley signals to result in hazards in LEDs. Moreover, the output feedback current will be ignored or underestimated [3]. Xu *et al.* reported a primary side control scheme for Triac compatible LED drivers. However, the constant input power control circuit and harsh output current regulation are difficult to achieve [3].

A primary side output current estimator for flyback LED drivers is proposed in this work to resolve the mentioned problems, as shown in Fig. 1. Detailed schematic and analysis of the proposed design will be given in Section II. Section III will demonstrate thorough simulation results to justify the performance of the LED current estimator and the diode conduction period detector designs. A conclusion is drawn in Section IV.

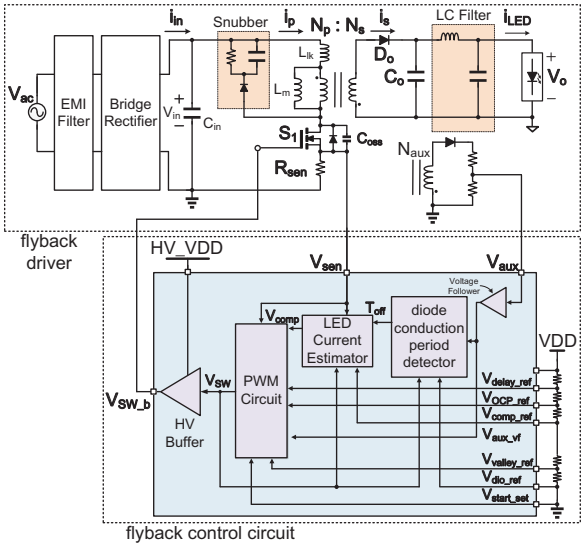

Fig. 1. Block diagram of the proposed flyback LED driver system.

II. Architecture of Flyback LED Driver

Fig. 1 shows our flyback LED driver system, including a flyback driver and a flyback control circuit. The flyback LED driver suppresses the conducted interference of AC voltage (V_{ac}) by rectifying it into a high DC voltage. The inductor of flyback is split to work as a transformer. Therefore, the flyback LED driver is turned into a buck-boost converter. Finally,

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the flyback control circuit determines the turn-on time of the switch (S_1) generating a varying magnetic field in the primary winding. The energy of the primary winding is transferred to the secondary winding via electromagnetic induction, thereby charging the output capacitor (C_o). The output voltage of the auxiliary side is detected by the flyback control circuit such that it auto-adjusts the turn-on time of the S_1 to keep a fixed output current (i_{LED}).

Waveforms of those signals during lighting operation are shown in Fig. 2. Notably, the peak of the primary side current is $i_{p,peak}$. Assume n is the primary-to-secondary transformer turn ratio, N_p/N_s. The peak secondary side current ($i_{s,peak}$) is derived as follows.

$$i_{s,peak} = n \cdot i_{p,peak} \tag{1}$$

The flyback control circuit is composed of a PWM circuit, a LED current estimator, a diode conduction period detector, and a voltage follower. The PWM circuit generates a gate drive on S_1. A turn-off signal is generated by the output of the LED current estimator compared with the sawtooth wave from the PWM circuit. Thus, the brightness of the LED can be adjusted by tuning the period of the PWM circuit. The LED current estimator generates a voltage proportional to the current of the S_1, if S_1 is turned on. The diode conduction period detector is in charge of estimating the conducting period as accurate as possible.

When S_1 is turned on, a current flows through primary side and the energy is stored in the winding. The diode (D_o) is cut off because the voltage induced in the secondary side is negative. Moreover, the voltage of the auxiliary side (V_{aux}) is also negative. V_{aux} can be written as Eqn. (2).

$$V_{aux}(t) = \frac{-N_{aux}}{N_p} \cdot V_{in}(t), \quad t_0 \le t < t_1 \tag{2}$$

where N_{aux} is the winding turns of the auxiliary side.

By contrast, the current of primary side winding drops immediately as soon as the S_1 is turned off. The voltage of the secondary side becomes positive such that D_o is forward biased allowing current to flow from the transformer. The capacitor is then recharged to supply energy to the load. In addition, the voltage of the auxiliary side is also positive. V_{aux} can be written as Eqn. (3).

$$V_{aux}(t) = \frac{N_{aux}}{N_s} \cdot V_o(t), \ t_1 \le t < t_2 \tag{3}$$

Primary side winding and the parasitic capacitor consist of a resonant circuit when the energy of transformer runs out. Therefore, the voltage of the auxiliary side also oscillates just like the scenario of the primary side. Finally, the diode clamps the negative voltage to prevent flyback control circuit from breakdown.

Because the average current of the LEDs (i_{LED}) equals to the average current of i_s, i_{LED} in one on-off period is simplified as follows according to Fig. 2.

$$i_{LED,avg} = i_{s,avg} = \frac{1}{T_s} \cdot \int_{t_0}^{t_3} i_s(t)dt = \frac{1}{T_s} \cdot \left(\frac{1}{2} \cdot i_{s,peak} \cdot T_{off}\right) \tag{4}$$

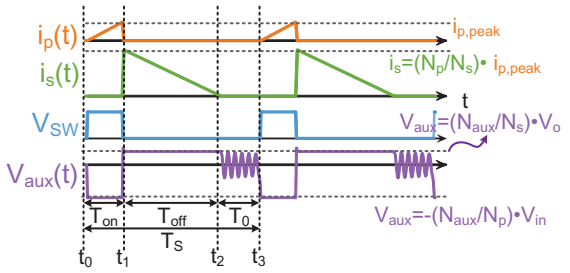

Fig. 2. Waveforms of several signals during lighting operation

Eqn. (4) can be re-organized as follows.

$$i_{LED,avg} = \frac{1}{T_s} \cdot \left(\frac{1}{2} n \cdot i_{p,peak} \cdot T_{off}\right) = \frac{1}{2} n \cdot i_{p,peak} \cdot \frac{T_{off}}{T_s} \tag{5}$$

A. Diode Conduction Period Detector

Fig. 3 shows the schematic of the diode conduction period detector. This circuit is designed to prevent misjudgment of the diode conduction period caused by the oscillation of V_{aux}. Referring to Fig. 2, V_{aux} is raised when the S_1 is turned off. Thus, T_{off} is pulled high and kept steady, as shown in Fig. 3 (a). Moreover, the rise of T_{off} indicates that D_o is forward-biased. By contrast, T_{off} is pulled down when the first falling edge of V_{aux} is detected in the same period. Since V_{sw} stays low, this circuit will neglect the rising edge caused by the oscillation of V_{aux}, as shown in Fig. 3 (b). In addition, the fall of T_{off} indicates that D_o is reverse-biased.

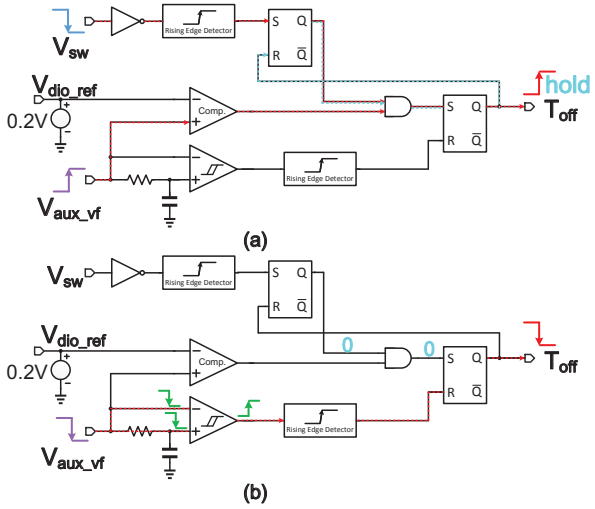

Fig. 3. Schematic of the proposed diode conduction period detector when S_1 is (a) turned off, and (b) turned on

B. LED current estimator

The LED current estimator in Fig. 4 consists of 4 transistors, 2 transmission gates, 2 resistors, 2 capacitors and a compensator. The source voltage of S_1 (V_{sen}) is converted into a sample current (i_1) by an error amplifier (EA), 2 transistors,

and a resistor. Referring to Fig. 1, V_{sen} and the current of the primary side (i_p) is assumed reasonably as Eqn. (6).

$$V_{sen}(t) = i_p(t) \cdot R_{sen} \tag{6}$$

Therefore, i_1 can be derived as follows.

$$i_1(t) = \frac{V_{sen}(t)}{R_{CE}} = \frac{i_p(t) \cdot R_{sen}}{R_{CE}} \tag{7}$$

The current mirror consisting of MP1 and MP2 duplicates i_1 to i_2 when the switch (S_2) is turned on by the PWM circuit. Then, the i_2 current charges an RC (R_{CE} and C_2) circuit. Therefore, the output voltage of the LED current estimator (V_{av}) is proportional to the current of S_1 when it is turned on. V_{av} is written as Eqn. (8).

$$V_{av}(t) = i_2(t) \cdot R_{CE} = \begin{cases} 0 & , \ t_0 \le t < t_1 \\ i_{p,peak} \cdot R_{sen} & , \ t_1 \le t \le t_2 \\ 0 & , \ t_2 < t \le t_3 \end{cases} \tag{8}$$

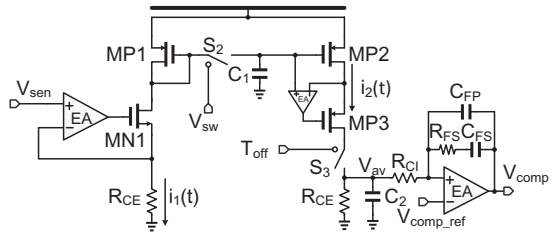

Fig. 4. Schematic of the proposed LED current estimator.

If the average over time is considered, V_{av} is re-organized as follows.

$$V_{av} = \frac{1}{T_S} \int_{t_1}^{t_2} V_{av}(t)dt = \frac{T_{off}}{T_S} \cdot i_{p,peak} \cdot R_{sen} \tag{9}$$

V_{av} is then concluded as Eqn. (10) when Eqn. (5) is considered.

$$V_{av} = \frac{2R_{sen}}{n} \cdot i_{LED} \tag{10}$$

Therefore, i_{LED} can be indirectly estimated by V_{av} with an appropriate aspect ratio $\frac{2R_{sen}}{n}$. Finally, the compensator compensates original zero pole and polar pole to provide sufficient phase margin. Thus, the flyback LED driver system remains stable. The compensation network transfer function can be deduced as follow.

$$\frac{V_{comp}}{V_{av}} = \frac{sR_{FS}C_{FS} + 1}{sR_{CI}(C_{FP} + C_{FS})(sR_{FS}\frac{C_{FP}C_{FS}}{C_{FP}+C_{FS}} + 1)} \tag{11}$$

C. Pulse Width Modulation

PWM circuit in Fig. 5 is a control signal generator of the power MOS switch. In one on-off period, V_{sw} is pulled high when V_{ct} is more than V_{sw_set}. Than, since V_{ct} is continuously raised higher than V_{comp}, V_{sw} will be pulled down. Further, the valley detector detects first valley of the V_{aux} when oscillation occur in V_{aux}. Thus, V_{valley_inv} is pulled down and V_{fb} is pulled high to drop V_{ct}. At last, S_2 is pulled down when V_{ct} is less than V_{valley_en}. Furthermore, V_{ct} is continuously decreased until V_{ct} is less than V_{sw_set}. On the other hand, LED should be able to provide high current tolerance, i.e., maximum 3 A [4]. If the current of LED is higher than 3 A due to abnormal operations, the over current protection is activated to turn off V_{sw}.

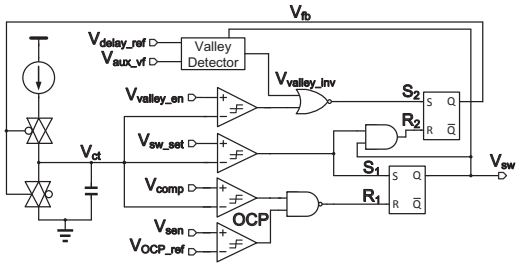

Fig. 5. Schematic of the proposed PWM.

D. High-voltage Buffer

The high-voltage (HV) BCD process offers HV devices and low-voltage (LV) devices. The voltage limitation of those LV devices is 5 V between any two terminals. By contrast, the voltage limitation of those HV devices is 12 V between any two terminals. Referring to Fig. 6, the HV buffer provide such a voltage level conversion is disclosed. If V_{sw} is 5 V, V_{sw_b} is the same as HV_VDD, i.e., 12 V.

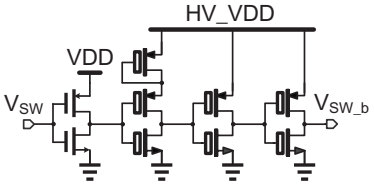

Fig. 6. Schematic of the proposed HV Buffer

III. Implementation and Simulation

The proposed primary side output current estimator of the flyback LED driver is carried out using TSMC 0.25 μm CMOS high volatge mixed siganl general purpose IIA based BCD 60 V. Fig. 7 shows the layout, where the overall chip area is 412.164×838.943 μm^2. The post-layout simulation results of the proposed flyback LED driver are shown in Fig. 8. An asymptote line from V_{av} results of Fig. 8 is concluded in Fig. 9. The proposed circuit has the worst-case 3.08 % prediction error of the current when V_o is 11.8 V. Take a LED string consisting of $2 \sim 8$ cascaded Cree LED cells as a load. The efficiency of the proposed flyback LED driver for 7 cases is summarized in Fig. 10. The efficiency has the worst-case 89.45 % when LED number is 2 (17.14 Ω). The power consumption is 165.8 mW at 2 LEDs. The performance comparison of the proposed design and several recent works is tabulated in Table I. Notably, our design works in the range of $12.07 \sim 47.66$ V, with the least maximum error around 3.08 %.

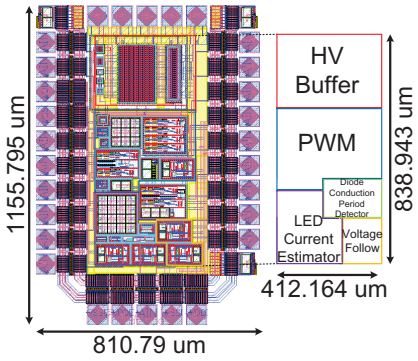

Fig. 7. Layout of the proposed primary side output current estimator

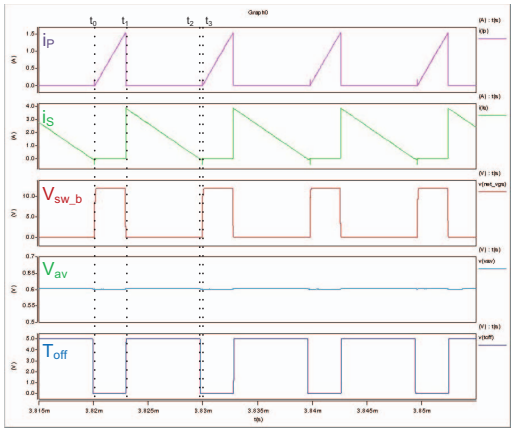

Fig. 8. Post-layout simulation of the proposed design

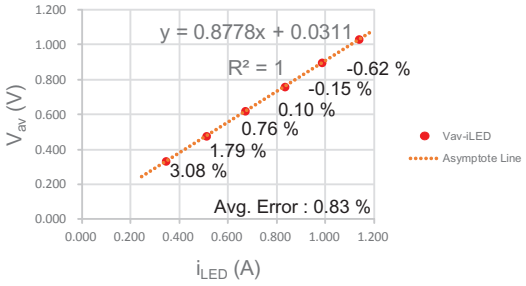

Fig. 9. V_{av} error of the LED current estimator

IV. Conclusion

In this paper, a primary side output current estimator of flyback control circuit IC is proposed. This work prevents misjudgment of the period when the resonance between inductor and capacitor of the S_1. Then, the primary side current is directly used for output current estimation. In summary, post-layout simulations of the proposed output current estimator demonstrates maximum error 3.08 % when the V_o is 11.8 V. In addition, the efficiency is 89.45 % when LED number is 2 (17.14 Ω).

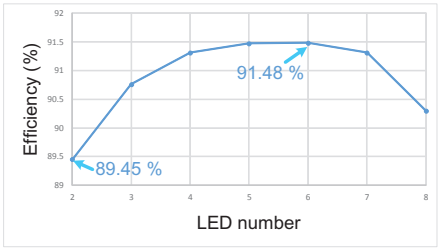

Fig. 10. The efficiency of the proposed design

TABLE I
Performance Comparison of Current Estimator

	[5] APEC	[6] APPEEC	[7] TPE	This work
Year	2010	2014	2014	2016
Implementation	PCB	FPGA	0.5 μm 5-V CMOS	0.25 μm HV CMOS
Switch Frequency (kHz)	100	20 ∼ 500	4000	50
Input Voltage Range (V)	360	N/A	2.7 ∼ 5.5	5
Output Voltage Range (V)	24	N/A	0.6 ∼ 3.3	11.8 ∼ 39
Max. Estimation Error (%)	6.57	5	4	3.08
Efficiency (%)	N/A	N/A	88	89.45
Power (W)	192	N/A	1.65	0.165
Chip Area (mm^2)	N/A	N/A	2.25	0.346

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