A Nano-scale 2×VDD I/O Buffer with Encoded PV Compensation Technique

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***Abstract*—A 2×VDD I/O buffer with process and voltage (PV) compensation technique is proposed. In this research, the purpose of slew-rate compensation is to maintain slew rate (SR) within predefined ranges regardless PV variations. The reason of temperature variation is not considered is that it is found to be a relatively low correlation factor to slew rate for 90 nm process. All bias voltages in process and voltage variation detectors are generated from bandgap circuits such that variations have been guaranteed by simulation within less than 3.57%. Notably, we add a resistor in series of MOS gate to trace leakage current of wide transistors with a -0.1 (V/ns) on SR for trade off. The data rate is 800/500 MHz given 1.0/2.0 V supply voltage with 20 pF load, respectively, by all-corner simulations. The △ SR improvement is 33.9% and 29.8% in the rising time, and 29.1% and 24.8% in the falling time of 1×VDD and 2×VDD, respectively. The core area is 0.052 × 0.388 mm^2.**

***Index Terms*—I/O buffer, PV variation, mixed-voltage tolerant, slew rate compensation, gate-oxide reliability.**

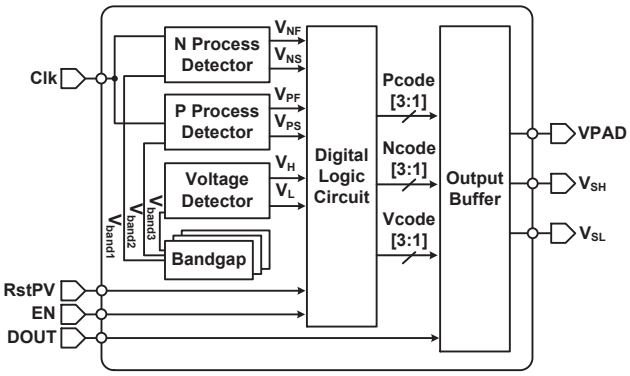

Fig. 1. Block diagrams of the proposed 2×VDD I/O Buffer.

I. Introduction

CMOS technologies have been developed rapidly with advantages including low supply voltage, low fabricating cost per area, and low power consumption. However, many recent applications would likely choose a legacy process for cost effectiveness purpose. Therefore, when a PCB-based system is equipped with many generations of chips, it will certainly need I/O buffers with mixed-voltage tolerance to communicate each other.

TABLE I
Comparison of Variation Factors to Slew Rate

VDD (V)	Corners	Temp. (°C)	ΔRise (V/ns)	ΔFall (V/ns)	Correlation Ratio (Rise/Fall)
0.9-1.1×VDD	TT	25	2.08	1.93	4.1/3.64
1×VDD	All	25	1.78	1.74	3.63/3.28
1×VDD	TT	0-100	0.49	0.53	1/1

As for I/O interfaces, the up-to-date DRAM product standard is DDR4 (Double Data Rate Fourth Generation) which arises to satisfy HPC (High Performance Computing system) requirements. The minimum SR limitation is 4 V/ns. Many researches in the past few years have been proposed to resolve problems given such a harsh SR condition such as overstress problems, PVTL variations, which were mainly based on stacked architecture and variation detectors to compensate SR and increase reliability, respectively [1]-[6]. Besides, an improved digital-based process detector was also reported to simplify the detection mechanism and increase the detection speed [7].

Temperature variation to SR is compared with process and voltage variations to SR, as shown in Table I. The simulation was conducted by a Monte-Carlo simulation (100 times) given 1V, TT, 25°C typical circumstance, where each simulation change one variable (P, V, or T) a time to see the difference resulted from each variation. When the impact of the temperature is assumed as 1 in the ratios both at rising and falling edges, the impact of voltage and process is 3 times larger than that of the temperature. Therefore, the temperature detection is not considered in this design.

In order to shorten the SR deviation caused by process and voltage variations, we propose to encode these signals into Output Buffer to compensate the SR. The delay mismatch resolution mentioned in [7] is also adopted in this design. The data rate of the proposed 2×VDD I/O buffer is up to 800/500 MHz by thorough simulations.

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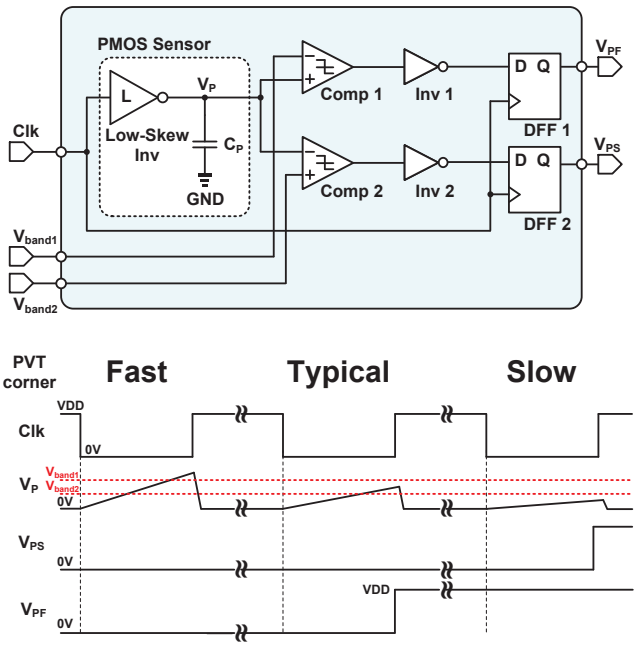

Fig. 2. Schematic of P-PVT Variation Detector.

II. 2×VDD I/O Buffer Design

Referring to Fig. 1, the proposed I/O buffer consists 2 Process Detectors, 1 Voltage Detector, 3 Bandgap circuits, 1 Digital Logic Circuit, and 1 Output Buffer. Clk is the system clock. RstPV and EN are 2 control signals for Digital Logic Circuit. More details will be given down below.

A. P Process and N Process Detectors

Fig. 2 reveals the schematic of P Process Detector and the illustrative waveforms for detecting. It is composed of PMOS Sensor and 2 comparators for distinguishing different corners. Low-Skew Inverter in PMOS Sensor charges C_P in a rate corresponding to the corner where the circuit resides. 2 signals, namely V_{PF} and V_{PS}, are generated for further encoding. Notably, N Process Detector design is similar to that of P Process Detector. Table II shows the function table of P Process and N Process Detectors.

TABLE II
Function Table of Process Detectors

P Process Detector			
PVT corner	V_P	V_{PF}	V_{PS}
Fast	$V_P > V_{band1} > V_{band2}$	Logic 0	Logic 0
Typical	$V_{band1} > V_P > V_{band2}$	Logic 1	Logic 0
Slow	$V_{band1} > V_{band2} > V_P$	Logic 1	Logic 1
N Process Detector			
PVT corner	V_N	V_{NF}	V_{NS}
Fast	$V_N > V_{band2} > V_{band3}$	Logic 0	Logic 0
Typical	$V_{band2} > V_N > V_{band3}$	Logic 1	Logic 0
Slow	$V_{band2} > V_{band3} > V_N$	Logic 1	Logic 1

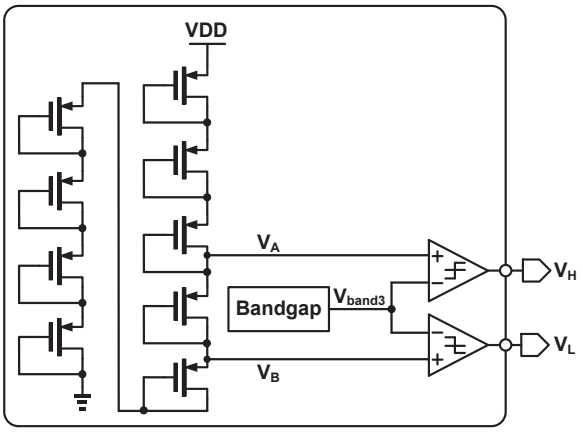

Fig. 3. Schematic of Voltage Detector.

B. Voltage Detector

Fig. 3 shows the schematic of Voltage Detector. In order to directly sense the variation of VDD between ±10% VDD, we use 9 diode-connected PMOS as resistors to separate VDD into 3 subranges : VDD ∼ V_A, V_A ∼ V_B, V_B ∼ GND. It is easy to tell what the voltage variation is by such a configuration. Considering Voltage Detector affected by process and temperature variations, the 9 PMOS transistors have the same size. Although the resistance of diode-connected MOS under different variations will drift, the voltages, V_A and V_B, are equally drifted as well. Therefore, when it comes to ±10% VDD variations, the output voltage of the bandgap circuit will be fluctuated between +1.49% and -1.26%. Detailed function is summarized in Table III.

TABLE III
Function Table of Voltage Detector

Voltage Level	V_H	V_L
+10% VDD	Logic 1	Logic 1
VDD	Logic 1	Logic 0
-10% VDD	Logic 0	Logic 0

C. Digital Logic Circuit

Process Detector and Voltage Detector deliver compensation signals, namely V_{PF}, V_{PS}, V_{NF}, V_{NS}, V_H, and V_L, to Digital Logic Circuit. EN forces Output Buffer to turn on all current paths. RstPV is in charge of turning on compensation mechanism. Then, Pcode [3:1], Ncode [3:1], and Vcode[3:1] are generated by hard-wired logic circuit to drive different current paths of Output Buffer. Notably, the priority of signal EN is higher than that of RstPV.

D. Output Buffer

The schematic of Output Buffer is shown in Fig. 4, consisting of Pre-Driver, Vg1 Generator, Vg2 Generator, Output Stage, and a sensing resistor R301. Pre-Driver receives the

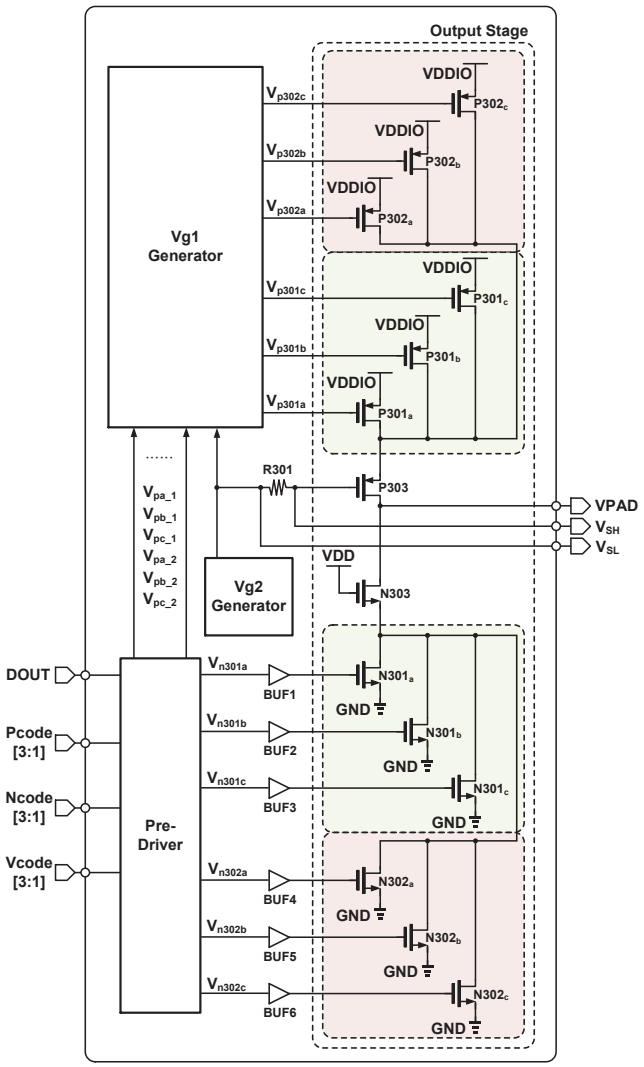

Fig. 4. Schematic of Output Buffer in Fig. 1.

TABLE IV
VOLTAGE LEVELS OF I/O BUFFER SIGNALS

VDDIO(V)	V_{p301x},V_{p302x}(V)	V_{SL}(V)	V_{n301x},V_{n302x}(V)
1.0	0.0/1.0	0.0	1.0/0.0
2.0	1.0/2.0	1.0	1.0/0.0

input signal DOUT, Pcode [3:1], Ncode [3:1], and Vcode[3:1]. However, when it comes to 2×VDD scenario, the gate drives of PMOS transistors must be shifted up to prevent over-stressed problems such that Vg1 Generator plays an important role. Vg2 Generator detects the voltage level of VDDIO, which notifies Vg1 Generator to shift up the gate drives. Notably, the sensing resistor R301 is coupled at the gate of P303 to monitor the leakage current thereof. In practice, the leakage current is impossible to measure. Therefore, by monitoring the voltage drop across R301, we can manage to assess the leakage current. Table IV revealed the internal voltage levels

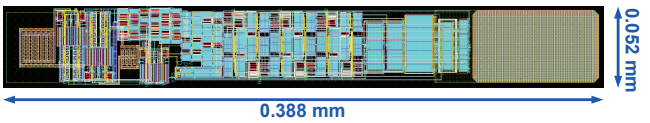

Fig. 5. Layout of the proposed I/O Buffer.

in Output Buffer. When VPAD is in the charging state (rise edge), the slew rate of VPAD can be expressed in Eqn. (1).

$$\begin{aligned} Q_{load} &= C_{load} \cdot (0.9 - 0.1) \cdot VDDIO = I_A \cdot T_C \\ T_C &= \frac{0.8 \cdot C_{load} \cdot VDDIO}{I_A} \\ SR_{rise} &= \frac{0.8 \cdot VDDIO}{T_C} = \frac{I_A}{C_{load}} \end{aligned} \quad (1)$$

where C_{load} is the load capacitor at VPAD, Q_{load} is the charge of the load capacitor, I_A is the charging current, T_C is the charging time. Firstly, the SR_{rise} is proportional to I_A. Secondly, no mater what region the transistor is, I_A is always proportional to the width of MOS. Therefore, SR_{rise} is also proportional to the transistor width. If the compensation factor $\alpha_{rise(max)}$ and $\alpha_{rise(min)}$ are given by specifications, e.g., DDR4, the appropriate width ratio can be delivered by the following equations.

$$SR_{rise(max)} = \alpha_{rise(max)} \cdot SR_{rise(mid)} \quad (2)$$

$$SR_{rise(min)} = \alpha_{rise(min)} \cdot SR_{rise(mid)} \quad (3)$$

where $SR_{rise(max)}$, $SR_{rise(min)}$, and $SR_{rise(mid)}$ are the SR when the circuit resides on FF, SS, and TT corners, respectively.

III. Implementation and Simulations

This work is realized by TSMC 90 nm CMOS Mixd Signal MS General Purpose Standard Process LowK Cu 1P9M 1.0 & 3.3 V. Fig. 5 shows the core layout of this work, where a single I/O buffer circuit is only 0.388 × 0.052 mm^2. Referring to Fig. 6 and 7, the slew rate enhancement of the rising edge is 33.9% and 29.8% and the falling edge is 29.1% and 24.8% for VDDIO = 1.0/2.0 V, respectively, when the proposed encoded PV compensation is activated.

Table V shows the comparison with several prior works. The proposed design is the only one to provide SR compensation such that it has 800 MHz data rate and meets DDR4 requirement (4 V/ns).

IV. Conclusion

A 2×VDD I/O buffer with the encoded PV compensation technique is reported in this work, which is realized using TSMC 90 nm CMOS process. The data rate is 800/500 MHz when VDDIO = 1.0/2.0 V, respectively. The encoded compensation technique is adopted to regulate slew rate. That is, when the process corner is faster than typical, it switches off current paths to slow it down. Otherwise, it switches on current paths to speed it up. Sensing resistors are embedded in this design to prepare for leakage measurement at the expense

TABLE V
PERFORMANCE COMPARISON OF OUTPUT BUFFER

	[3] *ICICDT 2012*	[4] *TCAS-I 2013*	[5] *ISCAS 2013*	[7] *EDSSC 2014*	This work
Process (nm)	90	90	40	90	90
VDD (V)	1.2	1.2	0.9	1.0	1.0
VDDIO (V)	0.9/1.2/1.8/2.5	2.5	0.9/1.8	1.0/1.8	1.0/2.0
Process Corner Detected	All	Only TT FF SS	All	All	All
Lock Time	Tens of cycles	One cycle	Tens of cycle	$\geq$ One cycle	One cycle
Maximum Date Rate (MHz)	300	N/A	460	330/500	800/500
SR Variation Improvement (%)	16	37.5	6	N/A	24.8 (Worst case)
Encoded compensation	NO	NO	NO	YES	YES
Core area (mm^2)	0.023	N/A	0.013	0.024	0.020

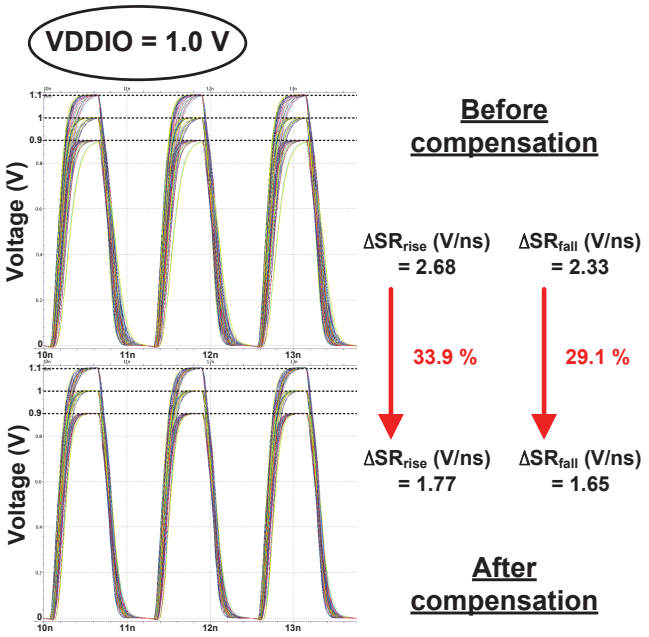

Fig. 6. Improvement of SR variation when VDDIO = 1.0 V.

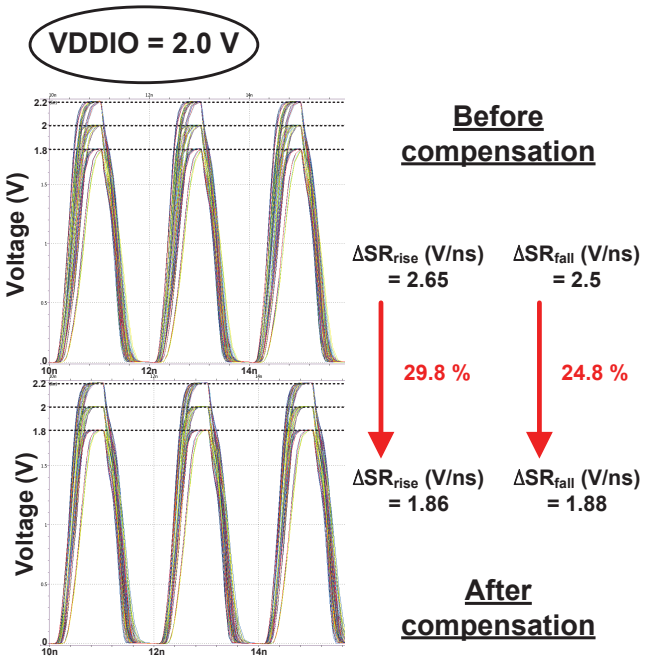

Fig. 7. Improvement of SR variation when VDDIO = 2.0 V.

of only 0.1 (V/ns) degradation for SR. The simulations of SR variation show that the difference of SR between corners can be reduced up to 33.9% when VDDIO = 1.0 V.

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