10 Mbps High-voltage Digital Transciever on Single Die for 50 V Voltage Swing

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***Abstract*— The proposed high-voltage (HV) digital transceiver comprises a pair of TX (transmitter) and RX (receiver) to exchange digital signals from different high-voltage domains. By taking advantage of the isolation capability of p-n junction provided by 800V 0.5 μm BCD CMOS process, a digital isolator is realized by a transformer which is able to be carried out with the TX and RX on the same die such that no off-chip bonding or discretes are needed. On-silicon measurements justify that the proposed HV digital transceiver demonstrates 10 Mbps data rate with 0.266 mJ/Mbps power dissiopation. This is by far the best performance for a single-die HV digital transceiver.**

***Keywords*—800V CMOS, single-die, coupled transformers, isolation, digital transmission**

I. Introduction

BMS (battery management system) has been recognized as the core of EVs (electrical vehicle) for future green transportation demand. BMS is in charge of monitoring battery modules consisting of many cells so that the status of each module and even each cell can be fully signaled back to a control center. However, since the battery modules are mainly compose of battery strings such that the voltage of those top cells will be very high. The cell or module status information in a digital format is very hard to be transmitted over these high-voltage (HV) cells and devices. Namely, the data communication among battery cells and modules in the BMS (battery management system) becomes a task to beat.

Discrete devices, e.g., opto-coupler, magnetic isolator, or capacitive isolator, have been widely used in BMS to prevent or avoid possible hazards across different high voltage domains. For instance, several HV transceivers or digital isolators have been reported [1] - [7]. An optical coupler was proposed to isolate and communicate between high voltage and low voltage systems [1], [2]. The disadvantages of optical couplers are high power consumption, poor integration, low speed, and degradation of LED (Light Emitting Diode) life. Digital isolators using magnetic coupling [3], [4] or capacitive coupling [5], [6] methods have also been reported. However, no matter magnetic or capacitive coupling transmissions, they will generate EMI (electromagnetic interference) noise to jam other circuits or be corrupted by external wireless signals to endanger the system reliability. Besides, they usually use a lot of large discrete components, i.e., transformer and capacitor. Therefore, it is not easily integrated in SOC (system on chip) designs for the purpose of miniaturization. A wireless battery monitor was also proposed [7]. However, it is not cost effective to realize a large scale battery system because it needs a lot of wireless transceiver modules.

All of the above solutions need extra packaging cost to pack them into one package, namely SiP (System in Package). They are well known as "multi-die" solutions. A 2-die isolation solution is the most sophisticated method so far, where Tx and Rx are respectively fabricated on 2 individual dies, and the corresponding coils are stacked up to realize a transformer. Notably, long bonding wires are required to couple coils to either Tx or Rx [9].

To reduce the size of BMS as well as power consumption, the best strategy is to reduce the number of discretes. Thus, single die solution has been recognized as one of the ultimate solutions. Thanks to the evolution of HV CMOS technologies, 800 V 0.5 μm BCD process, namely UHV (ultra-high voltage), with high p-n junction isolation has been developed [8]. Particularly, HVJT (high voltage junction termination), is available in the UHV process to carry out coupler and transformers with excellent isolation across different votlage domains. Thus, instead of traditional multi-die solutions using SiP technology, the proposed single-die solution to realize the isolator is demonstrated, where Tx (transmitter) converts the digital signal at Din into pulses. A pair of on-chip coils consisting of the transformer to couple the pulses to Rx (receiver), where the pulses are restored into digital signals at Dout.

II. Single-chip High-voltage Digital TX/RX

Referring to Fig. 1, instead of traditional multi-die solutions using SiP technology, the proposed single-die solution to realize the isolator is demonstrated. TX (transmitter) converts the digital signal at Din_tx_ls into pulses. A pair of on-chip coils consisting of the transformer to couple the pulses to RX (receiver), where the pulses are restored into digital signals at Dout_rx_hs.

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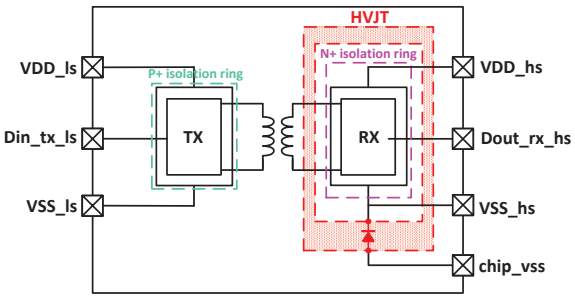

Fig. 1. Single-die TX/RX

A. High-voltge digital transmitter (TX)

Referring to Fig. 2, when a rising edge appears at Din, namely Din_tx_ls in Fig. 1, the gate drives at MP1 and MP2, respectively, are pulled down and up such that the former is turned on and latter off. Meanwhile, S2 is kept closed by a strobe with 2.0 ns width, and S1 is kept closed. MN2 is then turned on for a period of time and then turned off. MN1 is off at the same period of time. In such a scenario, a current path is formed to drive the current flowing through the transformer and back to MN2. V_2 is proportional to the direvative of I_1 based on Eqn. (1). Therefore, as soon as the current path is suddenly turned on, V_2 is boosted drastically. By contrast, when the I_1 drops fast caused by the cuff-off the current path due to the turn-on of MN2, V_2 will drops very fast as well, even to a negative potential. Apparently, it is a scenario vey hostile to determine if there is really a rising edge at Din.

$$V_2 \propto M_{21} \cdot \frac{dI_1}{dt} \tag{1}$$

where M_{21} denotes the mutual inductance of the transformer.

A resolution to avoid the mentioned possible misjudgement of the rising edge is to increase the aspect ratio, namely W/L, of MP3 and MP4, and decrease that of MN3 and MN4 such that MN2 will be turned on fast, but turned off slowly. Consequently, a postive pulse at V_2 will generated provided that a rising edge is present at Din. Notably, the similar design methodology is also applied to the scenario when a falling edge appears at Din. That is, a negative pulse at V_2 will generated provided that a falling edge is present at Din.

B. High-voltage digital receiver (RX)

The schematic of HV digital receiver (RX) is a little bit more complicated than that of TX counterpart, as shown in Fig. 3, where a pre-amplifer and a post-amplifer are needed.

Fig. 3(a) illustrates that a differential pair of signals, $V_{din\_rx\_hx\_p}$ and $V_{din\_rx\_hx\_n}$, generated by the secondary side of the transformer. Notably, the 2.5 V DC is used as the common mode DC voltage. The differential pair is coupled to the gate drives of MN5 and MN6 of the pre-amplifer shown in Fig. 3(b). The pre-amplifer is a postive feedback amplifer consisting of a differential pair (MN5 and MN6), and a cross-coupled load comprising MP5 - MP8. Notably, MP5 - MP8 is

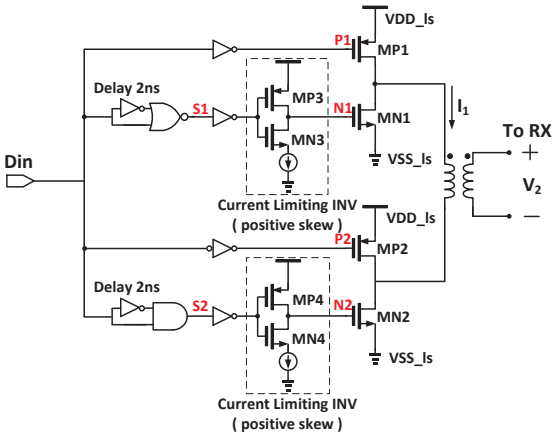

Fig. 2. Schematic of TX

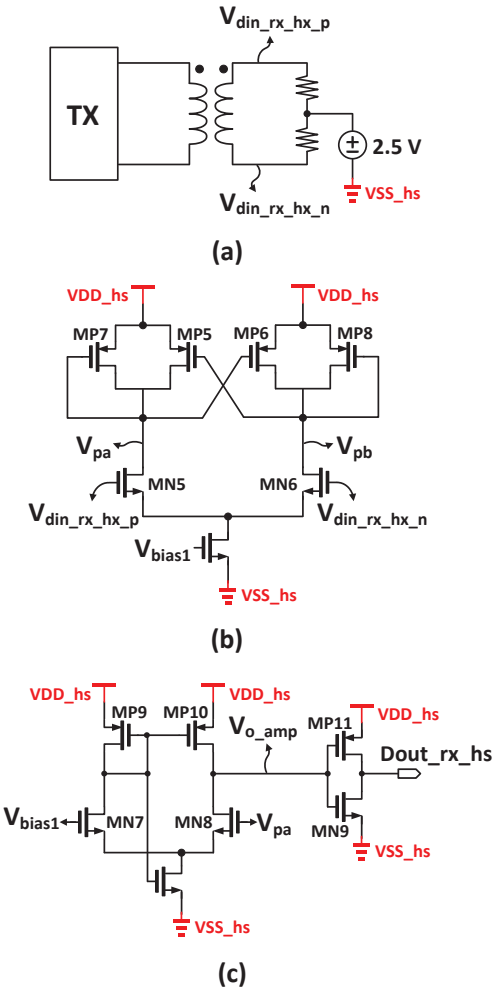

Fig. 3. Schematic of RX

a postive feedback to increase the overall gain, and the positive loop gain can be adjusted by tuning the aspect ratio between W/L of MP5 and MP6 vs. that of MP7 and MP8.

The postive feedback of MP5 - MP8 is explained as follows. Assume the input voltage at MN5 gate is positive, and the complementary one at MN6 gate is negative. Then, I_{ds5} is increased, but I_{ds6} is decreased to result in the drop of MP7 gate drive and the rise of MP8 gate drive. Consequently, I_{ds5} will go up even higher and I_{ds6} will become even smaller at the same time. The positive feeback keeps functioning till the decrease of MN5 gate drive and the increase of MN6 gate drive, respectively, result in a scenario that the increase rate of I_{ds5} and the decrease rate of I_{ds6} are equal. Thus, the pulse width of the received signals at $V_{din\_rx\_hx\_p}$ and $V_{din\_rx\_hx\_n}$, which is around 2 -3 ps, will be enlarged to 3 - 6 ns at the outputs of the pre-amplifer such that the following post-amplifer will be able to recognize that the recevied signals is valid or not.

One of the pre-amplifer's outputs, namely V_{pa} is coupled to the gate drive of MN8 in the post-amplifier, as shown in Fig. 3(c). Meanwhile, the other input the the post-amplifer is gate-biased by V_{bias1}, which is a tunable external bias. Notably, the post-amplifer is composed of a self-biased differential amplifer followed by a logic inverter. The post-amplifer is carry out the following functions.

$$\begin{aligned} V_{pa} &> V_{bias1} \rightarrow V_o = \text{VDD\_hs} \\ V_{pa} &< V_{bias1} \rightarrow V_o = \text{VSS\_hs} \end{aligned}$$

III. Experiment and Measurement

The proposed single-die HV digital transceiver is carried out by TSMC 0.5 μm high voltage based LDMOS 2P3M polycide process. The die photo is shown in Fig. 4, where the active chip area is 2009×1687 μm^2, and package is SB28. Notably, P+ isolation ring and N+ isolation ring must be added to surround TX and RX, respectively, as shown in Fig. 1. Otherwise, any high voltage, e.g. tens of volts, will punch through the devices therein to kill the chip.

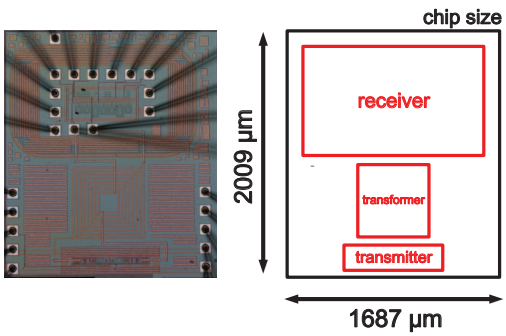

Fig. 4. Diephoto of the proposed design

Referrting to Fig. 5, one power supply is used to provide 0 V (VSS_ls) and 5 V (VDD_ls) in the measurement setup, and another HV power supply is used to provide HV TX/RX two voltage sources : 0 V + △ V (VSS_hs) and 5 V + △ V (VDD_hs).

Fig. 5. Measurement site setup

• △ V = 25 V : The highest data rate is 10 Mbps with voltage swing 1.388 V at Dout_rx_hs, as shown in Fig. 6. Fig. 7 demonstrates the eye diagram therewith, where the eye is 92 ns × 632 mV.

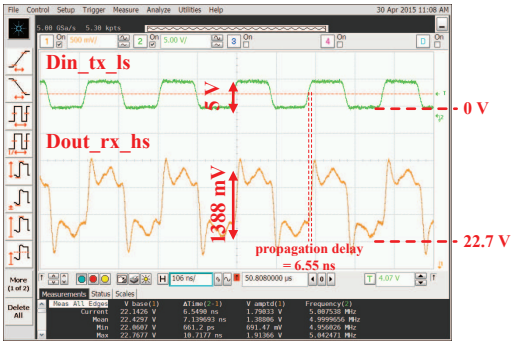

Fig. 6. Waveform of digtial pulse at 10 Mbps, 25 V

• △ V = 50 V : The highest data rate is 10 Mbps with voltage swing 1.175 V at Dout_rx_hs, as shown in Fig. 8. Fig. 9 shows the eye diagram therewith, where the eye is 97 ns × 345 mV.

To the best knowledge that we know, the proposed HV digital transceiver is by far the only single-die solution. Table I summarizes the performance comparison with exsiting solutions. The proposed design is the only single-die design.

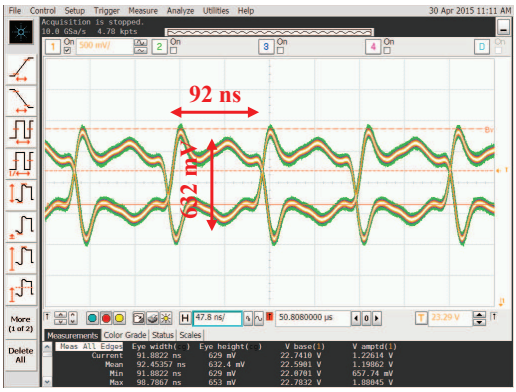

Fig. 7. Eye diagram at 10 Mbps, 25 V

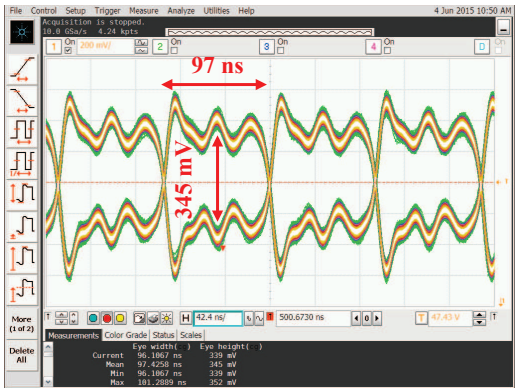

Fig. 9. Eye diagram at 5 Mbps, 50 V

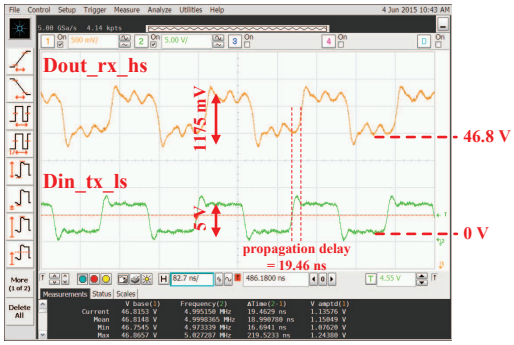

Fig. 8. Waveform of digtial pulse at 5 Mbps, 50 V

And the 10 Mbps data rate is also adequate for car-electronics standards, e.g., CAN and FlexRay.

TABLE I

COMPARISON WITH PRIOR WORKS

	[9]	[3]	this work
Year	2012	2005	2015
Process	5V CMOS	5V CMOS	0.5 μm 800V CMOS
Die#	2	3	1
Transformer#	1	1	1
Transform ϕ	230 μm	500 μm*	600 μm
Max. data rate	250 Mbps	120 Mbps	10 Mbps
Delay	N/A	27 ns	$<$ 19.5 ns
Chip area (μm^2)	0.953	N/A	3.389
Power (mJ/Mbps)	0.032	N/A	0.266
Modulation	pulse polarity	pulse count	pulse polarity

* : estimated from photo

IV. CONCLUSION

This paper presents a single-die HV digital transceiver such that no SiP nor off-chip bonding wires are needed. Measurement based on physical experiments demonstrates that the data rate is 10 Mbps across 50 V voltage domains. It is adequate to be applied to 13-cell battery strings to transmit the information of individual cell, including SOC (state of charge), SOH (state of health), temperature, residue voltage, etc. It is also meet the speed requirement of CAN bus and even FlexRay. By far, the proposed design is the only single-die soltion to our best knowledge.

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