A Capacity Monitoring System with HV Current Sensor and Calibrated Current Estimation Approach

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***Abstract*—This paper presents a battery module capacity monitoring system with a high voltage (HV) current sensor and a calibrated current estimation approach (CCEA) method. Battery modules usually are utilized to generate HV and large currents to drive motors of electric vehicle (EV). The battery modules are controlled and monitored by a system to protect the modules from possible hazards, e.g., battery management systems (BMS). However, since the BMS needs to deal with HV signals, it is very difficult to be implemented using logic integrated circuits (ICs). The proposed design, by contrast, is implemented using a typical 0.25 μm 1P3M 60V BCD process and field programmable gate array (FPGA) to resolve this issue. The sensing current range of the proposed system is 0.44 A $\sim$ 2.2 A, while the voltage is from 36 V to 55 V. The worst-case deviation of the capacity estimation is 8.6 %.**

***Index Terms*—battery management systems, state of charge, state of health, all-digital.**

I. Introduction

Electric vehicle (EV) is a key technology to replace conventional transportation tools [1]-[4]. The energy of the EV is generally from battery modules, which are used to driving motors [1]-[2]. The battery module is composed by many battery cells such as 6-cell, 8-cell, and 13-cell etc. [1]-[4]. Take a series of 13 batteries (battery module) as an example. The charge voltage and discharge cutoff voltage of the Lithium-Ion rechargeable battery are 4.2 V and 2.8 V, respectively, as shown in Table I [5]. Thus, the highest and lowest voltages of the 13-cell battery string become 54.6 V and 36.4 V, respectively. The discharge current and charge current of the Lithium-Ion rechargeable battery is up to 10 A and 2.0 A, respectively. The typical capacity of the battery cell is 2200 (mAh). The discharge and charge currents of the battery module are usually 0.2 C-rate $\sim$ 1 C-rate (that is, 0.2 C-rate and 1 C-rate are 0.44 A and 2.2 A, respectively). Due to the demand of safety and reliability, the battery management systems (BMS) usually uses battery-monitoring integrated circuits (ICs) to monitor temperature, voltage, current, state of charge (SOC), and state of health (SOH), etc. [1]-[2], [6]-[9]. Notably, the input and output of the BMS are always HV and large current.

Referring to [1]-[9], the battery monitoring ICs have been widely used in BMS. The primary function of the BMS is to keep users updated regarding the SOC and SOH of the battery, which indicate whether the battery cells are needed to be replaced or re-charged. The SOC and SOH estimation must be based on the acquired voltage and current data from the battery cells [3]-[4]. However, most of the existing battery monitoring ICs can not simultaneously monitoring large currents and HV signals of the battery cells [5]-[8]. Kim *et al.* proposed a modularized charge equalizer, which uses battery monitoring ICs with a microcontroller to provide information of battery cells for estimation and management [1]. Kadirvel *et al.* proposed a stackable architecture battery monitoring IC, which can monitor 6 cells. If the ICs are stacked, it can monitor a total of 192 cells [2]. Apparently, the stackable architecture needs a large number of battery monitoring ICs to monitor each cells. The on-chip battery current sensors were also proposed [10]. Shalmany *et al.* proposed a micro-power current-sensing system for battery monitoring, where a calibrated shunt resistor is used to sense the current of the battery [10]. However, the micro-power current-sensing system is only operated in low voltage range ($\leq$ 5 V).

TABLE I
CELL SPECIFICATION OF LITHIUM-ION RECHARGEABLE BATTERY (MODEL: IHR18650BN)

MODEL	IHR18650BN
Shape / Can material	Cylindrical / Steel
Typical Capacity (mAh)	2200
Nominal Voltage (V)	3.6
Charge Voltage (V)	4.2 ±0.05
Discharge Cutoff Voltage (V)	2.8
Charge Current (A)	Less than 2.0
Discharging current (A)	Max. 10

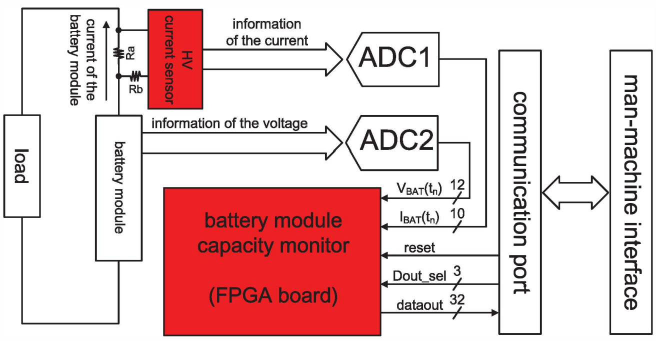

Fig. 1. The block diagram of the battery module management system.

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In this study, we propose a battery module capacity monitoring system with a HV current sensor. Besides, a CCEA method is proposed and realized to carry out the calibration. The sensing current range of the battery module capacity monitoring system is 0.44 A $\sim$ 2.2 A. The voltage range of the battery module capacity monitoring system is 36 V $\sim$ 55 V. The proposed system also estimates the capacity of the battery module with different discharge currents.

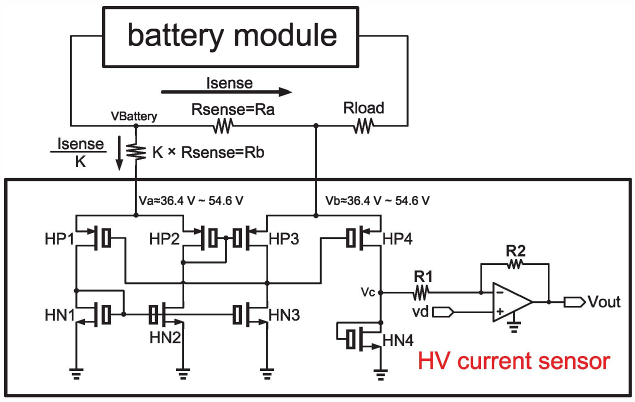

Fig. 2. The block diagram of the proposed HV current sensor.

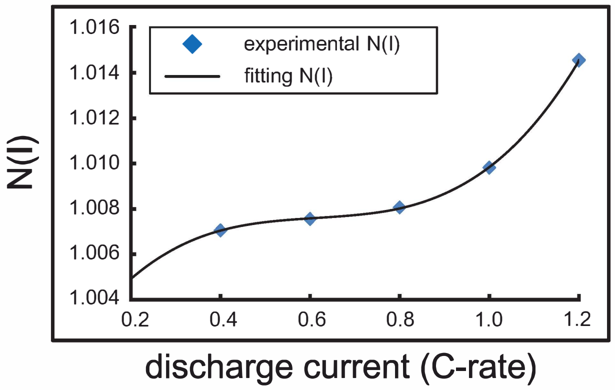

Fig. 3. A fitting curve given different discharging currents.

II. Battery Module Capacity Monitoring System

Fig. 1 shows the block diagram of the proposed battery module capacity monitoring system, comprising 4 major blocks, i.e., a HV current sensor, a battery module capacity monitor, and two analog-to-digital converters (ADCs). The HV current sensor measures the current of the battery module and sends to ADC1. ADC2 is used to monitor the voltage of the battery module. Based on the acquired current and voltage data of the battery module, the battery module capacity monitor estimates the capacity of the battery module. The details of the HV current sensor and the battery module capacity monitor are given in the following text.

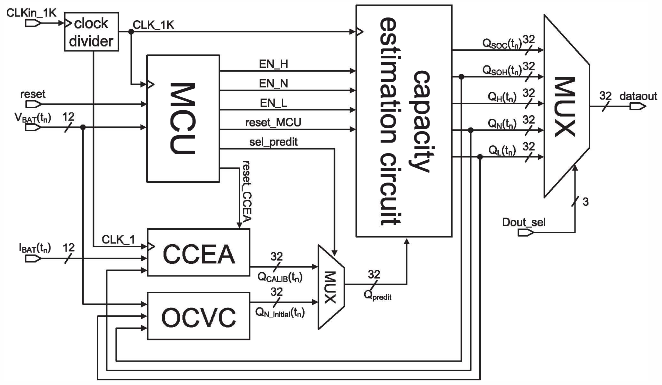

Fig. 4. The block diagram of the proposed battery module capacity monitor.

A. HV Current Sensor

The HV current sensor is composed of 4 HV PMOSs, 4 HV NMOSs, two resistors, and an OPA, as shown in Fig. 2. Rsense is designed as a very small resistor such that it will not affect the load of the BMS. Thus, the current via Rsense will not disturb the function of the HV current sensor. Va and Vb are written as Eqn. (1) and (2), respectively, as follows.

$$\text{Va} = \text{Vbattery} - \frac{\text{Isense}}{\text{K}} \times (\text{K} \times \text{Rsense}) \quad (1)$$

$$\text{Vb} = \text{Vbattery} - \text{Isense} \times \text{Rsense} \quad (2)$$

The resistance of Rsense and K $\times$ Rsense are set to be 0.01 Ω and K $\times$ 0.01 Ω, respectively, where K is selected to be 10^6.

Vc is written as:

$$\text{Vc} = \text{V}_{\text{GS, HN4}} \approx \kappa \times \text{V}_{\text{GS, HP4}} \quad (3)$$

where κ is $\sqrt{\frac{W_{HP4} \times L_{HN4}}{2 \times W_{HN4} \times L_{HP4}}}$, W_{HP4} and L_{HP4} are the width and the length of HP4, respectively, W_{HN4} and L_{HN4} are the width and the length of HN4, respectively. According to Eqn. (1)-(3), Eqn. (4) is re-organized as:

$$\text{Vc} \approx \kappa \times (\text{V}_{\text{G, HP4}} - \text{Vb}) \quad (4)$$

The above equation indicates that Vc varies with Vb, where Vb varies with Isense in Eqn. (1). Thus, the output variation of HV sense stage is indirectly varied by the current in Rsense. Notably, Vc can be tuned to be lower than 5 V by adjusting κ such that the HV hazards on the circuit can be prevented. Besides, R1, R2, and an OPA are used to adjust Vc to meet the input range requirement of ADC1, as shown in Fig. 1 and Fig. 2.

B. Battery Module Capacity Monitor

In this investigation, a battery module composed of 13 cells, which are IHR18650BN, is used as experimental subject. The charging and discharging procedures are repeated with different currents from 0.2 C-rate to 1.0 C-rate. A fitting curve, $N(I)$ vs. C-rate discharging currents, is found by a field solver.

$$N(I) = a \times I^3 + b \times I^2 + c \times I + d \quad (5)$$

where the a, b, c, and d are coefficients to be determined, I is the discharging current. Since the releasing capacity of the battery depends on the discharging current with different C-rate, the capacity of the battery must be calibrated. Another problem demanding calibration is that the capacity of a new battery is unknown if the new battery has not been completely discharged and charged before.

A battery module capacity monitor is proposed to resolve these problems, as shown in Fig. 4. The proposed battery module capacity monitor consisting of 7 major blocks, i.e., a clock divider, a calibrated current estimation approach (CCEA), an open circuit voltage circuit (OCVC), a microcontroller unit (MCU), a capacity estimation circuit, and two multiplexers (MUXs). Based on $V_{BAT}(t_n)$ (present voltage of the battery at time t_n), MCU sends 3 signals, EN_N, EN_H, or EN_L to the charge estimation circuit, where the output signals are tabulated in Table II. Charge estimation circuit estimates $Q_{SOC}(t_n)$, $Q_{SOH}(t_n)$, $Q_H(t_n)$, $Q_N(t_n)$, and $Q_L(t_n)$ based on $Q_{CALIB}(t_n)$, EN_N, EN_L, and EN_H, where $Q_L(t_n)$ is the capacity of the battery when its voltage is lower than 36.4 V, $Q_N(t_n)$ is the capacity at present, $Q_H(t_n)$ is the capacity if its voltage is higher than 54.6 V, $Q_{SOC}(t_n)$ is the normalized residual charge denoting SOC, and $Q_{SOH}(t_n)$ is the normalized residual capacity for SOH. MUX is driven by Dout_sel to select required data of the battery and send to the following communication port as shown in Fig. 1. Besides, the OCVC is used to provide an initial capacity of the battery module.

TABLE II
OUTPUT SELECTION SIGNALS IN DIFFERENT MODES.

mode	reset_MCU	EN_L	EN_N	EN_H
reset mode	1	X	X	X
normal mode	0	0	1	0
over-voltage mode	0	0	1	1
under-voltage mode	0	1	1	0

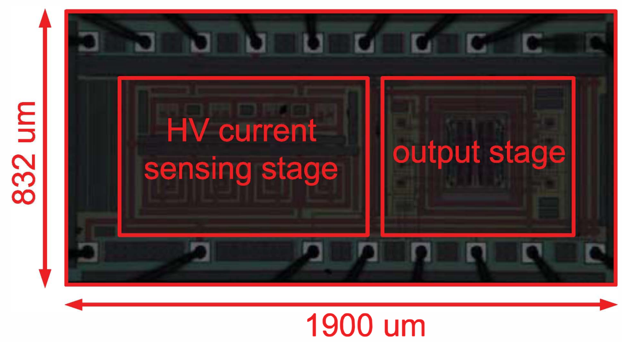

Fig. 5. Die of the proposed HV current sensor.

III. IMPLEMENTATION AND MEASUREMENT

The proposed HV current sensor and the battery module capacity monitor are implemented using a typical 0.25 μm 1P3M 60V BCD process and FPGA, respectively. Fig. 5 shows the die photo of the proposed HV current sensor, where the core area of the proposed design is 1.5808 mm^2. The proposed HV current sensor is measured given the current range from

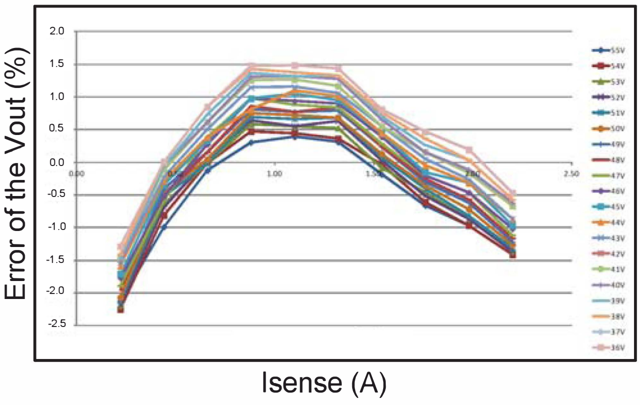

Fig. 6. Error distribution of the proposed HV current sensor.

TABLE III
PERFORMANCE OF THE PROPOSED HV CURRENT SENSOR

	HV current sensor
Process (μm)	0.25
Supply Voltage (V)	5
Sensing Voltage Range (V)	36 $\sim$ 55
Sensing Current Range (A)	0.44 $\sim$ 2.2
Max. Error (%)	-2.5 $\sim$ 1.5
Core Area (mm^2)	1.5808

0.44 A to 2.2 A, where the maximum error is lower than -2.5 %, as shown in Fig. 5. The performance comparison of the proposed design and several recent works is tabulated in Table III. Table IV shows the performance of the proposed battery module capacity monitor, where the number of total logic elements to carry out the proposed design is 909, where the total registers and pins are 206 and 67, respectively.

The proposed battery module capacity monitoring system is also measured, as shown in Fig. 7. The worst-case deviations of the proposed battery module capacity monitoring system is 8.6 %. The performance comparison of the proposed design and several prior works is tabulated in Table V. Notably, this work is the only solution realized on silicon.

IV. CONCLUSION

A battery module capacity monitoring system is proposed in this work. The proposed design is implemented using 0.25 μm 1P3M 60V BCD process and FPGA for functionality verification and performance evaluation. Notably, the proposed design normalizes the capacity of the battery with different discharging currents (0.2 C-rate $\sim$ 1 C-rate). The worst-case deviation of the proposed system is 8.6 %, where the error is mainly caused by the HV current sensor and ADCs. Thus, we can use higher resolution ADCs and a more accurate current sensor to improve the performance of the proposed system.

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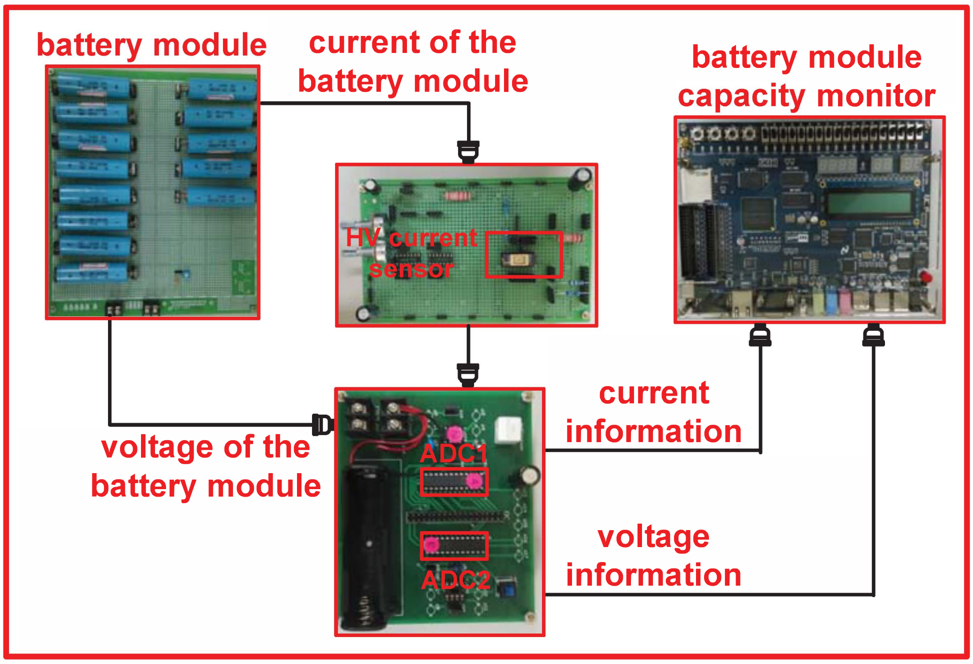

Fig. 7. The measurement set-up of the proposed system.

TABLE V
PERFORMANCE COMPARISON OF THE BATTERY CAPACITY MONITOR

	[8]	[6]	[7]	[9]	This work
Year	2011	2012	2012	2013	2014
Technology	online	online	online	online	0.25 μm 1P3M 60V BCD process / FPGA
Estimation Method	battery model	OVC	OVC	battery model	coulomb counting method / OCV
Calibration Method	AEKF	EKF	EKF	SVM	CCEA
Max. Error (%)	2.54	-5 $\sim$ +5	-5 $\sim$ +5	6	8.6
Clock (KHz)	N/A	N/A	N/A	N/A	1

TABLE IV
PERFORMANCE OF THE PROPOSED BATTERY MODULE CAPACITY MONITOR USING FPGA

	battery module capacity monitor
FPGA MODEL	DE2
FPGA chip	Cyclone II 2C35 FPGA
supply voltage (V)	3.3
total logic elements	909
total registers	206
total pins	67
total memory bits	0
sampling rate of the proposed design (Hz)	1

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