A Wide Range Power Detector for Biosensing Systems Using Frequency Shift Schemes

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ABSTRACT

This paper introduces a high frequency power detector with high conversion gain for frequency-shift applications used in biosensing systems. Proposed design comprises an amplitudeto-voltage convertor (AVC), a peak detector, and a bandgap. To increase the operating frequency range, AVC utilizes the half of an RMS power detector to attain the power measure of an input signal. Since the input power is converted to a DC voltage by AVC, the peak detector will secure the resonant frequency when AVC generates the highest voltage. The proposed power detector circuit is realized on silicon using a 60 V 0.25 μm CMOS technology. Postlayout simulation results show that the proposed circuit is able to detect input frequency from 500 Hz to 20 GHz, and the conversion gain of AVC is 176 mV/dB, while the power

1. INTRODUCTION

Power detectors in previous biosensing systems can be categorized into two types by the input frequency range. The first type employs a peak voltage detector as the power detector [1]. Since the peak detector includes OPA or OTA, it is limited in the low frequency range. The other type is RMS power detector [2]. Although RMS power detectors can operate in high frequency range, but it has the offset error problem and the output voltage resolution is too small to be correctly recognized [3]. To increase the sensitivity, an amplifier following the RMS power detector is usually added to amplify the output voltage. Unfortunately, the offset error will be amplified as well to kill the sensitivity. Therefore, the operating frequency range of the RMS power detector is limited by the offset error.

In this paper, a wide input frequency range power detector is presented. To cancel the offset error and increase the input frequency, we propose to use half of RMS power detector to convert the input amplitude into a DC voltage, namely amplitude-to-voltage convertor (AVC), which enhances the capability to detect high resonant frequency.

2. POWER DETECTOR DESIGN

Fig. 1 shows the architecture of the proposed power detector. $V_{in}(t)$ is a time-domain voltage signal generated by a SAWbased biosensor. The proposed power detector converts the $V_{in}(t)$ into a peak voltage, V_{peak}, which is sent to the following μC-based DSP core to be analyzed and processed. The power detector consists of an AVC, a peak detector, and a bandgap. Notably, this architecture is for the applications which the frequency response of the biosensor is a band-reject filter. If the frequency response is a band-pass filter, the peak detector should be replaced with a valley detector.

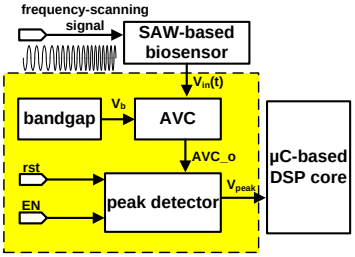

Fig. 1. System view using the proposed power detector

3. CIRCUIT DESCRIPTION AND ANALYSIS

A. Amplitude-to-voltage convertor (AVC)

To cancel the offset error, AVC, shown in Fig. 2, is carried out by only half of the RMS power detector circuit. C201 is utilized to decouple the DC term of Vin(t). Vb is a stable DC bias driving M201 into the saturation region.

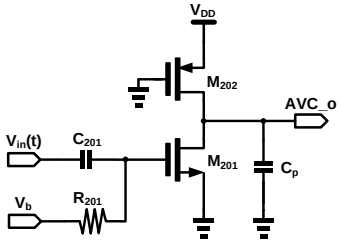

Fig. 2. Schematic of AVC

Fig. 3 shows the worst-case simulation result of AVC output voltage vs. the input amplitude. AVC output voltage increases as the input amplitude decreases. Therefore, when the frequency-scanning signal is equal to the resonant frequency of the sensor, which the frequency response acts like a band-reject filter, the minimum output amplitude will be acquired, and AVC generates the highest output voltage.

B. Peak detector

To reduce the power consumption, the proposed peak detector composed by an OPA which can be turned off when EN is high voltage, as shown in Fig. 4. When the

frequency of the frequency-scanning signal increases over the resonant frequency, the output of the peak detector, V_{peak}, stores the last highest voltage.

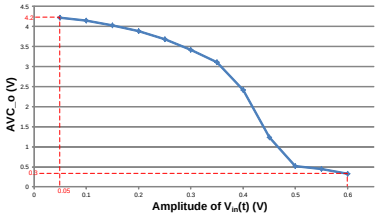

Fig. 3. Simulation result of AVC output voltage vs. the input amplitude

The conversion gain of AVC is 176 mV/dB, and the sensitivity of the peak detector is simulated to be 10 mV. Therefore, the sensitivity of the entire power detector is 0.06 dB. According to the frequency response of the sensors [4], the proposed power detector can detect the resonant frequency with less than 10% error given such a 0.06 dB sensitivity.

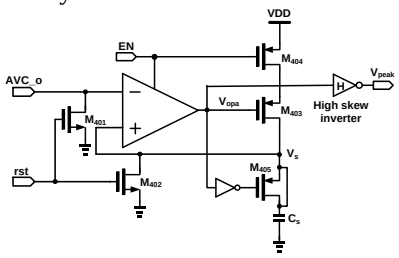

Fig. 4. Schematic of the peak detector

4. IMPLEMENTATION AND SIMULATION

The proposed power detector is realized using TSMC 60V 0.25 µm CMOS technology. Fig. 5 shows the entire circuit layout including I/O PADs. The chip area is 685 × 615 µm². Fig. 6 is the SS corner simulation result (worst case). If the amplitude of the frequency-scanning signal is less than 0.3 V, the proposed power detector will not able to detect the resonant frequency because AV C o exceeds the input range of the peak detector. The comparison with several prior works is tabulated in Table I. The proposed design attains the widest frequency range, 500 Hz to 20 GHz, and the highest conversion gain of AVC, 176 mV/dB.

5. CONCLUSION

This paper presents a wide input frequency range power detector for frequency-shift application. The proposed circuit is able to detect the input frequency from 500 Hz to 20 GHz. The conversion gain of AVC is 176 mV/dB, where the sensitivity of the entire design is 0.06 dB. It is by far the best theoretically in the literature.

6. ACKNOWLEDGEMENT

This investigation is partially supported by Ministry of Science and Technology under grant NSC 102-3113-P-110- 010. Besides, this research is supported by the Southern Taiwan Science Park Administration (STSPA), Taiwan, under contract no. BY-09-04-14-102. The authors would like to express their deepest gratefulness to Chip Implementation Center of National Applied Research Laboratories, Taiwan, for their thoughtful chip fabrication service and EDA tool support.

4. REFERENCES

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TABLE I
COMPARISON WITH PRIOR WORKS

	[2]	[5]	this work
Year	2012	2014	2014
Process	0.18 µm CMOS	0.25 µm CMOS	0.25 µm CMOS
Conversion Gain (mV/dB)	17	176	176
Supply voltage	1.8 V	5 V	5 V
Frequency range	0.5 GHz ~ 5 GHz	500 Hz ~20 GHz	500 Hz ~20 GHz
Power Consumption (mW)	0.9	1.96	1.2

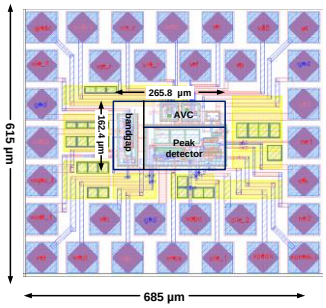

Fig. 5. The layout of the proposed design

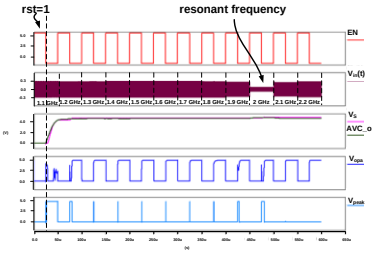

Fig. 6. Worst-case simulation of the proposed power detector