Low Power Cross-Domain High-Voltage Transmitters for Battery Management Systems†

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***Abstract*—This work presents a pair of low power high-voltage (HV) transmitters for battery management systems (BMS). Besides, the HV transmitter is designed using CMOS transistors without any isolator. To realize a solution on silicon, the proposed HV Transmitter shall be fabricated using an advanced HV semiconductor process, which usually is constrained by the voltage drop limitation between gate and source of HV devices. The proposed design is implemented using a typical 0.25 μm 1-poly 3-metal 60 V BCD process. The post-layout simulation results show that the HV transmitters can transmit data with HV dc level (36.4 $\sim$ 54.6 V) and the power consumption is less than 0.342 mW/Mbps.**

***Index Terms*—high voltage, battery management system, high-voltage transmitter**

I. Introduction

High-voltage (HV) battery management system (BMS) is widely needed in many applications, e.g., EV and HEV, where many battery modules are assembled and integrated. One of the popular BMS architectures is the modular formation, i.e., a module monitors several batteries with a daisy-chain interface. A critical issue in the BMS is the data communication carried out by HV transceivers or digital isolators. They are usually implemented by discrete devices, e.g., optocoupler, magnetic isolator, and capacitive isolator. Several HV transceivers or digital isolators have been reported [1]-[5]. An optical coupler is used to isolate and communicate between high voltage and low voltage systems [1]. The disadvantages of optical couplers are high power consumption, poor integration, low speed, and degradation of LED (Light Emit-ting Diode). Digital isolators using magnetic coupling [2] or capacitive coupling [3] methods were proposed. However, no matter magnetic or capacitive coupling transmissions, they will generate EMI (electromagnetic interference) effect to jam other circuits or be corrupted by external RF signals to endanger the reliability. Besides, they usually need a lot of discrete components, i.e., transformer and capacitor. Therefore, it is not easily integrated in SOC (system on chip) designs. A wireless battery monitor was also proposed [4]. However, it is not cost effective to realize a large scale battery system, because it needs a lot of wireless modules. In other words, the cost and area efficiency will be problems. A HV transceiver without discrete devices was also proposed [5]. However, it needs to consume a large power dissipation. To resolve all the above problems, a pair of low power HV transmitters are disclosed in this paper.

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II. Cross-Domain HV Transmitter

A typical architecture of BMS usually consists of HVMUX (HV multiplexer), ADC, Power Management, Main Controller, High to Low Transmitter, and Low to High Transmitter. HVMUX is used to detect the voltage of battery module. ADC and other resistors serve as a current sensor. Main Controller determines the status of battery module, e.g., SOC and SOH, and Power Management generates a stable voltage, namely VDDH, to supply the High to Low Transmitter. Assume the number of batteries is 13 for E-scooters such that the voltage range of battery module is from 36.4 V to 54.6 V. Therefore, the proposed Low to High Transmitter must convert a low-voltage (LV) digital signal (0 $\sim$ 2.5 V) into a digital signal with HV dc level (36.4 $\sim$ 54.6 V). By contrast, the proposed High to Low Transmitter should convert a digital signal with HV dc level into a LV digital signal.

A. Low to High Transmitter

Low to High Transmitter is composed of M201 $\sim$ M210, as shown in Fig. 1. The upper left corner of Fig. 1 shows the symbol description of all transistors, i.e., 2.5 V NMOS, 2.5 V PMOS, HV NMOS, and HV PMOS, where the gate to source voltage of HV PMOS and HV MOS must be limited under a low voltage $\approx$ 5 V. The proposed Low to High Transmitter is basically a differential architecture. M207 $\sim$ M210 are used to limit the currents through M205 and M206. M201 $\sim$ M204 and Mc1 are in charge of keeping the voltage of Vx and Vy between VDDH and VSSH. When TxL is pulled low to VSSL, Vx is pulled high to VDDH and Vy is pulled low to VSSH. Because the Latch locks Vx and Vy, RxH is pulled low to VSSH. By contrast, when TxL is pulled high to VDDL, RxH is pulled high to VDDH. Therefore, the proposed design can convert a digital signal with LV dc level into a HV dc level.

B. High to Low Transmitter

Fig. 2 shows the schematic of High to Low Transmitter, where two bias current sources (M311 $\sim$ M315 and M322 $\sim$ M325) are used to limit the currents of M316 and M317. M318 $\sim$ M321 and Mc2 force the voltage of Va and Vb to stay

TABLE I
COMPARISON BETWEEN THE PROPOSED HV TRANSMITTERS AND PRIOR WORKS

Specifications	This work	[1]	[3]	[2]	[5]
Year	2014	2003	2005	2012	2014
Process (μm)	0.25 μm 60 V BCD	GaAs & BiCMOS	SOI	5V CMOS	0.35 μm BiCMOS
Maximum data rate	4 Mbps	25 Mbps	1 Mbps	250 Mbps	N/A
Number of isolator	0	2 opto-couplers	4 capacitors	2 transformers	0
Propagation delay	8.3 $\sim$ 62.28 ns	$>$ 40 ns	30 $\sim$ 80 ns	5.5 ns	N/A
Power dissipation	0.342 mW/Mbps (20 pF load)	20 $\sim$ 100 mW/Mbps	40 mW/Mbps	5.4 mW/Mbps	$>$ 24 mW
Area	0.2536 mm^2	N/A	N/A	0.12 mm^{2†}	N/A

(†) Not including the area between Tx and transformer

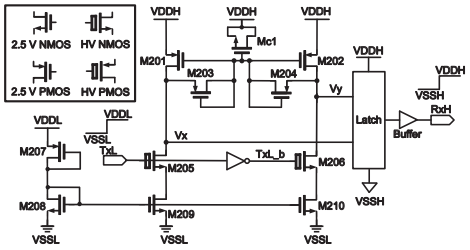

Fig. 1. Schematic of Low to High Transmitter

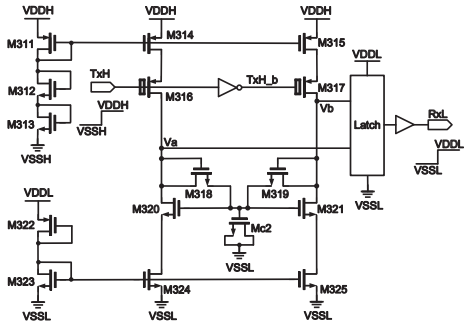

Fig. 2. Schematic of High to Low Transmitter

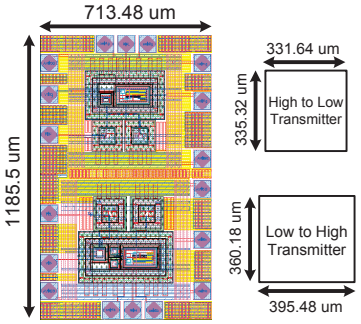

Fig. 3. Layout of the proposed designs.

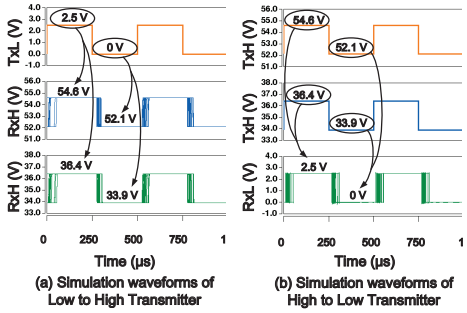

Fig. 4. Simulation results of the proposed design.

between VDDL and VSSL. When TxH is pulled low to VSSH, Va is pulled high to VDDL and Vb is pulled low to VSSL. Because the Latch locks Va and Vb, RxL is pulled low to VSSL. By contrast, when TxH is pulled high to VDDH, RxL is pulled high to VDDL. Therefore, this design will convert a digital signal with HV dc level into a LV dc level.

III. IMPLEMENTATION AND SIMULATION

The proposed designs are implemented using the 0.25μm 1-poly 3-metal 60V BCD process to justify the performance. Fig. 3 shows the layout of the proposed designs. The chip area is 0.71348$\times$1.1855 mm^2, where the active areas are 0.33532$\times$0.33164 mm^2 for High to Low Transmitter and 0.36018$\times$0.39548 mm^2 for Low to High Transmitter, respectively. Fig. 4 shows the simulation results of the proposed design at different VDDH (36.4 V and 54.6 V) and all PVT corners. The maximum propagation delay are 62.28 ns for Low to High Transmitter and 59.32 ns for High to Low Transmitter, respectively. Table I shows the comparison between the proposed HV Transmitter designs and prior works. Our design attains the smallest power dissipation (0.342 mW/Mbps) and it is the only solution without any isolators.

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