A 20 GHz Power Detector with 176 mV/dB Conversion Gain

Chua-Chin Wang†, *Senior Member, IEEE*,
Deng-Shian Wang, Shiou-Ya Chen, and Chia-Ming Chang
Department of Electrical Engineering
National Sun Yat-Sen University
Kaohsiung, Taiwan 80424
Email: ccwang@ee.nsysu.edu.tw

***Abstract*—This paper introduces a high frequency power detector with high conversion gain for frequency-shift applications. The proposed design comprises an amplitude-to-voltage convertor (AVC), a peak detector, and a bandgap. To increase the operating frequency range, AVC utilizes the half of an RMS power detector to attain the power measure of an input signal. Since the input power is converted to a DC voltage by AVC, the peak detector will secure the resonant frequency when AVC generates the highest voltage. The proposed power detector circuit is realized on silicon using a 60 V 0.25 μm CMOS technology. The post-layout simulation result shows that the proposed circuit is able to detect input frequency from 500 Hz to 20 GHz, and the conversion gain of AVC is 176 mV/dB, while the power consumption is 20 mW given a 5 V power supply voltage.**

***Index Terms*—Analog processing circuit, resonant frequency, power detector, peak detector, frequency-shift readout circuit**

I. Introduction

Recently, MEMS sensors with resonant features have been widely used in many applications, e.g., antigen concentration sensing [1], CO_2 concentration sensing [2], and temperature sensing [3], etc., where frequency detectors for sensors are needed. Fig.1 shows a typical frequency detector circuit. The control circuit generators a frequency-scanning signal to the sensor. When the frequency of the frequency-scanning signal equals to the sensor's resonant frequency, the maximum or minimum power will be presented. The power detector generates a digital signal to the control circuit to lock the detected frequency. However, different types of sensors are featured with different frequency ranges. For example, the FPW (flexural plate wave) devices able to estimate IgE (immunoglobulin E) antigen concentration are found to work in the range from 2 MHz to 10 MHz [1]. The SAW (surface acoustic resonator) able to sense the CO_2 concentration must be operated around 545 MHz [2]. The FBAR (film bulk acoustic resonator) for the temperature sensing works around 2.19 GHz [3]. Therefore, to accommodate the operating frequency ranges of various sensors, a wide input range power detector is needed.

The power detectors in previous works can be categorized into two types by the input frequency range. The first type employs a peak voltage detector to be the power detector [4]. Since the peak detector includes OPA or OTA, it is limited in the low frequency range. The other type is RMS power detector, as shown in Fig.2 [5]. Although RMS power detectors can operate in high frequency range, but it has the offset error problem and the output voltage resolution, V_{diff}, is too small

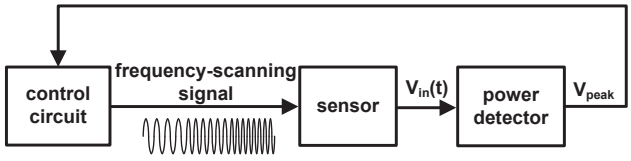

Fig. 1. Architecture of a typical frequency-shift detection circuit

[6]. In order to increase the output difference, an amplifier following the RMS power detector is usually added to amplify the output voltage. Unfortunately, the offset error will be amplified as well. Therefore, the operating frequency range of the RMS power detector is limited by the offset error.

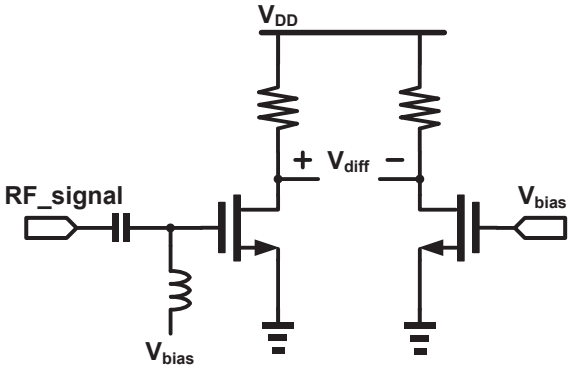

Fig. 2. Schematic of the RMS power detector [5]

In this paper, a wide input frequency range power detector has been presented. To cancel the offset error and increase the input frequency, we propose to use half of RMS power detector to convert the input amplitude into a DC voltage, namely amplitude-to-voltage convertor (AVC). After AVC, the peak detector is available to detect the resonant frequency.

II. Power Detector Design

Fig. 3 shows the architecture of the proposed power detector. It consists of an AVC, a peak detector, and a bandgap. Notably, this architecture is for the applications which the frequency response of the sensor is a band-reject filter. If the frequency

978-1-4799-5230-4/14/$31.00 ©2014 IEEE

response is a band-pass filter, the peak detector should be replaced with a valley detector. In the rest of this paper, AVC and the peak detector will be disclosed in detail and the post-layout simulation results of the entire power detector are shown to justify the functionality. Since the bandgap is carried out by conventional design methodologies, there is no need to rephrase hereby.

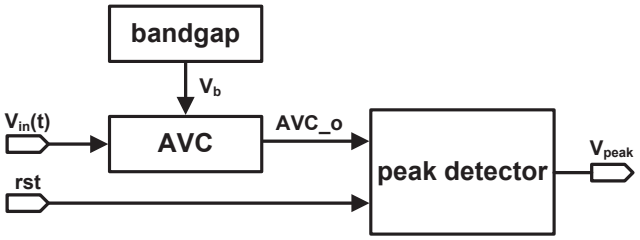

Fig. 3. Architecture of the proposed power detector

III. Circuit Description and Analysis

A. Amplitude-to-voltage convertor (AVC)

To cancel the offset error, AVC, shown in Fig. 4, is carried out by only half of the RMS power detector circuit. C_{401} is utilized to decouple the DC term of $V_{in}(t)$, where $V_{in}(t)$ is the output signal from the sensor. V_b is a stable DC bias driving M_{401} into the saturation region. Thus, the drain current of M_{401} can be expressed as follow.

$$i_{M_{401}}(t) = \frac{1}{2} \cdot \beta_n \cdot (V_{in}(t) + V_b - V_{TN})^2 \quad (1)$$

where $\beta_n = \mu_n C_{ox} (W_{401}/L_{401})$ is the MOSFET transconductance parameter, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, V_{TN} is the NMOS threshold voltage, W_{401} and L_{401} are the channel width and length of M_{401}, respectively. M_{402} is biased in the triode region to act as a resistor. The resistance can be written as follows.

$$r_{M_{402}} = 1/\beta_p \cdot (V_{DD} - |V_{TP}|) \quad (2)$$

where $\beta_p = \mu_p C_{ox} (W_{402}/L_{402})$, μ_p is the hole mobility, V_{TP} is the PMOS threshold voltage. W_{402} and L_{402} are the channel width and length of M_{402}, respectively. C_p is a low-pass filter to filter out the AC component of AVC_o. When the current $i_{M_{401}}(t)$ flowing through the resistor $r_{M_{402}}$ and $V_{in}(t)$ is substituted with $V_a \cdot \cos(2\pi ft + \theta)$, the DC term of the output voltage is attained as follows.

$$AVC\_o = V_{DD} - \frac{1}{2} \cdot \beta_n \cdot r_{M_{402}} \cdot \left[V_a^2 + (V_b - V_{TN})^2\right] \quad (3)$$

Fig. 5 shows the simulation result of AVC output voltage vs. the input amplitude, while Fig. 6 is that of AVC output vs. the input frequency. These two figures demonstrate that the output voltage is irrelevant with the input frequency. However, AVC output voltage increases as the input amplitude decreases. Therefore, when the frequency-scanning signal is equal to the resonant frequency of the sensor, which the frequency response acts like a band-reject filter, the minimum output amplitude will be presented, and AVC generates the highest output voltage.

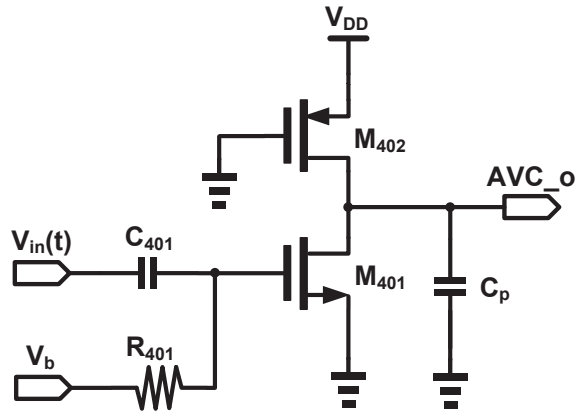

Fig. 4. Schematic of AVC

The conversion gain of AVC, CG_{AVC}, can be derived as follows.

$$CG_{AVC} = \frac{AVC\_o_{max} - AVC\_o_{min}}{20 \cdot \log(V_{a_{max}}/V_{a_{min}})} \quad (4)$$

where the AVC_o_{max}, AVC_o_{min}, $V_{a_{max}}$, and $V_{a_{min}}$ are the maximum and minimum output voltage and the maximum and minimum input amplitude of AVC, respectively. Besides, if AVC is able to detect the power attenuation of the sensor between -5 dB to -25 dB, the entire power detector can find the resonant frequency [7]-[9]. For instance, if the amplitude of the frequency-scanning signal is 1 V, the minimum input amplitude of AVC is 50 mV. Moreover, considering the the input range of the peak detector (use a OPA with p-type input stage) in our design, AVC_o is limited less than 4.5 V, as shown in Fig. 5. Therefore, since the input amplitude range of AVC is from 50 mV to 1 V and the output voltage is from 0 V to 4.5 V, the theoretical conversion gain is 180 mV/dB. However, M_{401} may be biased in the triode region when the input amplitude is too high so that the maximum output voltage will be less than 1 V and the minimum input amplitude will be higher than 0 V. Therefore, the conversion gain of the proposed AVC is 176 mV/dB by the post-layout simulations, as shown in Fig. 5.

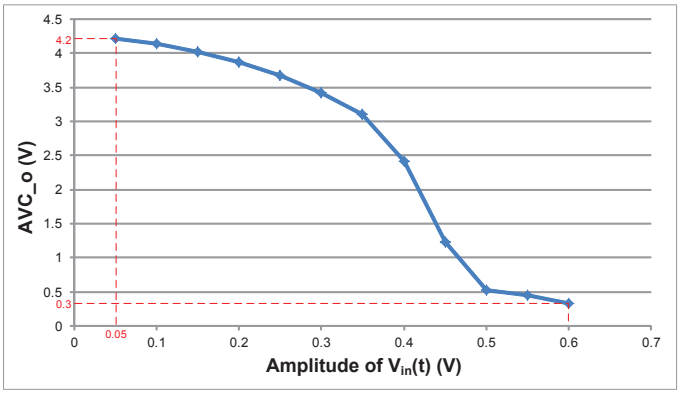

Fig. 5. Simulation result of AVC output voltage vs. the input amplitude

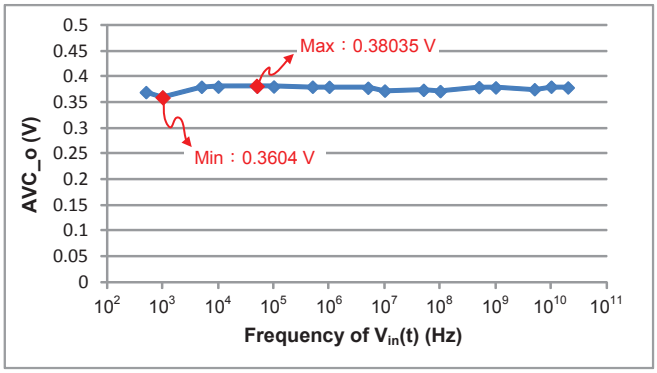

Fig. 6. Simulation result of AVC output voltage vs. the input frequency

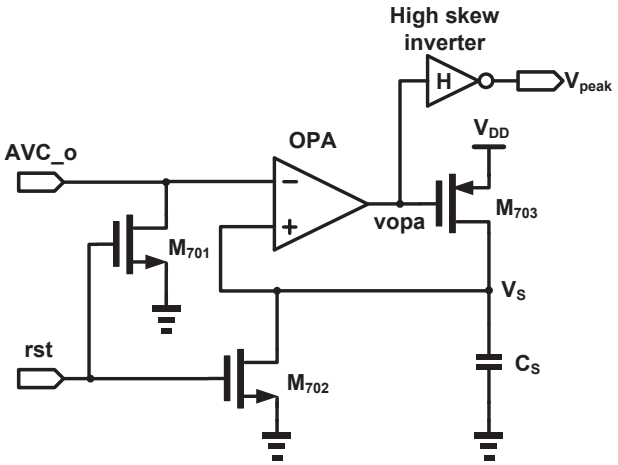

Fig. 7. Schematic of the peak detector

B. Peak detector

As soon as AVC converts the output power of the sensor into a DC voltage, the following peak detector senses the resonant frequency by monitoring the variation of the DC voltage. Fig. 7 shows the schematic of the proposed peak detector. The function of the peak detector is explained as follows.

step 1: Before the frequency-scanning begins, rst is pulled high to reset the power detector such that M_{701} and M_{702} are turned on to discharge AVC_o and V_s.

step 2: After rst is pulled low and the frequency-scanning is started, if the input voltage, AVC_o, is higher than V_s, the OPA discharges vopa to low to turn on M_{703} such that C_s will be charged.

step 3: As soon as $V_s \geq AVC\_o$, the OPA charges vopa to high and then turns off M_{703} to stop charging C_s.

In short, when the frequency of the frequency-scanning signal increases over the resonant frequency, the output of the peak detector, V_{peak}, stores the last high voltage. Besides, a high skew invertor is used to ensure the output V_{peak} is a digital signal where the switching voltage of the high skew invertor is tuned to be 4.09 V to ensure the functionality.

In the proposed power detector, the conversion gain of AVC is 176 mV/dB, and the sensitivity of the peak detector is simulated to be 10 mV. Therefore, the sensitivity of the entire power detector is 0.06 dB. According to the frequency response of the sensors [7]-[9], the proposed power detector can detect the resonant frequency with less than 10% error given such a 0.06 dB sensitivity.

IV. Implementation and Simulation

The proposed power detector is realized on silicon using TSMC 60V 0.25 μm CMOS technology. Fig. 8 shows the entire circuit layout including I/O PADs. The chip area is 435×435 μm^2, and the core area is 145.8×80.4 μm^2. Fig. 9 illustrates the setup of the post-layout simulation where a butterworth filter replaces an FBAR sensor [10]-[11]. The reason why the sensor is replaced by a butterworth filter is that the frequency response of the FBAR sensor is a band-reject filter, which can be approximated with an RLC-based filter. The equivalent circuit and the frequency response of the filter are shown in Fig. 10, where the resonant frequency is 2 GHz. The simulation result is shown in Fig. 11. The amplitude of the frequency-scanning signal is 0.3 mV. When the frequency of frequency-scanning signal is higher than the resonant frequency, the amplitude of $V_{in}(t)$, the output of the butterworth filter, starts to increase. Then, the output of AVC, AVC_o, decreases as $V_{in}(t)$ amplitude increases. When AVC_o does not increase any more, V_{peak} is kept at the same voltage level. Therefore, we record the resonant frequency when the last time the V_{peak} is pulled low. Notably, Fig. 11 is the SS corner simulation result (worst case), where the voltage of AVC_o is close to 4.5 V. If the amplitude of the frequency-scanning signal is less than 0.3 V, the proposed power detector will not able to detect the resonant frequency because AVC_o exceeds the input range of the peak detector.

The comparison with several prior works is tabulated in Table I. The proposed design attains the widest frequency range, 500 Hz to 20 GHz, and the highest conversion gain of AVC, 176 mV/dB.

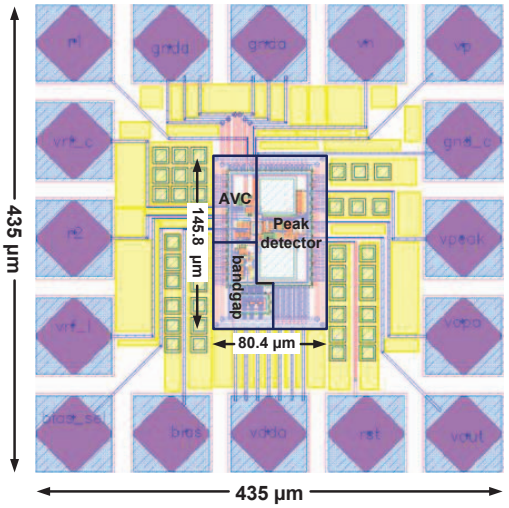

Fig. 8. The layout of the proposed design

TABLE I
COMPARISON WITH PRIOR WORKS

	[6]	[12]	[13]	[5]	this work
Year	2008	2008	2009	2012	2013
Process	0.13 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.25 μm CMOS
Conversion Gain (mV/dB)	6	50	6	17	176
Supply voltage	1.2 V	3.3 V	3.3 V	1.8 V	5 V
Frequency range	0.125 GHz ~8.5 GHz	0.9 GHz ~2.4 GHz	3.1 GHz ~10.6 GHz	0.5 GHz ~5 GHz	500 Hz ~20 GHz
Power Consumption (mW)	0.18 (RMS power detector)	N/A	N/A	0.9 (RMS power detector)	1.96 (power detector)
Core area (μm$\times\mu$m)	12600	31000	36000	7800	290

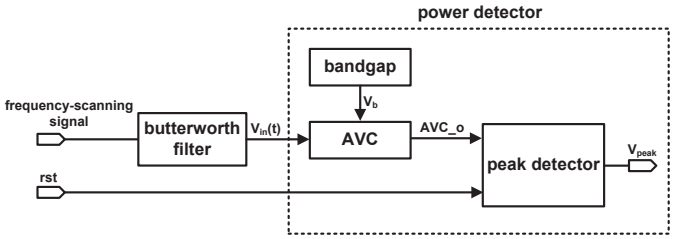

Fig. 9. Post-layout simulation setup

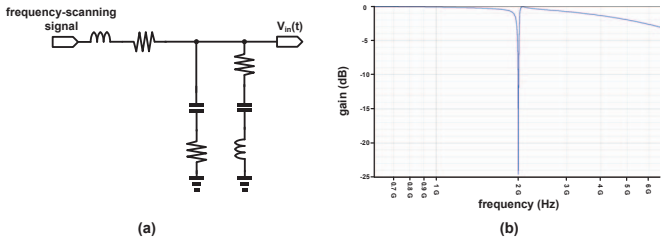

Fig. 10. (a) Equivalent circuit; (b) frequency response of the butterworth filter

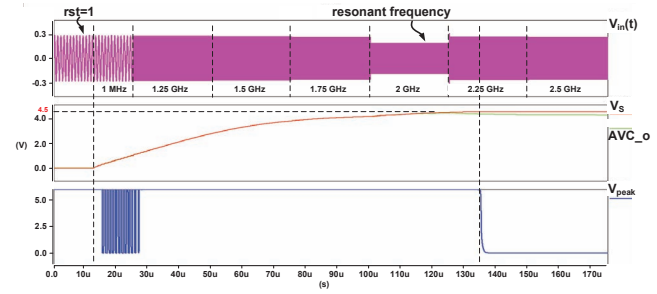

Fig. 11. Worst case simulation of the proposed power detector

V. CONCLUSION

This paper presents a wide input frequency range power detector for frequency-shift application. The proposed circuit is able to detect the input frequency from 500 Hz to 20 GHz. The conversion gain of AVC is 176 mV/dB, where the sensitivity of the entire design is 0.06 dB. It is by far the best theoretically in the literature.

ACKNOWLEDGEMENT

This investigation is partially supported by Ministry of Science and Technology under grant NSC 102-3113-P-110-010. Besides, this research is supported by the Southern Taiwan Science Park Administration (STSPA), Taiwan, under contract no. BY-09-04-14-102. The authors would like to express their deepest gratefulness to Chip Implementation Center of National Applied Research Laboratories, Taiwan, for their thoughtful chip fabrication service and EDA tool support.

REFERENCES

[1] C.-H. Hsu, Y.-R. Lin, Y.-D. Tsai, Y.-C. Chen, and C.-C. Wang, "A frequency-shift readout system for FPW allergy biosensor," *IEEE Inter. Conf. on IC Design & Technology (ICICDT),* pp. 1-4, May 2011.

[2] S. Fanget, H. Grange, F. Palancade, G. Ganuchaud, M. Matheron, S. Charlot, T. Bordy, T. Hoang, P. Rey, D. Mercier, P. Brunet-Manquat, and P. Robert, "CO2 measurement using an AlN/SI SAW sensor," *IEEE Inter. Conf. on Solid-State Sensors, Actuators and Microsystems,* pp. 1136-1139, Jun. 2011.

[3] Z. Wang, X. Qiu, J. Oiler, J. Zhu, and R. Hu, "Film bulk acoustic-wave resonator (FBAR) based infrared sensor," *IEEE Inter. Conf. on Nano/Micro Engineered and Molecular Systems (NEMS),* pp. 824-827, Jan. 2010.

[4] B. Rumberg and D. W. Graham, "A low-power magnitude detector for analysis of transient-rich signals," *IEEE Journal of Solid-State Circuits,* vol. 47, no. 3, pp. 676-685, Mar. 2012.

[5] S. Sakphrom and A. Tranachayanont, "A low-power CMOS RF power detector," *IEEE Inter. Conf. on Electronics, Circuits and Systems (ICECS),* pp. 177-180, Dec. 2012.

[6] Y. Zhou and Y.-W Chia, "A low-power ultra-wideband CMOS true RMS power detector," *IEEE Tran. on Microwave Theory and Techniques,* vol. 56, no. 5, pp. 1052-1058, May 2008.

[7] T. Yokoyama, T. Nishihara, S. Taniguchi, M. Iwaki, Y. Satoh, M. Ueda, and T. Miyashita, "New electrode material for low-loss and high-Q FBAR filters," *IEEE Inter. on Ultrasonics Symposium,* vol. 1, pp. 429-432, Aug. 2004.

[8] S. H. Yoon and D.-J. Kim, "Fabrication and characterization of ZnO films for biological sensor application of FPW device," *IEEE Inter. Symposium on Applications of Ferroelectrics,* pp. 1-4, Aug. 2006.

[9] S. Fujii and C. Jian, "High-frequency SAW filters based on diamond films," *IEEE Tran. on Ultrasonics, Ferroelectrics and Frequency Control,* vol. 59, no. 12, pp. 2758-2764, Dec. 2012.

[10] R.-C. Lin, Y.-C. Chen, W.-T. Chang, C.-C. Cheng, and K.-S. Kao, "Highly sensitive mass sensor using film bulk acoustic resonator," *Sens. Actuators A-Phys.,* vol. 147, no. 2, pp. 425-429, Oct. 2008.

[11] Y. Aota, U. Tohoku, S. Tanifuji, H. Oguma, and S. Kameda, "P1H-4 FBAR characteristics with alN film using MOCVD method and Ru/Ta electrode," *IEEE Ultrasonics Symposium,* pp. 1425-1428, Oct. 2007.

[12] A. Valdes-Garcia, R. Venkatasubramanian, J. Silva-Martinez, and E. Sanchez-Sinencio, "A broadband CMOS amplitude detector for on-chip RF measurements," *IEEE Tran. on Instrumentation and Measurement,* vol. 57, no. 7, pp. 1470-1477, Jul. 2008.

[13] K. A. Townsend and J. W. Haslett, "A wideband power detection system optimized for the UWB spectrum," *IEEE Journal of Solid-State Circuits,* vol. 44, no. 2, pp. 371-381, Feb. 2009.