An All-digital Battery Capacity Monitor Using Calibrated Current Estimation Approach

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***Abstract*—This paper presents an all-digital battery capacity monitor using calibrated current estimation approach (CCEA). The circuit implementation for state of charge (SOC) and state of health (SOH) estimation methods is also revealed as well. The capacity of the battery is highly correlated with different discharging currents. Due to the variation of the capacity, the accuracy of the SOC and SOH estimated methods will be affected with different discharging currents. The CCEA is used to calibrate the capacity of the battery with different C-rate discharging currents such that the capacity of the battery will be normalized. The proposed design is implemented using a typical 0.25 μm 1P3M 60V BCD process. The core area of the proposed design is 610 $\times$ 610 μm^2. In the range from 0.3 C-rate to 1.0 C-rate, the maximum error of the proposed design is -0.56 % $\sim$ 0.07 %. Particularly, the maximum improvement of the proposed design is 530 %.**

***Index Terms*—battery management systems, state of charge, state of health, all-digital.**

I. Introduction

Nowadays, batteries are the most echo-friendly energy source for transportation vehicles [1]. For instance, battery cells provide large current and high voltage to drive motors, LEDs, etc. Nevertheless, a battery monitoring integrated circuit (IC) is usually needed to monitor state of charge (SOC), state of health (SOH), voltage, current, and temperature of each battery module or cell string for the sake of safely, where the most important information is recognized as SOC and SOH, which tell the users the current battery condition, as shown in Fig. 1 [1]. However, many SOC and SOH estimation methods heavily relied on complex battery current characteristic equations or complicated battery models [2]-[8]. Thus, the complex estimation methods are always implemented online, which means the complex SOC and SOH estimation algorithms can not be implemented on silicon [2]-[8], to provide real-time information.

Referring to [2], [3], the SOC and SOH are defined as the residual capacity and present capacity of a battery, respectively. However, the capacity of the battery is varied with different discharging currents even though the aging issue is not considered [4]. Many extended Kalman filter (EKF) reports were widely used to calibrate the SOC and SOH estimation methods [2], [3], [5]-[7]. Kim *et al.* proposed an SOC estimation method based on the open circuit voltage (OVC) battery model [5].

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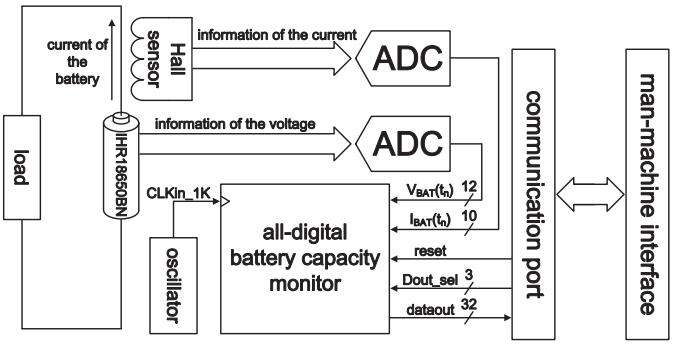

Fig. 1. The block diagram of the battery management systems.

TABLE I
Cell specification of Lithium-Ion rechargeable battery
(MODEL : IHR18650BN)

MODEL	IHR18650BN
Shape / Can material	Cylindrical / Steel
Typical Capacity (mAh)	2200
Nominal Voltage (V)	3.6
Charge Voltage (V)	4.2 $\pm$0.05
Discharge Cutoff Voltage (V)	2.8
Charge Current (A)	Less than 2.0
Discharging current (A)	Max. 10

This battery model is based on EKF to calibrate equivalent circuit models and variation parameters. He *et al.* proposed an adaptive EKF (AEKF) algorithm to calibrate nonlinearity of the EKF [7]. The AEKF was meant to reduce uncertainty of the battery model and environmental noise. However, since the EKF-based estimation methods are very complex algorithms, the cost of realization is very high [5]-[7]. Anton *et al.* proposed a battery model to estimate SOC, where the model parameters comprise battery charging testing cycles, discharging testing cycles, battery current, battery voltage, and battery temperature [8]. However, if these SOC estimation methods are implemented on silicon, large area as well as high cost are the price to pay [2]-[8]. In this study, we propose an all-digital battery capacity monitor on silicon using calibrated current estimation approach (CCEA). The CCEA carries out the calibration based on discharging the battery with different currents.

II. Theory of CCEA

The SOC and SOH estimation methods have been reported as follows [2]-[3]:

$$SOC(t) = \frac{Q(t)_{Residual\ Charge}}{Q_{Typical\ Capacity}} \quad (1)$$

$$SOH(t) = \frac{Q(t)_{Residual\ Capacity}}{Q_{Typical\ Capacity}} \quad (2)$$

where the $Q_{Typical\ Capacity}$ is the typical capacity of the battery , $Q(t)_{Residual\ Charge}$ is the residual charge of the battery, and $Q(t)_{Residual\ Capacity}$ is the residual capacity of the battery. To demonstrate the proposed CCEA, we need to use a battery as the illustrative example. Since the battery cell (IHR18650BN) has been announced as the standard cell for EVs [9], we consider it is a very good instance. The cell specification of the lithium-ion rechargeable battery is shown in Table I. Fig. 2 shows the characteristic curves of the battery using 1 C-rate discharging current. The charge voltage and discharge cutoff voltage of the battery are 4.2 V and 2.8 V, respectively. However, the releasing capacity ($Q_{4.2}$ - $Q_{2.8}$) of the battery is lower than its $Q_{Typical\ Capacity}$ [4], where $Q_{4.2}$ and $Q_{2.8}$ denote residual capacity at 4.2 V and 2.8 V, respectively. Since the releasing capacity of the battery depends on the discharging current with different C-rate, the capacity of the battery must be calibrated. Fig. 3 shows the fitting curve N(C-rate) vs. C-rate discharging currents. The fitting curve is found by a field solver.

$$N(\text{C-rate}) = 0.1477 \times (\text{C-rate})^3 - 0.3806 \times (\text{C-rate})^2$$

$$+0.3369 \times (\text{C-rate}) + 0.9275 \quad (3)$$

According to Eqn. (3), the proposed design can be applied in a wide discharging range (0.3 C-rate $\sim$ 1.0 C-rate).

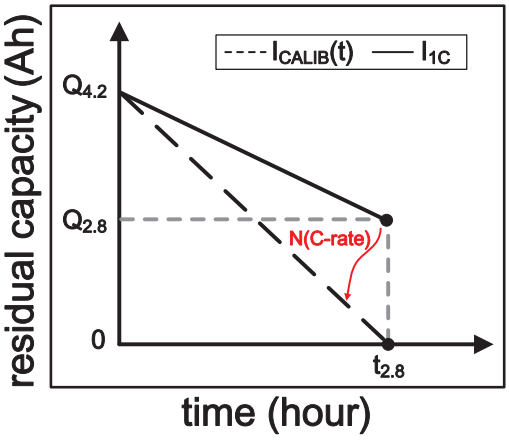

Fig. 2. The discharging curve of the battery with 1 C-rate discharging current.

III. All-digital Battery Capacity Monitor

Fig. 4 shows the block diagram of the proposed all-digital battery capacity monitor comprising 5 major blocks, i.e., a clock divider, a CCEA, a microcontroller unit (MCU), a charge

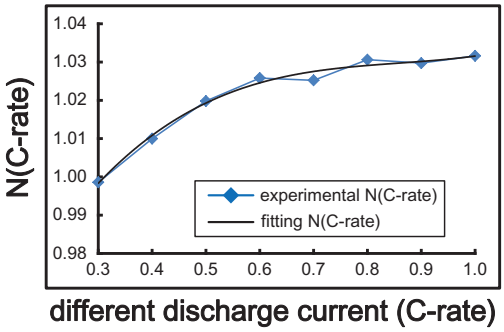

Fig. 3. The fitting curve vs. different discharging currents.

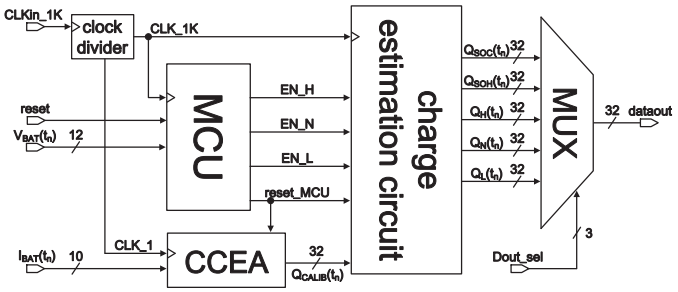

Fig. 4. The block diagram of the proposed all-digital battery capacity monitor.

estimation circuit, and a multiplexer (MUX). The reset is used to drive the MCU. The reset_MCU drives the CCEA and charge estimation circuit, the reset_MCU is a asynchronous reset signal. The clock divider provides clocks for MCU, charge estimation circuit, and CCEA, respectively. CCEA sends the calibrated capacity, $Q_{CALIB}(t_n)$, to charge estimation circuit. According to $V_{BAT}(t_n)$ (present voltage of the battery at time t_n), MCU sends 3 signals, EN_N, EN_H, or EN_L to charge estimation circuit. Charge estimation circuit estimates $Q_{SOC}(t_n)$, $Q_{SOH}(t_n)$, $Q_H(t_n)$, $Q_N(t_n)$, and $Q_L(t_n)$ based on $Q_{CALIB}(t_n)$, EN_N, EN_L, and EN_H, where $Q_L(t_n)$ is capacity of the battery when its voltage is lower than 2.8 V, $Q_N(t_n)$ is capacity of the battery at present time, $Q_H(t_n)$ is capacity of the battery if its voltage is higher than 4.2 V, $Q_{SOC}(t_n)$ is the normalized residual charge for SOC, and $Q_{SOH}(t_n)$ is the normalized residual capacity for SOH. MUX is driven by Dout_sel to select required data of the battery and send to the following communication port as shown in Fig. 1. The details of all the function blocks are given in the following text.

A. CCEA

Fig. 5 shows the schematic of CCEA composed of a calibrated current estimation circuit (CCEC) and a coulomb counting circuit. CCEC provides the calibrated current ($I_{CALIB}(t_n)$) of the battery for coulomb counting circuit. Since the coulomb counting circuit is used to estimate capacity, $Q_{CALIB}(t_n)$, of the battery, CCEA is able to estimate the calibrated capacity of the battery. The operation of the CCEA function is outlined as follows.

1) If the reset_MCU is logic "0", the current decoder of CCEC sends current, $I_{BATCD}(t)$, of the battery to the multiplier in CCEC. All the registers in CCEA are reset, if the reset_MCU is pulled high.
2) The fitting curve table stores the coefficients of the fitting curve, N(C-rate), in Eqn. (3), which will be delivered to the multiplier of the CCEC if selected by the 5 MSB bits of $I_{BATCD}(t_n)$. Thus, $I_{CALIB}(t_n)$ is written as : $I_{CALIB}(t_n) = N(\text{C-rate}) \times I_{BATCD}(t_n)$.
3) The coulomb counting circuit is an accumulator, which estimates the capacity, $Q_{CALIB}(t_n)$, of the battery, which is $Q_{CALIB}(t_n) = Q_{CALIB}(t_{n-1}) + I_{CALIB}(t_{n-1}) \times \triangle t$, where $\triangle t$ is the sampling period (presumably 1 second) of the CCEA.

In short, the capacity of the battery is calibrated based on the discharging current.

B. MCU & charge estimation circuit

Referring to Fig. 4, reset_MCU, EN_N, EN_H, and EN_L are control signals to drive charge estimation circuit. The operation charge estimation circuit function is based on these control signals as shown in Table II. According to $V_{BAT}(t_n)$ and reset, MCU might enter one of four modes : reset mode, normal mode, over-voltage mode, and under-voltage mode. These modes are determined by those control signals (EN_N, EN_H, and EN_L) from MCU as shown in Fig. 6. Then, $Q_{CALIB}(t_n)$ will be written into the $Q_L(t_n)$, $Q_N(t_n)$, and $Q_H(t_n)$, respectively. In the reset mode, all the registers are reset. The normal mode, over-voltage mode, and under-voltage mode denotes the status of the battery in the range of 2.8 V (discharge cutoff voltage) $\sim$ 4.2 V (charge voltage), higher than 4.2 V, and lower than 2.8 V, respectively. The operation of the charge estimation circuit function is outlined follows.

- If the reset_MCU is pulled low, $Q_{CALIB}(t_n)$ is sent to charge estimation circuit. All the registers of the charge estimation circuit are reset, as soon as the reset_MCU is pulled high.
- In the under-voltage mode (EN_N and EN_L are both high, and EN_H is low), $Q_{CALIB}(t_n)$ is written into $Q_N(t_n)$ and $Q_L(t_n)$.
- In the over-voltage mode (EN_N and EN_H are both high, and EN_L is low), $Q_{CALIB}(t_n)$ will be written into $Q_N(t_n)$ and $Q_H(t_n)$. Then, $Q_{SOH}(t_n)$ is estimated as : $Q_{SOH}(t_n) = Q_H(t_n) - Q_L(t_n)$.
- In the normal mode (EN_N is pulled high, and the rest two signals are low), $Q_{CALIB}(t_n)$ is written into $Q_N(t_n)$. Then, $Q_{SOC}(t_n)$ is calculated as : $Q_{SOC}(t_n) = Q_H(t_n) - Q_L(t_n)$.

TABLE II
TRUE TABLE OF THE MCU WITH THE VOLTAGE STATUSES OF THE BATTERY.

mode	reset_MCU	EN_L	EN_N	EN_H
reset mode	1	X	X	X
normal mode	0	0	1	0
over-voltage mode	0	0	1	1
under-voltage mode	0	1	1	0

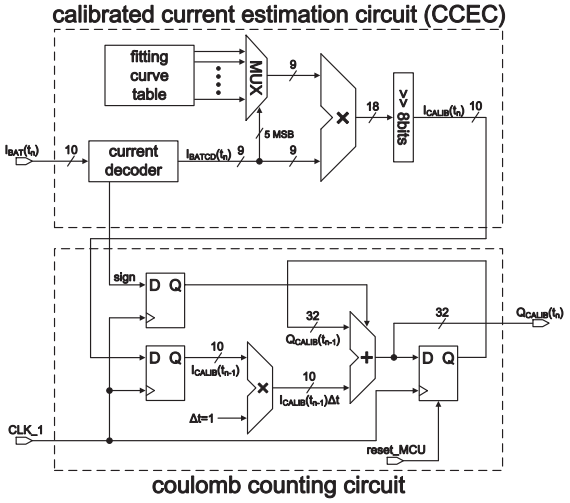

Fig. 5. Schematic of CCEA.

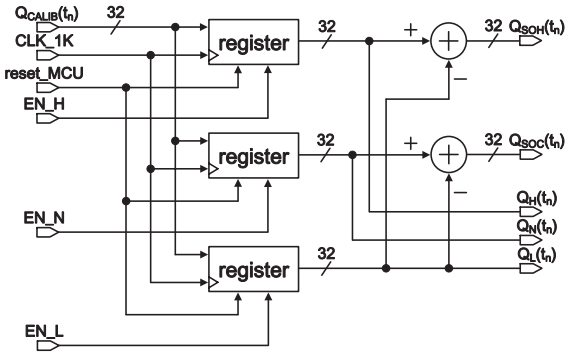

Fig. 6. Schematic of charge estimation circuit.

IV. IMPLEMENTATION AND SIMULATIONS

The proposed all-digital battery capacity monitor is implemented using a typical 0.25 μm 1P3M 60V BCD process. Fig. 7 shows the layout of this work, where the core area of the proposed design is 610 $\times$ 610 μm^2. The proposed all-digital battery capacity monitor is simulated in the 0.3 C-rate $\sim$ 1 C-rate discharging currents, as shown in Fig. 8. Fig. 9 summarizes the deviation distribution. The worst-case deviations of the calibrated and uncalibrated simulation results are -0.56 % $\sim$ 0.07 % and -2.97 % $\sim$ 0.24 %, respectively. The performance comparison of the proposed design and several prior works is tabulated in Table III. Our design attains the smallest error. The power of the proposed design is 33.2 μW. The maximum improvement of the proposed design attains 530 %. Notably, this work is the only solution realized on silicon.

V. CONCLUSION

An all-digital battery capacity monitor is proposed in this work. Since all signals of this design are manipulated in time domain, the proposed design can be implemented in a digital IC to reduce large cost and area. The proposed design is implemented using 0.25 μm 1P3M 60V BCD process for functionality verification and performance evaluation. The proposed design normalizes the capacity of the battery with

TABLE III
PERFORMANCE COMPARISON OF THE BATTERY CAPACITY MONITOR

	[7]	[5]	[6]	[8]	This work
Year	2011	2012	2012	2013	2014
Technology	online	online	online	online	0.25 μm 1P3M 60V BCD process
Estimation Method	battery model	OVC	OVC	battery model	coulomb counting method
Calibration Method	AEKF	EKF	EKF	SVM	CCEA
Max. Error (%)	2.54	-5 $\sim$ +5	-5 $\sim$ +5	6	-0.56 $\sim$ 0.07
Power (μW)	N/A	N/A	N/A	N/A	33.2
Clock (KHz)	N/A	N/A	N/A	N/A	1
Area (μm^2)	N/A	N/A	N/A	N/A	610 $\times$ 610
Max. Improvement (%)	589	N/A	N/A	N/A	530

different discharging currents (0.3 C-rate $\sim$ 1 C-rate) to attain very small error.

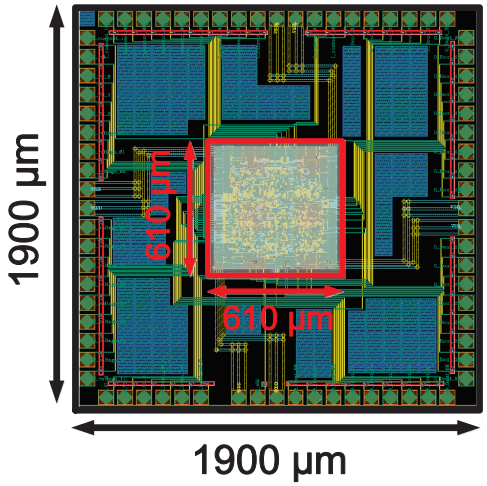

Fig. 7. Layout of the proposed all-digital battery capacity monitor.

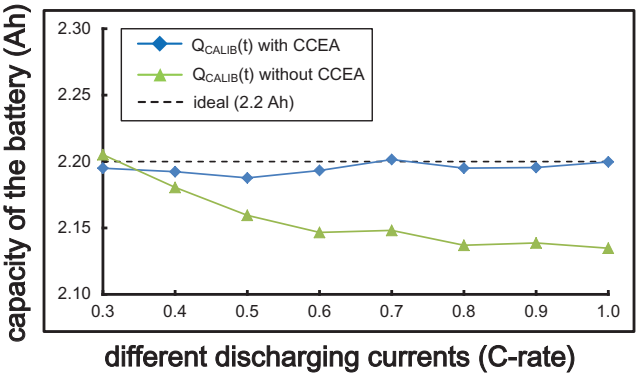

Fig. 8. Simulation results of the proposed all-digital battery capacity monitor.

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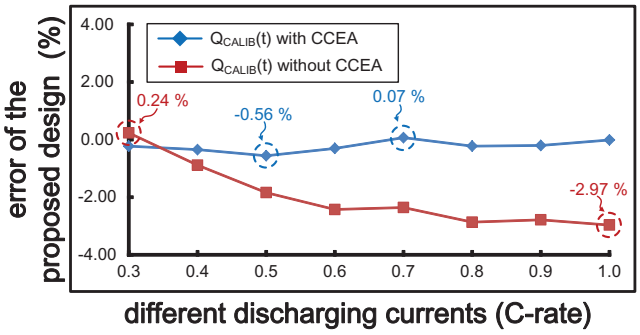

Fig. 9. Error distribution of the proposed all-digital battery capacity monitor.

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