Slew Rate Improved 2×VDD Output Buffer Using Leakage and Delay Compensation

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***Abstract*—A slew rate improved 2×VDD output buffer is proposed in the paper. By using the leakage compensation circuit, the gate oxide overstress at the output stage is avoided and the rising SR is improved. Besides, by using the Delay Buffer, the falling SR is improved by avoiding the PMOS and NMOS transistors turned on at the same time. The proposed design is carried out using a typical 90 nm CMOS process. After the leakage and delay compensation, the SR of the rising and falling edge of the output signal for VDDIO = 1.8 V is improved 27% and 22%, respectively. The maximum data rate is simulated to be 330/500 MHz for VDDIO = 1.8/1.0 V, respectively.**

Keywords—mixed-voltage; gate oxide overstress; leakage compensation

I. Introduction

PVT compensated 2×VDD output buffer is presented to adjust the output slew rate (SR) [1]. However, the gate leakage current in the nano-scale process causes over voltage and under voltage for Vsg of the PMOS transistor in the stacked output stage [2]. The over and under voltage for Vsg results in the gate oxide overstress and decreased SR (slew rate), respectively.

Thus, this paper proposes a 2×VDD output buffer with leakage and delay compensation to avoid the gate oxide overstress and the SR degradation. The SR is improved by 27% and 22% for the rising and falling edge after compensation.

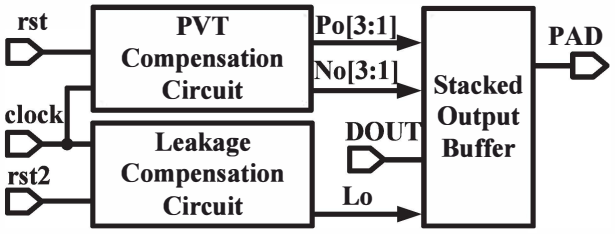

Fig. 1. Block diagram of the proposed 2xVDD output buffer.

II. The Proposed 2×VDD Output Buffer using Leakage and Delay Compenation

Fig. 1 reveals the block diagram of the proposed 2×VDD output buffer, which is composed of the PVT Compensation Circuit, Leakage Compensation Circuit, and Stacked Output Buffer. The PVT Compensation Circuit generate two digital control codes Po[3:1] and No[3:1] for controlling the on/off state of the Stacked Output Buffer based on the prior work [1]. The Leakage Compensation Circuit generates a control signal, Lo, to activate the Leakage Current Compensator for the Stacked Output Buffer.

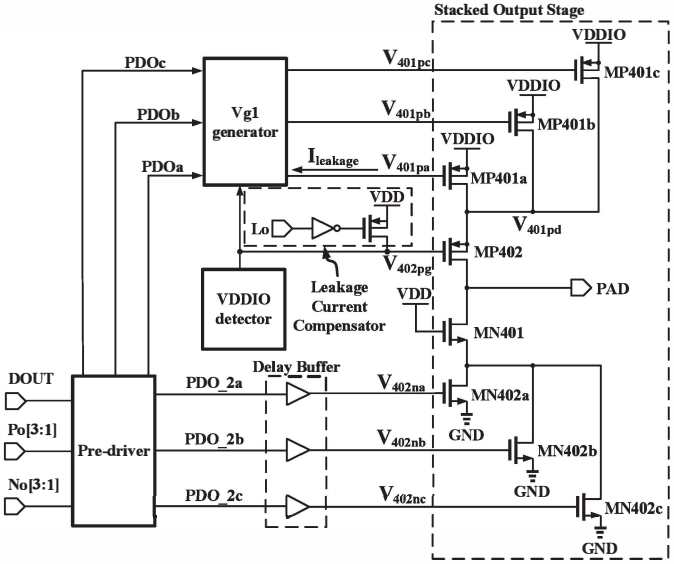

Fig. 2. Block diagram of the Stacked Output Buffer.

Fig. 2 reveals the block diagram of the Stacked Output Buffer. The Pre-driver generates the on/off control signals for the Output Stage according to DOUT, Po[3:1] and No[3:1]. Vg1 generator is a level converter to shift the control signals for the PMOS transistors, MP401a∼MP401c. The Delay Buffers are employed to compensate the delay of V_{g1} generator, thus, the falling SR is improved by avoiding the NMOS and PMOS transistors turned on at the same time. When V_{401pd} is pulled low due to the leakage current, the Leakage Current Compensator is activated by Lo to avoid the gate oxide overstress at MP401a∼MP401c and improve the rising SR.

Fig. 3 shows the schematic of the Leakage Compensation Circuit. The Output Stage Replica possesses miniaturized size of the Stacked Output Stage to avoid the high power consumption and the coupling effect due to the gate oxide capacitors. Lout is the indicator for the variation of V_{401pd} due to the leakage. By comparing Lout with the reference

voltage, VRL, the activation signal, Lo, is generated to turn on the Leakage Current Compensator. Thus, the gate oxide overstress and rising SR degradation caused by the leakage can be compensated.

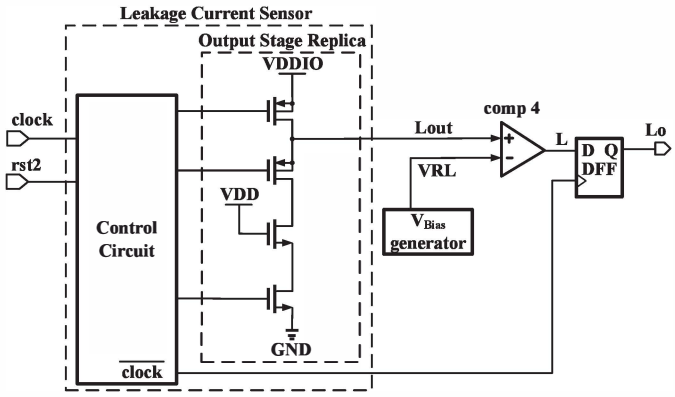

Fig. 3. Schematic of the leakage compensation circuit

III. Implementation and Simulation Results

The proposed 2×VDD Output Buffer is implemented using a typical 90 nm CMOS process. The core area is only 0.056 × 0.439 mm^2. Based on the post-layout simulation, V_{401pa} and V_{401na} rise at the same time and the transient current of MP402 is reduced, as shown in Fig. 4. Thus, the falling SR of the output signal is improved. Besides, V_{401pd} is clamped at 0.72 V after the leakage compenssation, as shown in Fig. 5. Thus, the gate oxide overstress at MP401a∼MP401c is avoided. The SR of the rising and falling edge of the output signal for VDDIO = 1.8 V is improved by 27% and 22%, respectively. Table I reveals the comparison of the specifications with several prior works. A FOM (figure of merit) is given to show the performance among these works.

TABLE I. C●MPARIS●N WITH SEVERAL PRI●R W●RKS

	This work	[1]	[3]	[4]
Year	2014	2012	2007	2004
Production	EDSSC	VLSI-DAT	ISSCC	ISSCC
Process	90 nm	90 nm	0.18 μm	0.35 μm
VDD (V)	1.0	1.2	1.8	3.3
VDDIO (V)	1.8/1.0	2.5/1.8/1.2/0.9	1.8	3.3
Data rate (MHz)	330/500	345	500	50
SR (V/ns)	1.89-2.32	1.1-2.5	2.1-3.58	N/A
Power (mW)	2.36	5.6	13.7	2.2
FOM‡	0.89	0.32	0.21	N/A

Note: ‡ FOM = $\frac{\text{Averaged SR}}{\text{Power}}$.

IV. Conclusion

This paper proposes a SR improved 2×VDD output buffer. By using the leakage and delay compensation, the gate oxide overstress is avoided. Moreover, the SR is improved by 27% and 22% for the rising and falling edge, respectively.

Acknowledgment

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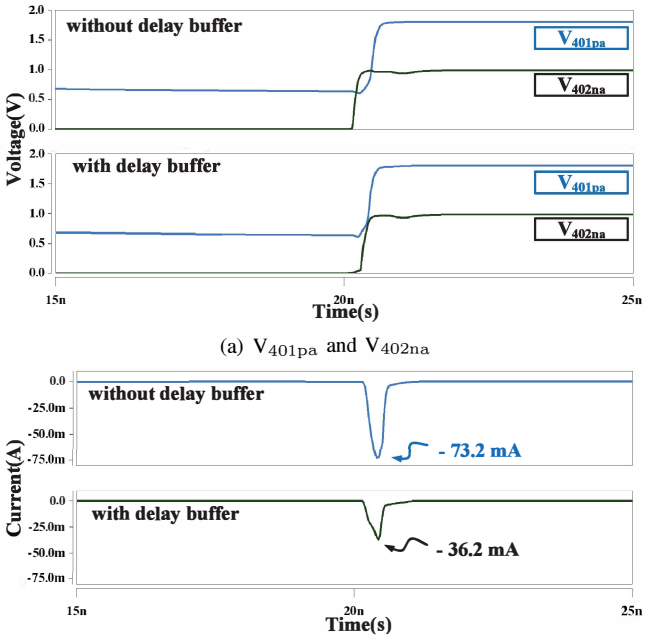

(a) V_{401pa} and V_{402na}

(b) Transient current of MP402

Fig. 4. Simulated waveforms with and without delay buffer at [TT, 25°C] for VDDIO = 1.8 V.

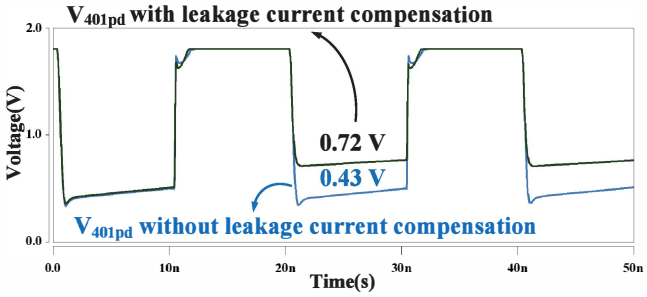

Fig. 5. Simulated V_{401pd} with and witout leakage current compensation at [TT, 25°C] for VDDIO = 1.8 V, 50 MHz data rate and 20 pF loads.

References

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