A CMOS Wide-Range Temperature Sensor with Process Compensation and Second-Order Calibration for Battery Management Systems

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***Abstract*—This paper presents a temperature sensor with process compensation and second-order calibration for Battery Management Systems (BMS). Particularly, the second-order calibrated CTAT and PTAT sensors utilizing a current mirror and an n-well resistor are used to eliminate the second-order term of the temperature coefficient such that the relationship between the output voltage and the temperature is linearized. The proposed temperature sensor is implemented using a typical 0.18 μm CMOS process. The core area and power of the proposed temperature sensor are 0.177 mm^2 and 2.0 mW, respectively. In the range from -40 ^{o}C to 125 ^{o}C, the worst deviation of the temperature sensor is -1.49 ^{o}C $\sim$ +2.13 ^{o}C at FF, TT, and SS corners, respectively. The maximum non-linearity reduction of second-order calibrated CTAT and PTAT sensors are 72.5% and 90.5%, respectively.**

***Index Terms*—second-order effects, process compensation, PTAT sensor, CTAT sensor, temperature sensor.**

I. Introduction

Nowadays, electrical vehicle (EV) is considered as a possible solution to replace conventional fossil-energy-powered vehicles in the future. Battery modules are the major energy storage in the EV. Due to the demand of safety, the EV battery modules must be protected and properly managed. For instance, the temperature of batteries in BMS is an important parameter for safety, since serious temperature rise and drop indicate the battery might be damaged or aged. A widely acceptable range of an in-car system is -40 ^{o}C to 125 ^{o}C [1], which means a temperature sensor is required to monitor the batteries in such a wide temperature range and ensure that no hazards would be caused by temperature problems.

Referring to [2]-[6], the linearity of the temperature sensor is seriously affected by process variations and non-linearity of the temperature coefficient. Thus, Jeong *et al.* proposed a method to cancel the process offset by applying the same circuit architecture to realize temperature sensors [2]. Most of the prior temperature sensors did not consider process variation effect [3]-[8]. If the temperature detection is based on Vth monitoring, the major non-linear effects of the temperature coefficient are caused second-order effects of MOSs. Lin *et al.* proposed a non-linear calibration method by isolating body effect, but this design did not consider the process variation [6]. Chung *et al.* also proposed an all-digital temperature sensor, but serious process and non-linear effects still exist [7]. Most important of all, the temperature range of these prior works was not wide enough to meet the general car electronics demand, which is up to -40 ^{o}C $\sim$ 125 ^{o}C [2]-[5], [7], [8].

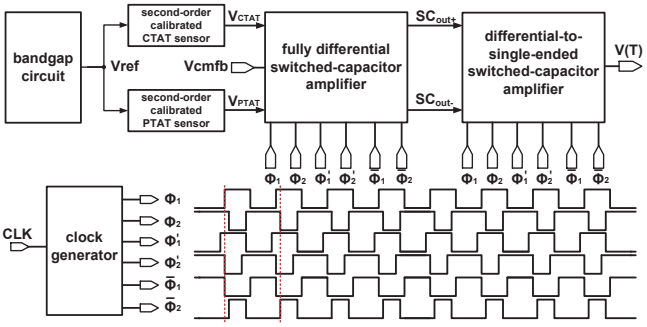

Fig. 1. The block diagram of the proposed temperature sensor.

In this study, we propose a temperature sensor with process compensation and second-order calibration to resolve all the mentioned problems. By using the proposed second-order calibrated CTAT and PTAT sensors consisting of the current mirror and n-well resistors, the linearity of proposed temperature sensor can be enhanced. The temperature range of the proposed temperature sensor is -40 ^{o}C $\sim$ 125 ^{o}C, where the worst deviation is -1.49 ^{o}C $\sim$ +2.13 ^{o}C at FF, TT, and SS corners, respectively. Notably, the maximum non-linearity reduction of the CTAT and PTAT sensors are found to be 72.5% and 90.5%, respectively.

II. Wide-Range Temperature Sensor

Fig. 1 shows the block diagram of the proposed temperature sensor composed of 6 major blocks, i.e., second-order calibrated PTAT sensor, second-order calibrated CTAT sensor, fully differential switched-capacitor amplifier, differential-to-single-ended switched-capacitor amplifier, bandgap circuit, and clock generator. A simple process compensation thought is that the same architecture must be used in CTAT and PTAT sensors to cancel process offsets [2]. That is, the same process variation at FF, TT, and SS corners will be automatically cancelled when

summed up. The fully differential switched-capacitor amplifier provides an appropriate gain for V_{CTAT} and V_{PTAT}. Then, the SC_{out^+} and SC_{out^-} are subtracted using differential-to-single-ended switched-capacitor amplifier. Notably, the second-order calibrated CTAT and PTAT sensors utilize an n-well resistor to calibrate second-order of the MOSs. Notably, the designs of the fully differential switched-capacitor amplifier, the differential-to-single-ended switched-capacitor amplifier, the bandgap circuit, and the clock generator can be easily referred in prior works or textbooks, e.g., [2], such that they will not be addressed in this paper to meet the page limitation. The details of the other function blocks are given in the following text.

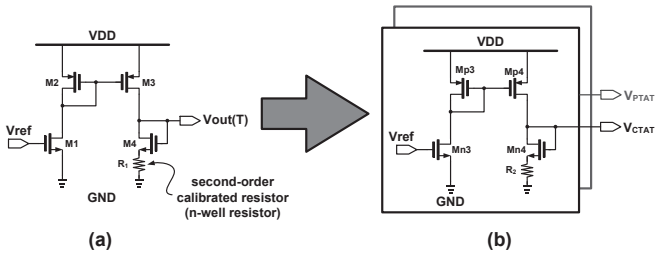

Fig. 2. Schematics of the (a) second-order calibrated temperature sensor and (b) second-order effects calibrated CTAT and PTAT sensor.

A. Theory of second-order temperature calibration

Fig. 2 (a) show the schematic of the second-order calibrated temperature sensor composed of 2 PMOSs, 2 NMOSs, and an n-well resistor. The output voltage of the second-order temperature sensor is expressed as:

$$\mathrm{Vout(T)} = \mathrm{V_{GS4}(T)} + \mathrm{I_{sat}(T)R(T)} \tag{1}$$

where T is the absolute temperature in degrees of Kelvin, $\mathrm{V_{GS4}(T)}$ is voltage difference between gate and source voltage of M4 with temperature variation, $\mathrm{I_{sat}(T)}$ is the saturation current in M4, R(T) is resistance of the n-well resistor. $\mathrm{I_{sat}(T)}$ can be expressed as [6]:

$$\mathrm{I_{sat}(T)} = \frac{1}{2}\mathrm{u(T)C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}[\mathrm{V_{GS}(T) - Vth(T)}]^2 \tag{2}$$

where W is channel width of M4, L is channel length, $\mathrm{C_{ox}}$ is oxide capacitance, u(T) is mobility, and Vth(T) is threshold voltage. u(T) and Vth(T) is defined as [6]:

$$\mathrm{u(T)} = \mathrm{u_0}(\frac{\mathrm{T}}{\mathrm{T_0}})^{\mathrm{UTE}} \tag{3}$$

$$\mathrm{Vth(T)} = \mathrm{Vth0} - \alpha(\mathrm{T} - \mathrm{T_0}) \tag{4}$$

where α can be written as $\frac{1}{\mathrm{T_0}}(\mathrm{KT1} + \frac{\mathrm{KT1L}}{\mathrm{Leff}} + \mathrm{KT2} \times \mathrm{V_{BS}})$, $\mathrm{T_0}$ is roughly equal to 298 °K or 25 °C, UTE is a negative temperature coefficient of mobility, Vth0 is the threshold voltage at $\mathrm{T_0}$, $\mathrm{u_0}$ is the mobility at $\mathrm{T_0}$, KT1 is temperature coefficient of the threshold voltage, KT1L is channel length dependence of temperature sensitivity, KT2 is body-bias coefficient of the threshold voltage with temperature variation, $\mathrm{V_{BS}}$ is the voltage difference between bulk and source voltage of M4, and α is a positive temperature coefficient. According to the above equations and the current mirror characteristic, when all MOSs are saturated, $\mathrm{I_{D1}}$ and $\mathrm{I_{D4}}$ can be written as:

$$\frac{\mathrm{I_{D1}}}{\mathrm{I_{D4}}} = \frac{\frac{\mathrm{W_2}}{\mathrm{L_2}}}{\frac{\mathrm{W_3}}{\mathrm{L_3}}} \tag{5}$$

$$\frac{\frac{1}{2}\mathrm{u(T)C_{ox}}\frac{\mathrm{W_1}}{\mathrm{L_1}}[\mathrm{V_{GS1} - Vth(T)}]^2}{\frac{1}{2}\mathrm{u(T)C_{ox}}\frac{\mathrm{W_4}}{\mathrm{L_4}}[\mathrm{V_{GS4}(T) - Vth(T)}]^2} = \frac{\frac{\mathrm{W_2}}{\mathrm{L_2}}}{\frac{\mathrm{W_3}}{\mathrm{L_3}}} \tag{6}$$

According to Eqn. (5) and Eqn. (6), $\mathrm{V_{GS4}(T)}$ can be written as:

$$\mathrm{V_{GS4}(T)} = \omega \times (\mathrm{V_{GS1}} - \mathrm{Vth0}) + \mathrm{Vth0} + \triangle\mathrm{V_{GS4}(T)} \tag{7}$$

where ω is $\sqrt{\frac{\frac{\mathrm{W_3}}{\mathrm{L_3}}}{\frac{\mathrm{W_2}}{\mathrm{L_2}}} \times \frac{\frac{\mathrm{W_1}}{\mathrm{L_1}}}{\frac{\mathrm{W_4}}{\mathrm{L_4}}}}$ and $\triangle\mathrm{V_{GS4}(T)}$ is $(\omega - 1)\alpha(\mathrm{T} - \mathrm{T_0})$. If $\mathrm{V_{GS1}}$ and $\mathrm{V_{BS}}$ are chosen appropriately, α is always very small [2]. Thus, the $\mathrm{V_{GS4}(T)}$ becomes almost a constant, which is written as:

$$\mathrm{V_{GS4}(T)} \cong \omega \times (\mathrm{V_{GS1}} - \mathrm{Vth0}) + \mathrm{Vth0} \tag{8}$$

By Eqn. (2)-(4), $\mathrm{I_{sat}(T)}$ is derived as:

$$\mathrm{I_{sat}(T)} = \frac{1}{2}\beta_0[\mathrm{V_C} + \alpha(\mathrm{T} - \mathrm{T_0})]^2(\frac{\mathrm{T}}{\mathrm{T_0}})^{\mathrm{UTE}} \tag{9}$$

where β_0 is $\mathrm{u_0C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}$ and $\mathrm{V_C}$ is $\mathrm{V_{GS4}(T)} - \mathrm{Vth0}$. Then, we use Taylor series to approximate $\mathrm{I_{sat}(T)}$,

$$\mathrm{I_{sat}(T)} \cong \mathrm{I_0}[1 + \eta(\mathrm{T} - \mathrm{T_0}) + \eta'(\mathrm{T} - \mathrm{T_0})^2] \tag{10}$$

where $\mathrm{I_0}$ is $\frac{1}{2}\beta_0\mathrm{V_C}^2$, η equals to $(\frac{2\alpha}{\mathrm{V_C}} + \frac{\mathrm{2UTE}}{596})$, and η' becomes $(\frac{\alpha^2}{\mathrm{V_C}^2} + \frac{2\alpha\mathrm{UTE}}{298\mathrm{V_C}} + \frac{\mathrm{2UTE(UTE-1)}}{4\times298^2})$. Besides, different resistances of n-well resistor vs. temperature variation is simulated in range of [-40 °C ; +125 °C], which is shown in Fig. 3. The resistance characteristic of the n-well resistor, based on these simulations can be approximated as:

$$\mathrm{R(T)} = \mathrm{R_0}[1 + \gamma(\mathrm{T} - \mathrm{T_0}) + \gamma'(\mathrm{T} - \mathrm{T_0})^2] \tag{11}$$

where $\mathrm{R_0}$ is the resistance of the n-well resistor at $\mathrm{T_0}$, and the γ and γ' are first-order and second-order temperature coefficients thereof, respectively. Thus, the $\mathrm{I_{sat}(T)} \times \mathrm{R(T)}$ is simplified as the following equation owing to the fact that γ, γ', η, and η' are always very small.

$$\mathrm{I_{sat}(T)} \times \mathrm{R(T)} \cong \mathrm{I_0R_0}[1 + \eta(\mathrm{T} - \mathrm{T_0}) + \eta'(\mathrm{T} - \mathrm{T_0})^2 + \gamma(\mathrm{T} - \mathrm{T_0}) + \gamma'(\mathrm{T} - \mathrm{T_0})^2] \tag{12}$$

If γ' is equal to -η', both the second-order terms are cancelled such that Vout(T) becomes a linear equation. Thus, Eqn. (12) is derived based on this assumption,

$$\mathrm{I_{sat}(T)} \times \mathrm{R(T)} \cong \mathrm{I_0R_0}[1 + \eta(\mathrm{T} - \mathrm{T_0}) + \gamma(\mathrm{T} - \mathrm{T_0})] \tag{13}$$

Therefore,

$$\mathrm{Vout(T)} = \mathrm{V_{GS4}(T)} + \mathrm{I_0R_0}[1 + \eta(\mathrm{T} - \mathrm{T_0}) + \gamma(\mathrm{T} - \mathrm{T_0})] \tag{14}$$

The temperature coefficient of Vout(T) becomes the following equation.

$$\frac{\partial}{\partial \mathrm{T}}(\mathrm{Vout(T)}) = \mathrm{I_0R_0}(\eta + \gamma) \tag{15}$$

According to Eqn. (15), the output of the second-order calibrated temperature sensor, Vout(T), will be a first-order (linear) function versus temperature.

Notably, the linearization of the output voltage temperature coefficient relies on the cancellation of γ' and η'. Thus, by adjusting the resistance of the n-well resistor, an appropriate second-order positive temperature coefficient (γ') of the n-well resistor will be attained to cancel the second-order effects (η') of M4.

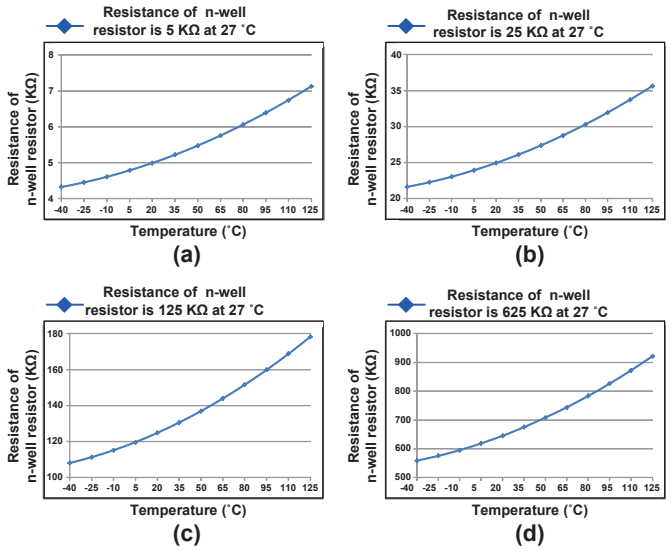

Fig. 3. Simulations of n-well resistor (a) resistance = 5 KΩ, (b) resistance = 25 KΩ, (c) resistance = 125 KΩ, and (d) resistance = 625 KΩ.

B. Second-order calibrated CTAT and PTAT sensors

Based on the second-order calibrated temperature sensor in Fig. 2 (a), the second-order effects calibrated CTAT and PTAT sensors are shown in Fig. 2 (b). According the Eqn. (14), the η and γ are negative and positive temperature coefficients, respectively. If $|\eta| > |\gamma|$, the output of the temperature sensor attains negative temperature characteristic, and vice versa. The temperature characteristic of the second-order calibrated temperature sensor is given as follows.

If $|\eta| > |\gamma|$, the description can be written as:

$$-(\frac{2\alpha}{(V_{GS4}(T) - Vth0)} + \frac{2UTE}{596}) > \gamma \quad (16)$$

According to Eqn. (8), Eqn. (16) can be written as:

$$\frac{1}{\omega} > (-\gamma - \frac{2UTE}{596})(\frac{V_{GS4}(T) - Vth0}{2\alpha}) \quad (17)$$

According to Eqn. (17), the output of the second-order calibrated temperature sensor shows a negative temperature characteristic. By contrast, if $|\eta| < |\gamma|$, the description is as follows.

$$\frac{1}{\omega} < (-\gamma - \frac{2UTE}{596})(\frac{V_{GS4}(T) - Vth0}{2\alpha}) \quad (18)$$

Thus, the output of the second-order calibrated temperature sensor attains a positive temperature feature. In summary, the second-order calibrated temperature sensor can be designed to possess either a negative or positive temperature coefficient by adjusting ω.

Besides, as addressed earlier, the fully differential switched-capacitor amplifier is used to provide an appropriate gain for V_{CTAT} and V_{PTAT}. Then, the SC_{out^+} and SC_{out^-} are subtracted by differential-to-single-ended switched-capacitor amplifier. Thus, the process variation of temperature sensor will be cancelled, as shown in Fig. 1.

III. Implementation and Simulation Results

In this work, the proposed temperature sensor is implemented using a typical 0.18 μm CMOS process. Fig. 4 shows the layout, where the core area is 0.177 mm^2. The power consumption of the proposed temperature sensor is 2.0 mW. Fig. 5 (a) and (b) show the non-calibration and calibration simulation results of the proposed CTAT sensor, respectively, while Fig. 5 (c) and (d) are those of the proposed PTAT sensor. Table I compares the non-calibrated and calibrated simulation results, where the maximum non-linearity reduction of the CTAT and PTAT sensors are 72.5% and 90.5%, respectively. The proposed temperature sensor is also simulated at FF, TT, and SS corners, as shown in Fig. 6. Fig. 7 summarizes the deviation distribution of the proposed temperature sensor at FF, TT, and SS corners. The performance comparison of the proposed design and several prior works is tabulated in Table II. In the range from -40 °C to 125 °C, the worst deviation of the temperature detector is -1.49 °C $\sim$ +2.13 °C at all process corners. Meanwhile, our design attains the smallest normalized temperature deviation and the largest FOM.

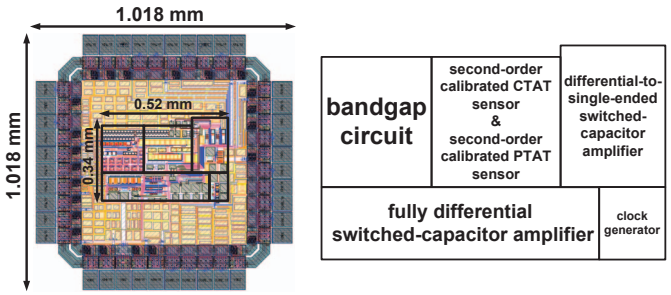

Fig. 4. Layout of the proposed temperature sensor.

TABLE I
CALIBRATION RESULTS AT CTAT SENSOR AND PTAT SENSORS

	non-calibrated results	calibrated results	Linearity improvement
CTAT sensor	1.24%	0.34%	72.5%
PTAT sensor	8.7%	0.82%	90.5%

IV. Conclusion

In this work, the proposed temperature sensor including CTAT and PTAT sensors attains process compensation and second-order calibration, where the CTAT and PTAT sensors are second-order calibrated by using a current mirror and an n-well resistor to eliminate the second-order term of the temperature coefficient. The maximum non-linearity reduction of

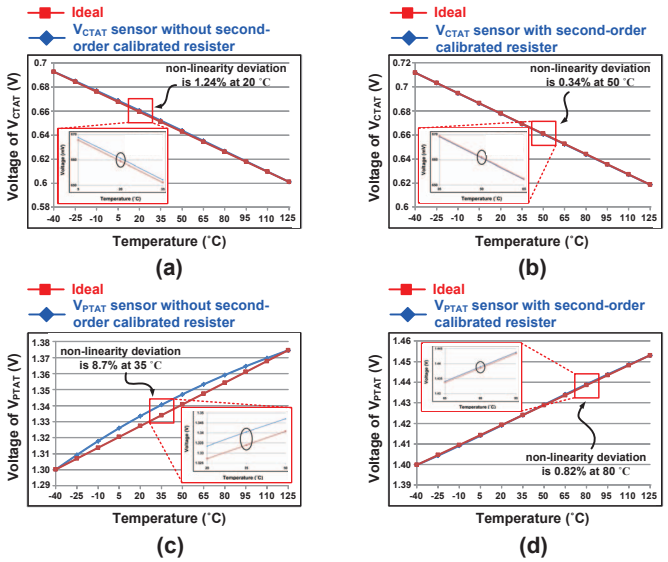

Fig. 5. Simulations of (a) non-calibrated CTAT sensor, (b) second-order calibrated CTAT sensor, (c) non-calibrated PTAT sensor, and (d) second-order calibrated PTAT sensor.

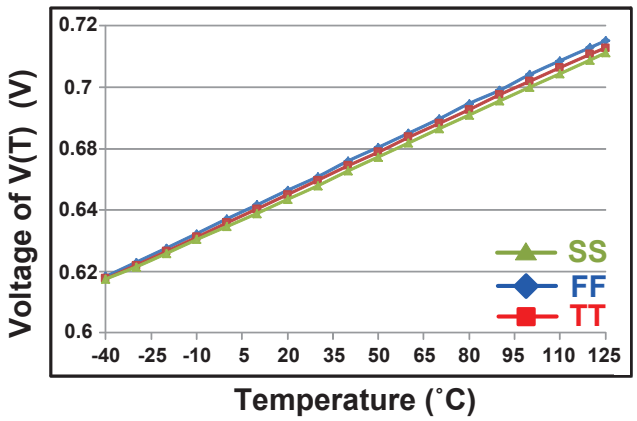

Fig. 6. Simulation results of the proposed temperature sensor at FF, TT, and SS corners.

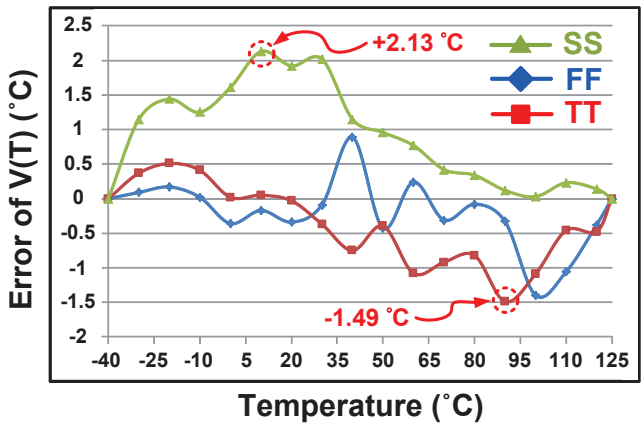

Fig. 7. Error distribution of the proposed temperature sensor at FF, TT, and SS corners.

TABLE II
PERFORMANCE COMPARISON OF TEMPERATURE SENSORS

	[7] TCAS-II	[8] TCAS-II	This work
Year	2011	2012	2013
Process (μm)	0.065	0.032	0.18
Supply Voltage (V)	1	1.65	1.8
Temperature Range (^{o}C)	0 $\sim$ 60	5 $\sim$ 100	-40 $\sim$ 125
Max. Error (^{o}C)	-5.1/+3.4	-1.95/+1.95	-1.49/+2.13
Core Area (mm^2)	0.01	0.001	0.177
Power Consumption (mW)	0.15	0.1	2.0
Normalized temperature deviation¶	0.085	0.021	0.013
FOM§	1988	126116	376381

¶: Normalized temperature deviation = $\frac{\text{Max. Error}}{\text{Temperature range}}$

§: FOM = $\frac{\text{Temerature range}}{\text{Normalized area} \times \text{Normalized power} \times \text{Normalized temperature deviation}}$

the CTAT and PTAT sensors are 72.5% and 90.5%, respectively. Lastly, the proposed temperature sensor possesses the smallest normalized temperature deviation and the best FOM to date.

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