An On-chip High-voltage Current Sensor for Battery Module Monitoring

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***Abstract*—This paper presents an on-chip high-voltage (HV) current sensor for battery module monitoring. Battery management systems (BMS) are key technology of electric vehicles (EV) or hybrid EV. BMS is assembled by battery modules consisting of series of battery cells. Owing to high supply voltage and large current, the HV current sensors are needed for security, but they are not easily implemented on chip. Thus, we proposes an on-chip high-voltage current sensor to resolve this issue. The proposed HV current sensor in this work provides a wide sensing voltage range as well as large sense current range. The proposed design is implemented using a typical 0.25 μm 1P3M 60V BCD process. The on-chip sensing current range of the proposed HV current sensor is from 0.5 A to 1 A. The error of the proposed HV current sensor is only $\pm$ 0.37 %. Notably, the sensing voltage range is up to 20 V $\sim$ 40 V.**

***Index Terms*—high voltage, current sensor, on-chip, battery module**

I. Introduction

Nowadays, electric vehicle (EV) has been considered as a key role to replace conventional fossil-energy-powered vehicles in the energy-shortage future. The EV uses electric energy from battery modules for driving motors [1]-[2]. The series battery cells consist of battery modules in EV. In this type of structures, the battery management systems (BMS) must be able to monitor state of charge (SOC), state of health (SOH), voltage, current, and temperature of each battery module or cell string. The BMS usually uses a cell-monitoring integrated circuit (IC) to carry out cell monitoring, cell protection, and charge equalization. [3]-[4]. However, these monitoring chips have to face high voltage (HV) and large current problems. If the monitoring IC is required to be integrated with other controller chips on the same die to reduce the system size, it might jeopardize the entire die, chip, and even the whole system.

Referring to [5]-[6], IGBT devices have been used for large current monitoring. Motto *et al.* proposed an IGBT-based current sensor, where a current mirror structure is used to duplicate a portion of the main emitter current to the sensing emitter [5]. A lateral insulated-gate bipolar transistor (LIGBT) structure was then proposed, which has been used in smart power IC [6]. Most of the prior current sensors were not made for high voltage system usage, because the HV designs are not easily implemented in low-voltage (LV) technology [7]-[11]. Wang *et al.* proposed a current flow path design generating a voltage drop over existing interconnects, which is used to estimate the current [7]. Shalmany *et al.* proposed a micro-power current-sensing system for battery monitoring, where a calibrated shunt resistor is used to sense current of the battery [8]. Notably, the sensing resistor of this design is implemented on chip [8]. Many other current sensors were also implemented on chip [3]-[11]. However, only one design physically included a sensing resistor on the same die [8]. Another dynamically biased shunt feedback technique current sensor was proposed, which pushes non-dominant poles to higher frequencies to enhance the speed and stability of the wide range load current in the current sensor [10]. However, this design was found to be functional only in low voltage and small sensing voltage range [7]-[11].

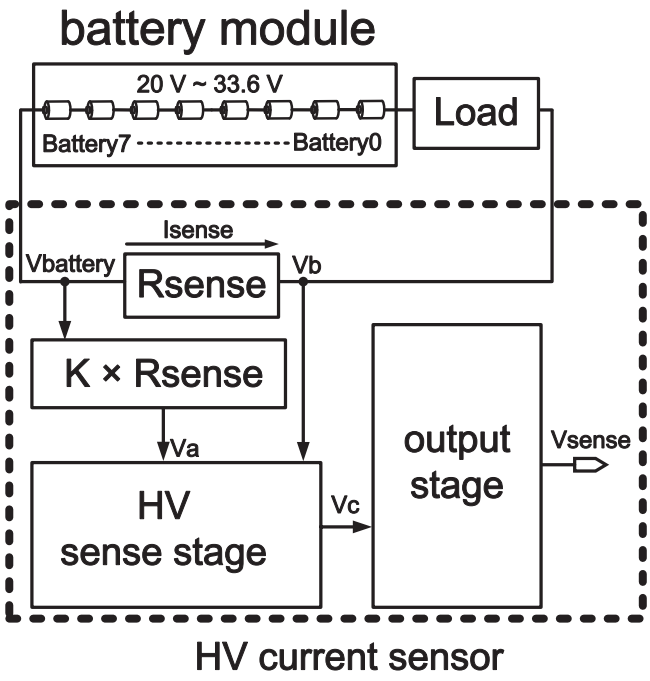

Fig. 1. The block diagram of the proposed HV current sensor.

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TABLE I
CELL SPECIFICATION OF LITHIUM-ION RECHARGEABLE BATTERY
(MODEL : IHR18650AG)

	IHR18650AG
Shape / Can material	Cylindrical / Steel
Typical Capacity	2000 mAh
Nominal Voltage	3.6 V
Charge Voltage	4.2 V
Discharge Cutoff Voltage	2.5 V

In this study, we propose an on-chip high-voltage current sensor. The proposed HV current sensor attains a wide sensing voltage and large sensing current. Take an 8-cell string, which has been deemed as a medium-size module, as an example. The discharge cutoff voltage and charge voltage of a single lithium-ion rechargeable battery are 2.5 V and 4.2 V, respectively, as shown in Table I [2]. Thus, the lowest and highest voltage of the 8-cell string will be around 20 V and 33.6 V, respectively, as shown in Fig. 1. The typical capacity of the battery cell is 2000 (mAh). The discharge and charge of the battery module is usually 0.5 C-rate (0.5 C-rate is 1 A). The on-chip sensing current range of the proposed HV current sensor is then in the range 0.5 A to 1 A, while the sensing voltage range should be up to 20 V $\sim$ 40 V for the sake of enough system margin.

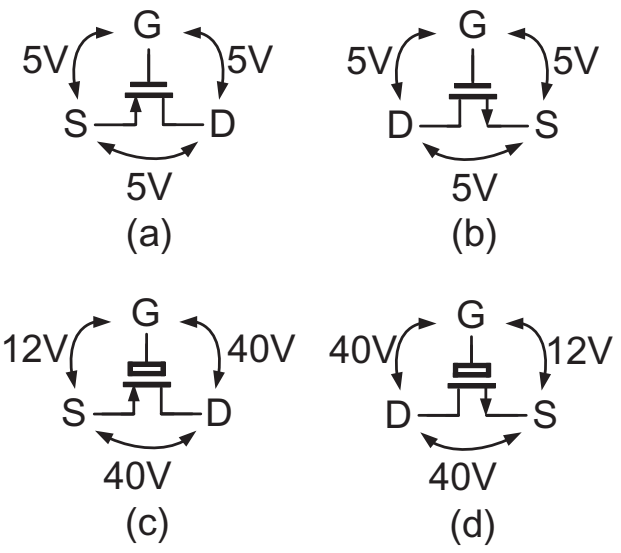

Fig. 2. Schematic of (a) LV PMOS, (b) LV NMOS, (c) HV PMOS, and (d) HV NMOS.

II. HV CURRENT SENSOR

Fig. 1 shows that the proposed HV current sensor is composed of 4 major blocks, i.e., a Rsense, a K $\times$ Rsense, a HV sense stage, and an output stage. Rsense is a very small resistor such that it will not affect the load of BMS [7]-[8]. Similarly, the current via the load must not interfere the HV current sensor. Thus, the resistance of Rsense and K $\times$ Rsense are set to be 0.01 Ω and K $\times$ 0.01 Ω, respectively. The K is selected to be 10^6. Besides, the current of battery module is always used to estimate SOC and SOH [1], [3]-[4]. Thus, the

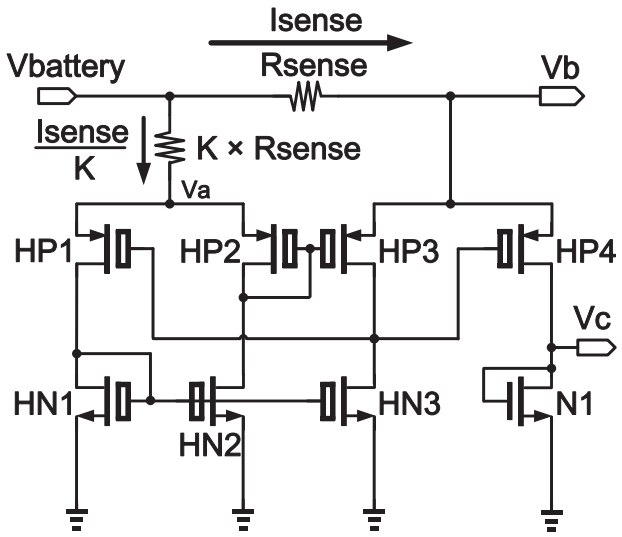

Fig. 3. Schematics of the proposed HV sense stage and two resistors.

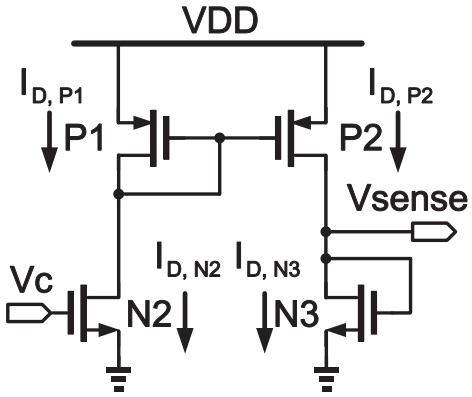

Fig. 4. Schematics of the proposed output stage.

output voltage of the proposed HV sensor must be a linearity curve with sensing current of battery module. The details of the other function blocks are given in the following text.

A. Features of MOS and sensing resistors

Fig. 2 (a) and (b) show the LV PMOS and LV NMOS, respectively, defined by the 60V BCD process. The voltage limitation is 5 V between any two terminals. By contrast, the voltage constraints of HV PMOS and HV NMOS are different, as shown in Fig. 2 (c) and (d), respectively. V_{GS} of HV PMOS and HV NMOS must be held on 12 V or less to prevent hazards.

Rsense and K $\times$ Rsense, which are made of polysillcon, and the HV sense stage are shown in Fig. 3. The current density of poly resistor is 6 $(\frac{\text{mA}}{\mu\text{m}^2})$ according the specifications of 60V BCD process. N1 of HV sense stage is a LV NMOS, which is used to match the following output stage.

B. HV sense stage

The HV sense stage in Fig. 3 composed of 4 HV PMOSs, 3 HV NMOSs, a LV NMOS and two polysilscon resistors [9]. $\frac{W_{HP2}}{L_{HP2}}$ and $\frac{W_{HN2}}{L_{HN2}}$ equal to $\frac{W_{HP3}}{L_{HP3}}$ and $\frac{W_{HN3}}{L_{HN3}}$, respectively, such that Va equals to Vb. Va and Vb can be written as Eqn. (1) and (2), respectively.

$$\mathrm{Va} = \mathrm{Vbattery} - \frac{\mathrm{Isense}}{\mathrm{K}} \times (\mathrm{K} \times \mathrm{Rsense}) \tag{1}$$

$$\mathrm{Vb} = \mathrm{Vbattery} - \mathrm{Isense} \times \mathrm{Rsense} \tag{2}$$

Rsense is selected to be very small, e.g., 0.01 Ω, to make Vbattery almost equal to Vb. K × Rsense, however, is much larger than Rsense such that the overall current will flow via Rsense, and the current in K × Rsense is very small. Vbattery then almost equals to Va. Since the voltage of one single cell string will be as high as tens of volts, the HV sense stage needs HV MOSs to resist HV stress.

Assume Isat is the saturation current in a MOS,

$$\mathrm{Isat} = \frac{1}{2}(\mathrm{u_n}\ or\ \mathrm{u_p})\mathrm{C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}(\mathrm{V_{GS}} - \mathrm{Vth})^2 \tag{3}$$

where W is the channel width of MOS, V_{GS} is the voltage difference between gate and source of the MOS, L is the channel length, C_{ox} is the oxide capacitance, u_p is the mobility of PMOS, u_n is that of NMOS, and Vth is the threshold voltage.

Vc in Fig. 3 can be written as:

$$\mathrm{Vc} = \mathrm{V_{GS,\ N1}} \approx \kappa \times \mathrm{V_{GS,\ HP4}} \tag{4}$$

where κ is $\kappa = \sqrt{\frac{W_{HP4} \times L_{N1}}{2 \times W_{N1} \times L_{HP4}}}$.

According to Eqn. (1)-(3), Eqn. (4) is re-organized as:

$$\mathrm{Vc} \approx \kappa \times (\mathrm{V_{G,\ HP4}} - \mathrm{Vb}) \tag{5}$$

The above equation indicates that Vc varies with Vb, where Vb varies with Isense shown in Eqn. (2). Thus, the output variation of HV sense stage is indirectly varied by the current in Rsense. Another important fact is that Vc can be tuned to be lower than 5 V by adjusting κ such that the HV hazards possibly attacking on the circuit can be prevented. Notably, N1 of the proposed HV current sensor is used to mirror Vc for the output stage. All of the MOSs in the output stage are LV PMOSs and NMOSs. Thus, N1 must be a LV NMOS to match those LV transistors in the output stage.

C. Output stage

The output stage composed of 2 LV PMOSs and 2 LV NMOSs is shown in Fig. 4. Assume all the MOSs are saturated in the current mirror, $I_{D,\ N2}$, $I_{D,\ N3}$, $I_{D,\ P2}$ and $I_{D,\ P1}$ attain the following equality.

$$\frac{\mathrm{I_{D,\ N3}}}{\mathrm{I_{D,\ N2}}} = \frac{\mathrm{I_{D,\ P2}}}{\mathrm{I_{D,\ P1}}} \tag{6}$$

Therefore, since $V_{GS,\ P1}$ is equal to $V_{GS,\ P2}$, Eqn. (6) is derived as follows.

$$\frac{\mathrm{I_{D,\ P2}}}{\mathrm{I_{D,\ P1}}} = \frac{\frac{\mathrm{W_{P2}}}{\mathrm{L_{P2}}}}{\frac{\mathrm{W_{P1}}}{\mathrm{L_{P1}}}} \tag{7}$$

After Eqn. (6) is substituted into Eqn. (3) and Eqn. (7), the above equation is rewritten.

$$\frac{\frac{1}{2}\mathrm{u_n C_{ox}}\frac{\mathrm{W_{N3}}}{\mathrm{L_{N3}}}[\mathrm{Vsense} - \mathrm{Vth}]^2}{\frac{1}{2}\mathrm{u_n C_{ox}}\frac{\mathrm{W_{N2}}}{\mathrm{L_{N2}}}[\mathrm{Vc} - \mathrm{Vth}]^2} = \frac{\frac{\mathrm{W_{P2}}}{\mathrm{L_{P2}}}}{\frac{\mathrm{W_{P1}}}{\mathrm{L_{P1}}}} \tag{8}$$

Thus,

$$\mathrm{Vsense} = \mathrm{Vc} \times \omega + (1 - \omega) \times \mathrm{Vth} \tag{9}$$

where ω is $\omega = \sqrt{\frac{\frac{W_{P2}}{L_{P2}}}{\frac{W_{P1}}{L_{P1}}} \times \frac{\frac{W_{N2}}{L_{N2}}}{\frac{W_{N3}}{L_{N3}}}}$.

Eqn. (9) demonstrates a conclusion that the output range and the linearity of output stage can be ensured by tuning ω.

III. Implementation and simulations

In this work, the proposed current sensor is implemented using a typical 0.25 μm 1P3M 60V BCD process. Fig. 5 shows the layout of a HV voltage detector and the proposed HV current sensor, where the core area of the HV current sensor is 0.902 × 1.026 mm^2. The power consumption of the current sensor is 2.0 mW given that Vbattery is 40 V. The proposed current sensor is also simulated with an on-chip sensing current range from 0.5 A to 1 A, where the worst case of all-PVT corners is shown in Fig. 6. The output range of the HV current sensor, Vsense, is from 2.03 V to 3.27 V. Fig. 7 summarizes the deviation distribution of the proposed HV current sensor, where the maximum error is only ± 0.37 % in all-PVT-corner simulations. The performance comparison of the proposed design and several recent works is tabulated in Table II. Notably, our design is the only one to work in the range of 20 V ∼ 40 V to meet the demand of HV current sensing.

TABLE II
Performance Comparison of Current Sensors

	[10] TCAS-I	[8] ISSCC	This work
Year	2010	2013	2014
Process (μm)	0.35	0.13	0.25
Supply Voltage (V)	3.3	1.5	5
Sensing Voltage Range (V)	2.7 ∼ 4.2	0 ∼ 1.5	20 ∼ 40
Sensing Current Range (A)	0.025∼0.5$^{\xi}$	0∼1¶	0.5∼1¶
Max. Error	5 %	± 0.03 %	± 0.37 %
Core Area (mm^2)	1.1	1.1	0.925

Note: ¶: The sensing load on chip.

Note: $^{\xi}$: The sensing load off chip.

IV. Conclusion

This paper presents an on-chip HV current sensor for battery module monitoring. The proposed design is implemented using a typical 0.25 μm 1P3M 60V BCD process. The on-chip sensing current range of the proposed HV current sensor is from 0.5 A to 1 A. Besides, the operating voltage of the HV current sensor is as high as 20 V ∼ 40 V.

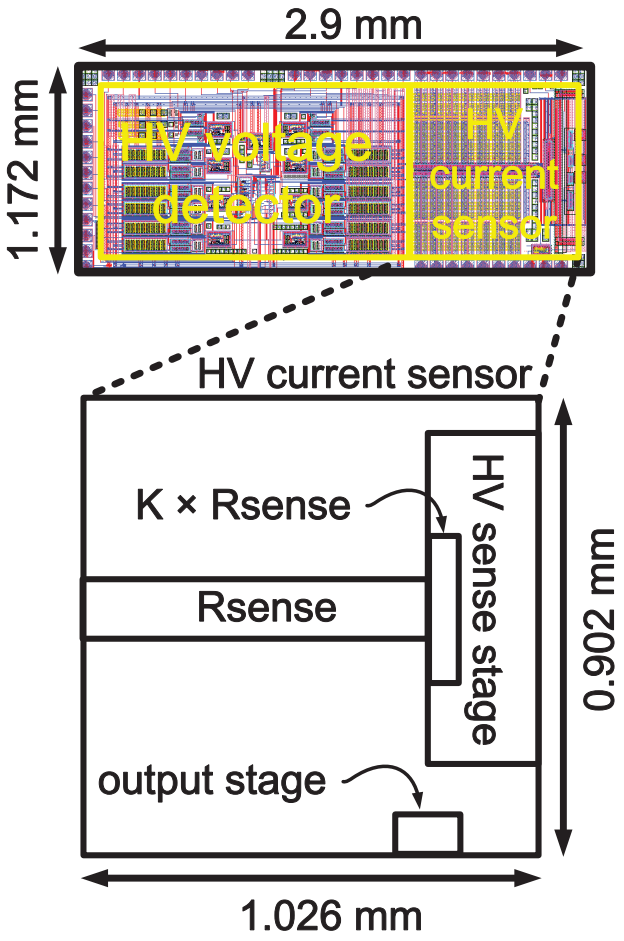

Fig. 5. Layout of the proposed HV current sensor.

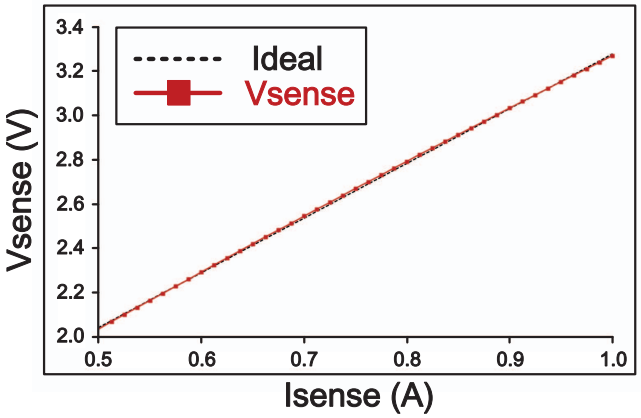

Fig. 6. Simulation results of the proposed HV current sensor.

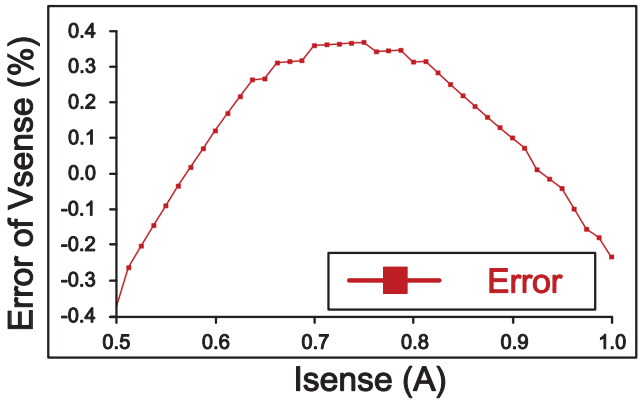

Fig. 7. Error distribution of the proposed HV current sensor.

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