32% Slew Rate and 27% Data Rate Improved 2×VDD Output Buffer Using PVTL Compensation

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***Abstract*—A 2×VDD Output Buffer using PVTL compensation is proposed in this paper. Beside the PVT compensation, a Leakage compensation circuit is employed. With the proposed Leakage compensation circuit, the SR (slew rate) and data rate are improved by 32% and 27%, respectively, for VDDIO = 1.8 V at the worst case. Moreover, the reliability problem caused by the unstable voltage, gate oxide overstress and hot carrier degradation is avoided. The proposed design is implemented using a typical 90 nm CMOS process. The core area is 0.425 mm × 0.0563 mm. The SR is simulated to be 1.3-3.0 V/ns. The data rate is simulated to be 454, 370, and 500 MHz for VDDIO = 1.8, 1.2, and 1.0 V, respectively.**

Keywords—leakage compensation, slew rate, nano scale, mixed-voltage, output buffer

I. Introduction

With the development of semiconductor technology, the advanced CMOS processes are released for implementing low power and high speed digital systems in several years. In order to communicate with chips using different processes in a PCB system, 2×VDD output buffers are presented to operate with different suppply voltages. To obtain the good transmission quality in extreme environments, the slew rate is adjusted in the output buffers using PLL [1], DLL [2], SLL (speed-locked loop) [3] based and PVT (process, voltage, and temperature) [4] compensation. However, these compensation circuits cannot be applied to 2×VDD output buffers. Therefore, the PVT compensation for the slew rate of 2×VDD output buffers are presented recently [5], [6].

However, these prior works do not consider the leakage problem. The leakage current is a severe problem due to the direct tunneling and FN (Fowler-Nording) tunneling in nano scale CMOS process [7]. The leakage current results in unstable gate bias voltages at the output stage of 2×VDD output buffer. The unstable gate bias voltages cause the SR (slew rate) reduction. And what's even worse, it causes the reliability problem due to the gate oxide overstress and hot carrier degradation if the voltage differences across the terminals of the transistors are larger than the tolerant voltage.

Thus, this paper proposes the PVTL (process, voltage, temperature, and leakage) compensation for SR of 2×VDD Output Buffer in a 90 nm CMOS process. By employing the proposed Leakage compensation circuit, the slew rate and data rate are improved by 32% and 27%, respectively, for VDDIO =1.8 V at the worst case. Besides, the reliability problem caused by the leakage current is avoided.

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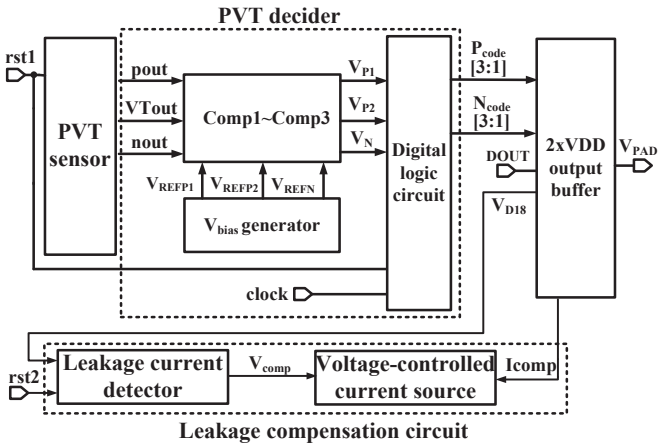

Fig. 1. Block diagram of the proposed 2×VDD Output Buffer using PVTL compensation.

II. The Proposed 2×VDD Output Buffer using PVTL Compensation

Fig. 1 shows the block diagram of the proposed 2×VDD Output Buffer, which is composed of the PVT sensor, PVT decider, Leakage compensation circuit, and 2×VDD output buffer.

A. PVT compensation

The PVT sensor and PVT decider are employed for the PVT compensation based on the prior work [8]. The PVT Sensor generates two self-discharged signals, pout and VTout, whose discharging rate is corresponding to the PMOS corner and the temperature, respectively. Moreover, they are finally clamped at around 2×Vth of PMOS. Similarly, nout is a self-charging signal with the charging rate proportional to the variation due to the NMOS corner. The signal, nout, is finally clamped at VDD−2×Vth of NMOS. By comparing pout, VTout, and nout with three reference voltages generated by $V_{\rm bias}$ generator, the three comparators, Comp1∼Comp3, generate three signals, V_{P1}, V_{P2}, and V_N. The required time for the rising edge of

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V_{P1}, V_{P2}, as well as the falling edge of V_N, would vary according to the PVT corners. By detecting the required times for the edge using counters, the Digital logic circuit generates two digital codes, P_{code}[3:1] and N_{code}[3:1], to compensate the SR of the 2×VDD output buffer.

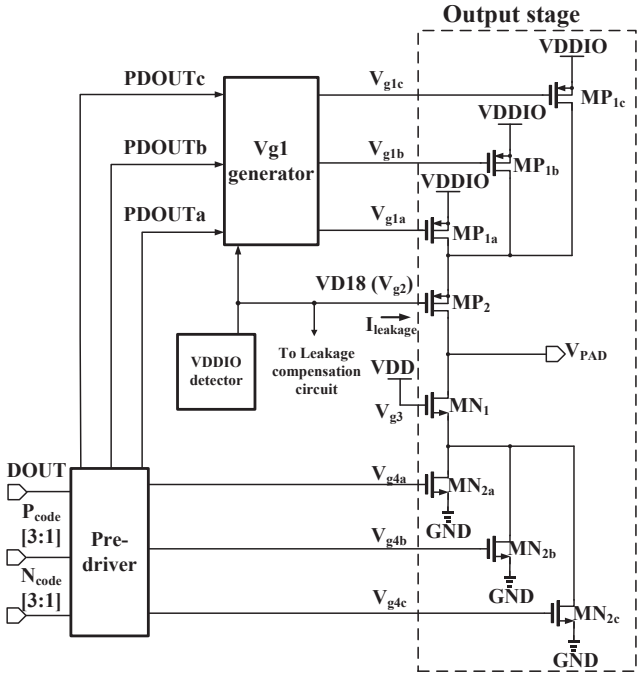

Fig. 2. Block diagram of the 2xVDD output buffer.

B. 2×VDD output buffer

Fig. 2 reveals the schematic of the 2×VDD output buffer. The Pre-driver receives the PVT codes, P_{code}[3:1] and N_{code}[3:1], as well as the data signal, Dout. The Pre-driver generates the require gate bias signals, PDOUTa∼PDOUTc and V_{g4a}∼V_{g4c}, for the Output stage. The Output stage is composed of the stacked PMOS and NMOS transistors to avoid the gate oxide overstress for VDDIO = 1.8 V. The parallel NMOS transistors, MN_{2a}∼MN_{2c}, are controlled by V_{g4a}∼V_{g4c} to compensate the SR for the falling edge of the output signal, V_{PAD}. Similarly, MP_{1a}∼MP_{1c} are controlled by the level-shifted signal V_{g1a}∼V_{g1c} to compensate the SR for the rising edge of V_{PAD}. The level-shifted signals, V_{g1a}∼V_{g1c}, are generated by the V_{g1} generator which is a level shifter according to the signals PDOUTa∼PDOUTc and VD18. VD18 is generated by the VDDIO detector, which is 0.6 V for VDDIO = 1.8 V and 0 V for VDDIO ≤ 1.2 V. By employing the V_{g1} generator and VDDIO detector, the gate bias signals, V_{g1a}∼V_{g1c} and VD18, are generated to compensate the rising SR according to the PVT corner and avoid the gate oxide overstress in all VDDIO modes. The required gate bias voltages for different VDDIO modes are revealed in Table I.

TABLE I
THE TRUTH TABLE FOR THE GATE BIAS VOLTAGES

VDDIO mode	V_{g1x} (Tx1/Tx0,Rx)	V_{g2}	V_{g3}	V_{g4x} (Tx1/Tx0,Rx)
1.8 V	0.6/1.8 V	0.6 V	1.0 V	0/1.0 V
1.2 V	0/1.2 V	0 V	1.0 V	0/1.0 V
1.0 V	0/1.0 V	0 V	1.0 V	0/1.0 V

Note: V_{g1x} refers to V_{g1a}∼V_{g1c}.
V_{g4x} refers to V_{g1a}∼V_{g4c}.
Tx1 indicates for transmitting logic 1.
Tx0 indicates for transmitting logic 0.

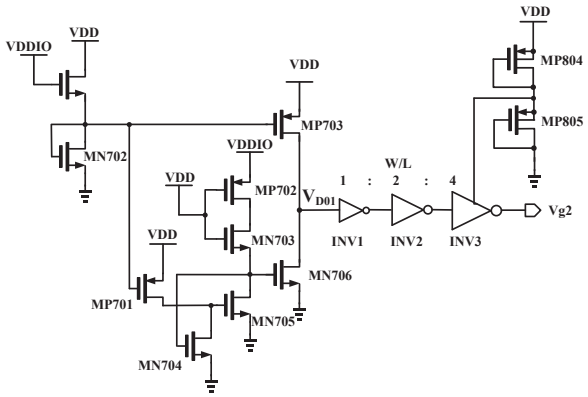

Fig. 3. Schematic of the VDDIO detector.

C. VDDIO detector

Fig. 3 shows the schematic of the VDDIO detector. When VDDIO = 1.8 V, MP702, MN703, and MN704 are turned on such that MN706 is turned on. It pulls V_{D01} to 0 V. With the three cascaded inverters as driving buffers, the gate bias signal, V_{g2}, is at the high state. Because the supply voltage of the inverter, INV3, is biased at the divided voltage of MP804 and MP805, V_{g2} is charged and clamped at 0.6 V. When VDDIO = 1.2/1.0 V, MP702 and MN706 are turned off. At the same time, MP703 and MP701 are turned on to pull V_{D01} to 1.0 V. With the three cascaded inverters, V_{g2} is biased at 0 V. Thus, V_{g2} is 0.6 V for VDDIO = 1.8 V and 0 V for VDDIO = 1.2/1.0 V.

D. Leakage compensation circuit

Fig. 4 shows the schematic of the Leakage compensation circuit, which is composed of the Leakage current detector and the Voltage-controlled current source. MP803∼MP805 and MN801∼MN802 are a single stage comparator with the positive input biased at VD18 and the negative input biased at V_{REF18}. V_{REF18} is generated by the VDDIO detector 2, which is the replica of the VDDIO detector. Notably, VDDIO detector 2 operates without the loading effect and leakage effect caused by the great-size PMOS transistor MP_2. When VD18 > V_{REF18}, V_x is biased at VDD. It turns on MN803 such that V_{comp} is pulled to 0 V. Thus, MN805 and MN806 are turned off. The compensation current I_{comp} is zero. When VD18 < V_{REF18}, V_x is biased at 0 V. MN803 is then turned

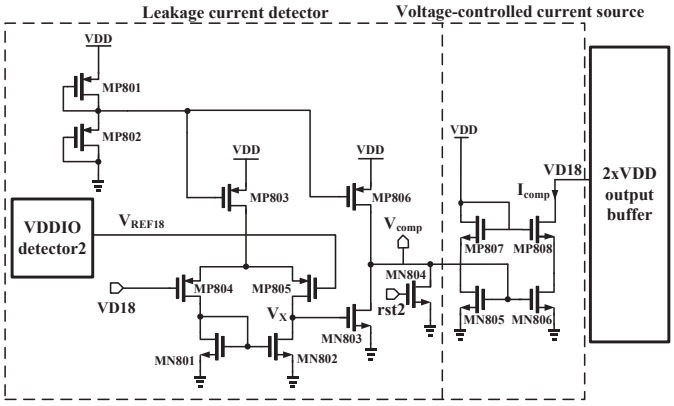

Fig. 4. Schematic of the Leakage compensation circuit.

off such that V_{comp} is pulled to VDD. MN805 and MN806 are turned on. The compensation current, I_{comp}, is determined by the transistors of MP807, MN805 and MN806. By tuning the values of W/L of MP807, MN805 and MN806, the leakage current, $I_{leakage}$, at MP_2 can be compensated.

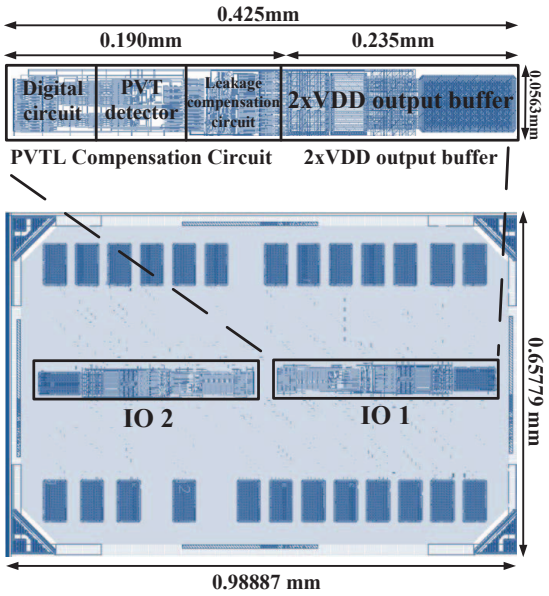

Fig. 5. Layout of the proposed 2xVDD Output Buffer.

III. Implementation and Simulation Results

The proposed 2×VDD Output Buffer is implemented using a typical 90 nm CMOS process. The core area is 0.425 mm × 0.0563 mm, as shown in Fig. 5. By using the proposed PVTL compensation, the data rate is simulated to be 454, 370, and 500 MHz for VDDIO = 1.8, 1.2, and 1.0 V, respectively, as shown in Fig. 6. Referring to Fig. 7 and 8, the leakage current is reduced and V_{g2} is pulled back to 0.6 V and 0 V for VDDIO = 1.8 and 1.2 V, respectively, after the leakage compensation. It increases the Vsg of MP_2 and improves the SR of the rising edge for V_{PAD}.

After the leakage compensation, the ripple of V_{g2} is reduced and the rising SR is improved from 2.275 V/ns to 3.0 V/ns for VDDIO = 1.8 V, as shown in Fig. 9. Morevoer, the falling SR is improved from 1.971 V/ns to 2.641 V/ns. Referring to Fig. 10, the rising SR is improved from 0.61 V/ns to 1.23 V/ns for VDDIO = 1.2 V. For VDDIO = 1.0 V, the rising SR is improved from 1.939 V/ns to 1.95 V/ns, as shown in Fig. 11. Table II shows the improved data rate and SR for 20 pF capacitive load and VDDIO = 1.8/1.2/1.0 V at the worst case. The data rate is improved by 27% for VDDIO = 1.8 V. The SR is improved by 32% at the worst case for VDDIO = 1.8 V. Table III reveals the comparison of the specifications with several prior works using only PVT compensation. The proposed design possesses the fast data rate among these prior works. The SR is better than the prior works [6] and [8] under the worst condition with the capacitive load of 20 pF.

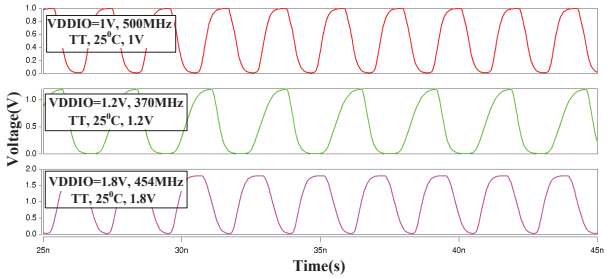

Fig. 6. Simulated V_{PAD} with maximum data rate for capacitive load of 20 pF at different corners.

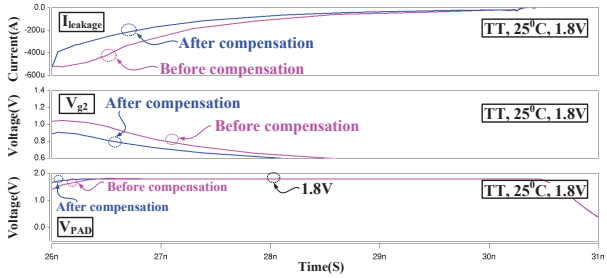

Fig. 7. Simulated waveforms of $I_{leakage}$, V_{g2} and V_{PAD} for VDDIO = 1.8 V before and after leakage compensation.

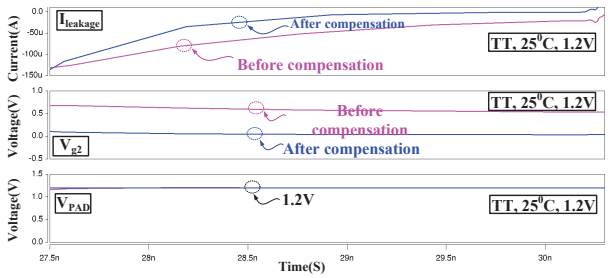

Fig. 8. Simulated waveforms of $I_{leakage}$, V_{g2} and V_{PAD} for VDDIO = 1.2 V before and after leakage compensation.

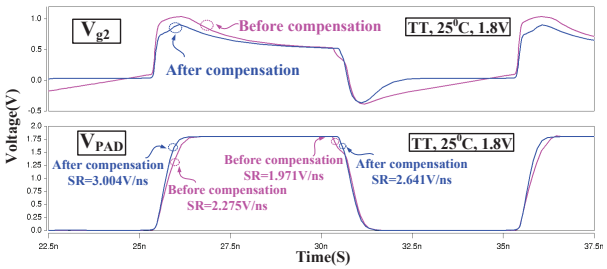

Fig. 9. Before and after leakage compensation of simulated V_{g2} and V_{PAD} at the corner of [TT, 25^{o}C] and VDDIO = 1.8 V.

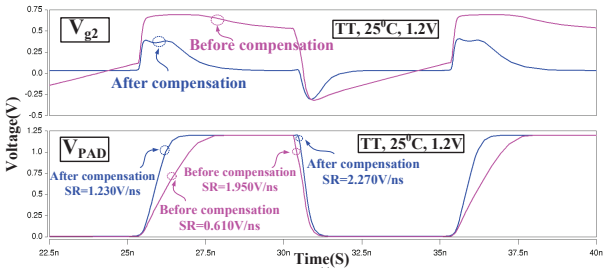

Fig. 10. Before and after leakage compensation of simulated V_{g2} and V_{PAD} at the corner of [TT, 25^{o}C] and VDDIO = 1.2 V.

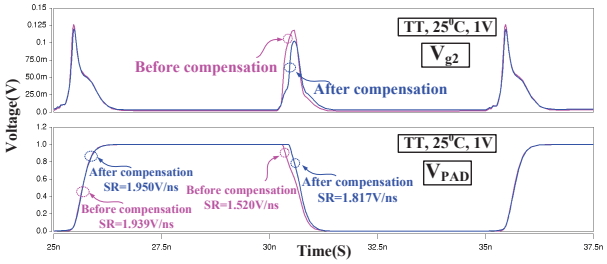

Fig. 11. Before and after leakage compensation of simulated V_{g2} and V_{PAD} at the corner of [TT, 25^{o}C] and VDDIO = 1.0 V.

TABLE II
SIMULATED IMPROVEMENT OF DATA RATE AND SR FOR THE WORST CASE WITH 20 PF LOAD.

VDDIO	1.8 V	1.2 V	1.0 V
Improved data rate (MHz)	+27% (357→454)	+63% (227→370)	+15% (434→500)
Improved rising SR (V/ns)	+32%* (2.275→3.004)	+93.48%¶ (0.372→0.719)	+0.011%¶ (1.237→1.248)
Improved falling SR (V/ns)	+34%* (1.971→2.641)	+8.65%¶ (1.421→1.544)	+23.2%¶ (1.034→1.274)

* This corner is at [TT, 25^{o}C] for VDD = 0.9 V, data rate = 100 MHz.
¶ This corner is at [SS, 100^{o}C] for VDD = 0.9 V, data rate = 100 MHz.

TABLE III
COMPARISON WITH SEVERAL PRIOR WORKS

	This work	[6]	[5]	[8]
Year	2014	2013	2013	2012
Production	ICICDT	TCAS-I	TCAS-I	VLSI-DAT
Process	90 nm	0.18 μm	90 nm	90 nm
VDD (V)	1.0	1.8	1.2	1.2
VDDIO (V)	1.8/1.2/1.0	3.3/1.8	2.5/1.2	2.5/1.8/1.2/0.9
Data rate (MHz) (Loads)	454/370/500 (20 pF)	120 (10 pF)	125 (15 pF)	345 (N/A)
SR (V/ns)	1.3-3.0	1.28-2.79	2.1-3.4	1.1-2.5
Power (mW)	4.627	0.427	N/A	5.6
Compensation	PVTL	PVT	PVT	PVT

IV. CONCLUSION

This paper proposes the 2×VDD output buffer with PVTL compensation. By using the proposed Leakage current compensation, the gate oxide overstress is avoided. Moreover, the SR is improved by 32% for the rising edge for VDDIO = 1.8 V. The data rate is improved by 27% for VDDIO = 1.8 V.

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REFERENCES

[1] S.-K. Shin, W. Yu, Y.-H. Jun, J.-W. Kim, and B.-S. Kong, et al., "A slew rate controlled output driver using PLL as compensation circuit," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1227-1233, Jul. 2003.

[2] T. Matano, Y. Takai, T. Takahashi, Y. Sakito, I. Fujii, and Takaishi, et al., "A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slewrate-controlled output buffer," *IEEE J. Solid-State Circuits*, vol. 38, no.5, pp. 762-768, May 2003.

[3] M. Bazes, "Output buffer impedance control and noise reduction using a speed-locked loop," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 1, pp. 486-541, Sep. 2004.

[4] Y.-H. Kwak, I. Jung, H.-D. Lee, Y.-J. Choi, Y. Kumar, and C. Kim, "A one cycle lock time slew-rate-controlled output driver," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech.*, Papers, pp. 408-611, Feb. 2007.

[5] M.-D. Ker, and P.-Y. Chiu, "Design of 2×V_{DD}-tolerant I/O buffer with PVT compensation realized by only 1×V_{DD} thin-oxide devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 10, pp. 2549-2560, 2013.

[6] C.-C. Wang, C.-L. Chen, R.-C. Kuo, H.-Y. Tseng, J.-W. Liu, and C.-Y. Juan, "On-chip process and temperature monitor for self-adjusting slew rate control of 2×VDD output buffers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 6, pp. 1432-1440, 2013.

[7] A. Mishra, and R.-A. Mishra, "Leakage current minimization in dynamic circuits using sleep switch," *Students Conference on Engineering and System(SCES)*, pp. 1-6, Mar. 2012.

[8] C.-L. Chen, H. -Y. Tseng, R. -C. Kuo, and C. -C. Wang, "A slew rate self-adjusting 2×VDD output buffer with PVT compensation," *2012 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT)*, Apr. 2012.