A 50-MHz Clock Generator with Voltage and Temperature Compensation Using Low Dropout Regulator

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***Abstract*—This paper presents a clock generator featuring a feedback temperature and voltage compensation circuit and low dropout regulator circuit on-chip capable of constraining frequency variation to 3.49 %. The inclusion of an OPA, MOS transistors and resistors eliminates the need of large BJT devices to reduce the area penalty and achieve low power consumption. Particularly, a negative feedback temperature compensation bias circuit utilizes only a MOS transistor and a resistor to improve compensation capability. The proposed design is implemented using TSMC 0.18 μm CMOS process followed by simulation in the temperature range between of 0 ^{o}C to 100 ^{o}C. The post-layout-extracted simulation results reveal that the worst-case error is less than 2 mV with calibration, which is 72 % improvement compared with the state of art.**

***Index Terms*—clock generator, voltage, temperature, compensation, low dropout regulator, low power consumption**

I. Introduction

Stable clock generator is a crucial component of many systems, e.g., microprocessor [1], digital radio [2], and biomedical device [3]. Kurit *et al.* proposed a PLL-based clock generator with loop filters to avoid the noise and reduce the influence of temperature variation [1]. However, this approach is still susceptible to process variation due to the inclusion of analog components. Another reported approach is to use a resistor-capacitor (RC) delay, where the size of the capacitor is controlled by an external control signal to eliminate process and temperature variations [2]. However, this method requires an external clock source increasing the overall size and the cost of the chip. This paper proposes a frequency generator with a low dropout regulator to reduce the impact of temperature and voltage variation thereby ensuring a stable output frequency and full integration on a single chip.

II. Temperature and voltage Compensation Clock Generator

Fig. 1 outlines the architecture of the clock generator presented in this paper. The clock generator block comprises a low dropout (LDO) regulator, a feedback temperature compensation circuit, a replica bias circuit, a differential ring oscillator (DRO), and a differential-to-single-end converter. The low dropout regulator provides a temperature-independent reference-regulated power signal ($\mathrm{V_{ref}}$), which serves as a stable supply voltage for other components to ensure a favorable power supply rejection ratio (PSRR). The DRO generates a reference frequency using three delay stages with the feedback temperature compensation circuit generating the compensation voltage ($\mathrm{V_{COMP}}$) required to ensure the generation of a stable output frequency. The replica bias circuit duplicates $\mathrm{V_{COMP}}$ to be the control signal, $\mathrm{V_{CTRL}}$. Since, the DRO is indirectly biased by $\mathrm{V_{COMP}}$ (equal to $\mathrm{V_{CTRL}}$), the feedback temperature compensation circuit remains isolated from the noisy oscillator while controlling the oscillation frequency of the DRO. The DRO generates a reference frequency corresponding to replica bias voltage to deliver a pair of differential oscillated signals, Vop and Von, to the following differential-to-single-end converter. A single-end signal, Vout, will then be generated. The design of DRO, replica bias circuit, and differential-to-single-end converter are the same as those corresponding circuits in our previous work [5]. The other two blocks are described in the text below.

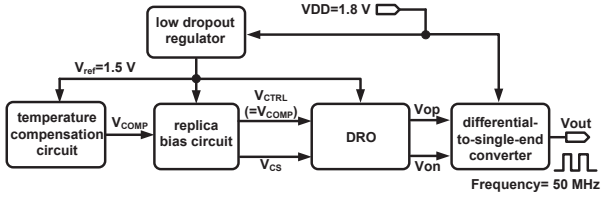

Fig. 1. Block diagram of the proposed temperature and process compensation clock generator.

A. low dropout (LDO) regulator

Fig. 2 shows block diagram of the proposed low dropout (LDO) regulator mainly comprising a bandgap circuit, an error amplifier (EA_1), and a voltage divider composed of resistors R202 and R203. The bandgap circuit provides a stable supply voltage without temperature and process drifting [7]. EA_1 is used to reduce the noise coupled from VDD and provide a source and gate potential drop to match M222 and M223. Beside, EA_1 is capable of increasing the gain to provide a precise output voltage ($\mathrm{V_{ref}}$) of LDO [8]. M224 and M225 are connected to the same source (VDD) such that the same current is forced through each side of the voltage reference resulting in the same voltage potential. The cascode structure

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of M222 and M223 is used to force the pass transistor (M224) into saturation. M225 and M226 provide an appropriate bias voltage to ensure that M222 and M223 are in saturation status. A description of this circuit is given in the following text.

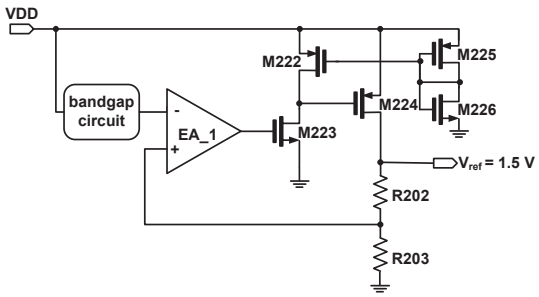

Fig. 2. Schematic of the low dropout (LDO) regulator.

*1) error amplifier (*EA_1): The speed and the gain of the LDO are mainly determined by the error amplifier and the loop therewith. EA_1 in Fig. 3 is capable of providing high gain independent of power-supply voltage and process parameters [9], while ensuring a highly accurate LDO output voltage. M234 $\sim$ M239 and R205 consists a bias circuit to provide an independent and stable transconductance. The differential input stage and the following compensation-source stage provide wide input bandwidth range, while M215 is biased into the triode region acting as a drain-source connected resistor. A compensation path is composed of this D-S-connect resistor and a capacitor (C1) to fasten the step response. Moreover, the output stage also provides a large gain to ensure a precise output voltage of LDO.

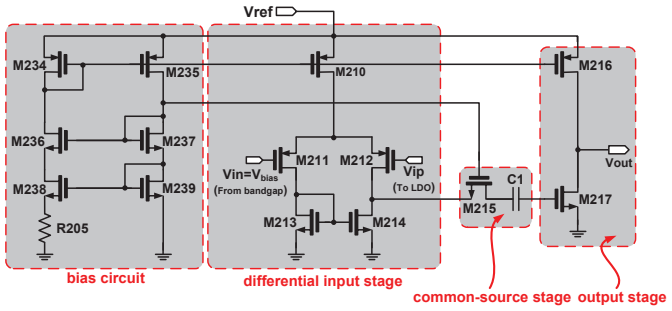

Fig. 3. Schematic of the error amplifier (EA_1). [9]

2) bandgap circuit: The bandgap circuit generates a stable voltage resisting the process and temperature variations. The detailed circuit is shown in Fig. 4. The start-up circuit is used as a positive feedback beta-multiplier reference circuit to provide an initial DC voltage to start up the bias circuit swiftly. The regulation loop comprises an error amplifier, EA_2, forces the drain and gate of M227 and M228 to the same potential. Notably, the circuit of EA_2 is the same as that of EA_1. Because the gate and the source voltages of M229 and M230 are at the same potential, the same current is forced through each side of the reference. When the currents flowing through the two current paths are nearly identical, the sensitivity of the circuit to VDD variation is reduced, thereby generating a stable bias voltage (V_{bias}).

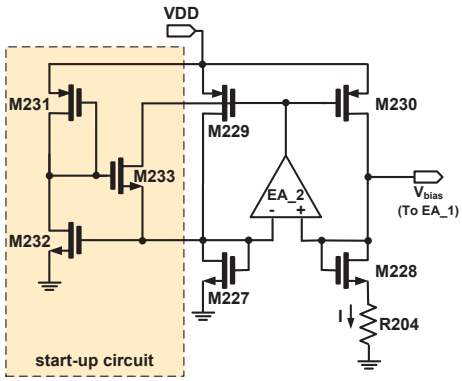

Fig. 4. Schematic of the bandgap circuit.

B. temperature compensation circuit

According to [5], a stable output frequency can only be attained by the application of an external voltage to compensate for variations in temperature and process. Thus, a temperature compensation circuit as shown in Fig. 5 (a) is proposed, where the threshold voltage (V_{T218}) and V_{GS218} of M218 decrease with an increase in temperature. The variation of the output compensation voltage with respect to temperature is formulated as follows.

$$V_{COMP} = V_{ref} - I_{CO} \cdot R_{201}, \tag{1}$$

The small signal model I_{CO} and V_{COMP} of the temperature compensation circuit can be approximated as

$$I_{CO} = \frac{V_{ref}}{R_{201} + 1/gm_{218}}, \tag{2}$$

$$V_{COMP} = V_{ref} - \frac{V_{ref}}{R_{201} + 1/gm_{218}} \times R_{201}, \tag{3}$$

To dependence between compensation voltage (V_{COMP}) and temperature (T) is defined as the partial derivative of Eqn. (3) [7].

$$\frac{\partial V_{COMP}}{\partial T} = A \cdot \frac{\partial 1/gm_{218}}{\partial T} + B \cdot \frac{\partial V_{ref}}{\partial T} - C \cdot \frac{\partial R_{201}}{\partial T}, \tag{4}$$

where

$$A = \frac{V_{ref} - R_{201}}{(R_{201} + 1/gm_{218})^2}$$

$$B = \frac{1/gm_{218}}{(R_{201} + 1/gm_{218})}$$

$$C = \frac{V_{ref}/gm_{218}}{(R_{201} + 1/gm_{218})^2} \tag{5}$$

Referring to Eqn. (4), the derivative of compensation voltage w.r.t. the temperature, namely sensitivity, is determined by (V_{ref}), the transconductance of M218 ($1/gm_{218}$) and resistor (R201). Notably, resistors can be made of several materials with different temperature coefficients on silicon such that the sensitivity is tunable. R201 is a polysilicon resistor with a resistivity, R_{poly}, modeled in Eqn. (6).

$$R_{poly}(T) = R_{poly}(T_0) \cdot (1 + TCR_{Poly} \cdot (T - T_0)), \tag{6}$$

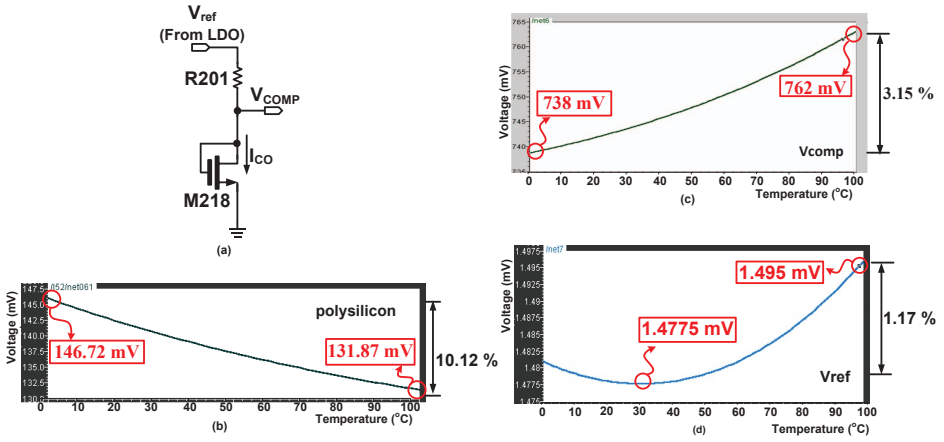

Fig. 5. Schematic of the (a) temperature compensation circuit; Voltage variation of (b) polysilicon resistor, (c)V_{COMP}, and V_{ref} (d) from LDO.

where T_0 indicates the room temperature, and TCR_{poly} is the temperature coefficient of the polysilicon resistor, which decreases with the rise of temperature. As a result, its partial derivative with respect to the temperature is negative ($\frac{\partial R_{poly}}{\partial T}$) as shown in Fig. 5 (b). By contrast, V_{comp} determined by $1/gm_{218}$ shows a positive temperature coefficient in Fig. 5 (c). Therefore, the overall temperature coefficient looking from V_{ref} into V_{comp} in Fig. 5 (a) will be nullified if the resistance of R201 and the aspect of M218 are properly tuned. By plugging the technology parameters into Eqn. (5), a simulation result is shown in Fig. 5 (d), where a stable voltage (V_{ref}) supplied from LDO is attained. The worst case is ($\cong 1.17\%$) at [1.495 mV, 100 ^{o}C]. To verify that the compensation voltage enables the oscillator to generate a stable frequency as shown in Fig. 1, the temperature coefficient of the voltage (TCV) of V_{comp} is derived based on Eqn (4).

$$TCV = \frac{1}{V_{COMP}}\frac{\partial V_{COMP}}{\partial T} = \frac{1}{V_{COMP}} \cdot \left[\left|\frac{\partial 1/gm_{218}}{\partial T}\right| \cdot A + \left|\frac{\partial V_{ref}}{\partial T}\right| \cdot B - \left|\frac{\partial R_{201}}{\partial T}\right| \cdot C\right], \quad (7)$$

Theoretically, if the output voltage is stable regardless of temperature variation, TCV should be 0 [7], which means a partial derivative with respect to temperature is 0 ($\frac{\partial V_{COMP}}{\partial T} = 0$). Notably, $\frac{\partial (V_{ref})}{\partial T}$ is tuned to close to 0 and ($\frac{\partial 1/gm_{218}}{\partial T}$) is positive. Therefore, the polynomial which it is multiplied with must be positive. According to Fig. 5 (a), though $\frac{\partial R_{201}}{\partial T}$ is negative, the negative sign therewith in Eqn. (7) can be used to eliminate the positive terms. By carefully adjusting these 3 terms, i.e., A, B and C, the variation of V_{comp} can be substantially minimized and close to nullity.

III. Implementation and Simulation Results

The proposed clock generator with temperature and process compensation was fabricated using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS process. Fig. 6 shows the layout of the proposed clock generator where the chip area is 0.693×0.693 mm^2 (with pad). Fig. 7 illustrates V_{ref}, provided that V_{DD} varies from 0 V to 2.4 V at different process corners. Fig. 8 presents the simulation waveforms of Vout at [TT, 25 ^{o}C] and the frequency is 50.05 MHz. To verify the stability of the proposed temperature compensation circuit, we disable the temperature compensation circuit and directly couple a DC voltage to Vcomp (Vcomp = 0.756 V) to compare the temperature drifting of compensated and uncompensated scenarios, as shown in Fig. 9. The variation is dropped from 8.32 % to 3.49 % when the proposed compensation circuit is enabled. Meanwhile, Fig. 10 shows the simulation results given different VDDs. The worst case frequency variation is 52.716 MHz given VDD = 1.98 V, which is 3.49 %. Table I shows a comparison of several recent works. The proposed design demonstrates the best performance with regard to frequency deviation. Besides, the proposed design attains the best Figure-of-merit (FOM), FOM = $\frac{\text{Power}}{\text{Frequency}}$, which is the average power divided by bandwidth.

IV. Conclusion

This paper proposes a clock generator with temperature and voltage compensation using the low dropout regulator and temperature compensation circuit. The frequency deviation is lower than 3.49 % for the worst case of [VDD= 1.98 V, 100 ^{o}C]. The proposed circuit can easily be integrated in low-power, high performance SoC applications.

TABLE I
Comparison with Several Prior Works

	This work	[5]	[6]
Process	0.18 μm CMOS	0.25 μm BCD	0.18 μm CMOS
Supply voltage (V)	1.8	2.5	1.8
Output frequency	50 MHz	2.0 MHz	130 MHz
Frequency error	±3.49 %	±2.10 %	±4.99 %
Temp. Range (^{o}C)	0∼100	0∼100	0∼100
Voltage Range (V)	1.62∼1.68	2.2∼2.5	N/A
Voltage error	±1.5 %	±10 %	±5.4%
Core Area (mm^2)	0.0309	0.076	0.0042
Power (mW)	18.40	1.28	61
Year	2013	2012	2010
FOM†	0.368	0.64	0.471

† FOM = $\frac{\text{Power}}{\text{Frequency}}$.

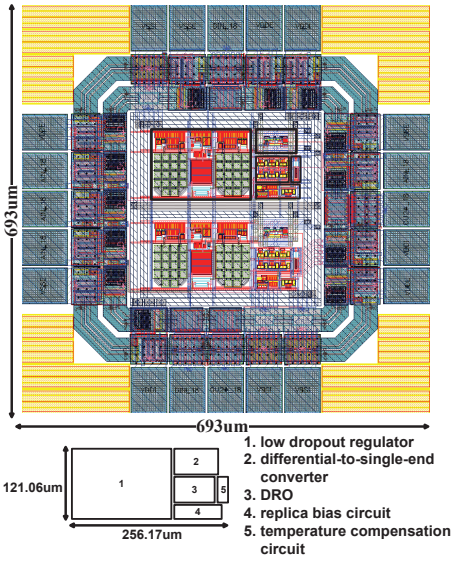

Fig. 6. Layout of the proposed clock generator.

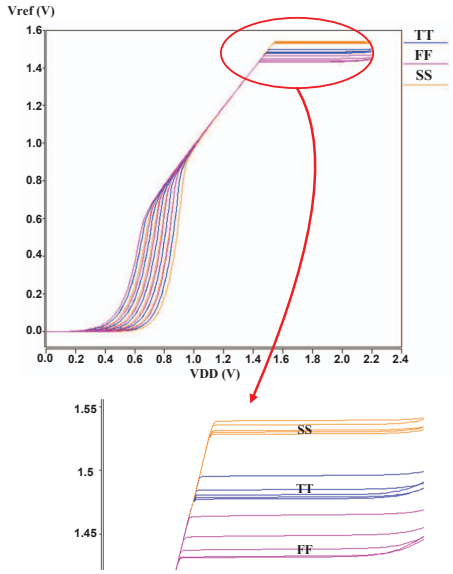

Fig. 7. Vref given different VDD from 0 V to 2.4 V.

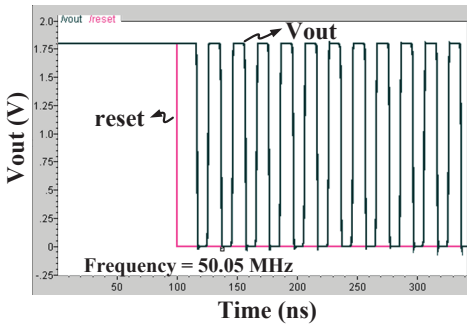

Fig. 8. Simulation waveforms of Vout at TT, 25°C.

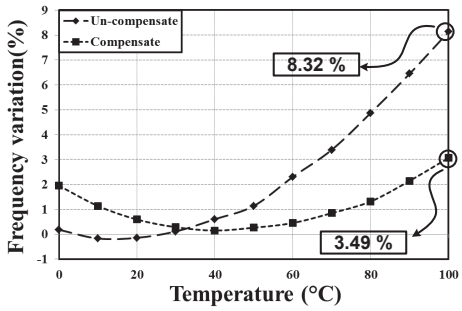

Fig. 9. Compensated and uncompensated output frequency error in TT corner.

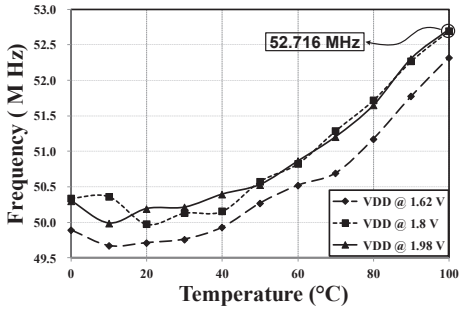

Fig. 10. Simulated of frequency in different supply voltage (VDD).

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