A 10-bit 400-MS/s Current-Steering DAC with Process Calibration

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***Abstract*—A 10-bit 400-MS/s current-steering DAC is proposed in this paper. A proposed process detector, and a current calibration circuit are used in the binary current cells to calibrate the current error due to the process variation. Besides, an auxiliary delay circuit is employed in the current cell to turn off the additional calibration current. The proposed DAC is implemented using a typical 0.18 μm 1P6M CMOS process. With the proposed process calibration circuit and delay compensation, the design complexity and core area is dramatically reduced. The core area is 0.29 $\times$ 0.20 mm^2. Besides, the worst DNL and INL of the DAC are simulated to be 0.18 LSB and 0.32 LSB, respectively. The power consumption is 3.7 mW.**

Keywords—current-steering, digital-to-analog converter, process calibration, nonlinearity

I. Introduction

DACs (Digital to analog converters) are commonly used in various communication systems [1]- [3], and readout systems [4]. Resolution, sampling rate, DNL (Differential nonlinearity), INL (Integral nonlinearity) and area are the important factors to choose an appropriate DAC for those applications. In a current-steering DAC, the output current of each current cell varies dramatically at different process corners. It causes poor DNL and INL performance for the current-steering DAC. In order to improve the DNL and INL for the current-steering DAC, A process independent current driver and an external resistor are utilized in several prior works [5]. However, the process independent current driver increases the design complexity and chip area. Moreover, the external resistor increases the system size. Thus, this paper proposes a 10-bit 400 MS/s DAC using a process detector, a current calibration circuit, and a delay circuit to calibrate the nonlinearity caused by the process variation. The DNL and INL are simulated to be 0.18 LSB and 0.32 LSB, respectively.

II. The proposed Current-Steering DAC

Fig. 1 (a) reveals the block diagram of the proposed current-steering DAC, which is composed of three current segments, LLSB Seg, ULSB Seg, MSB Seg and a Process detector. Referring to Fig. 1 (b), LLSB Seg is a 4-bit binary weighted segment composed of the current cells, DA1 $\sim$ DA4. Referring to Fig. 1 (c), ULSB Seg is a 3-bit binary weighted segment consisted of the current cells, DA5 $\sim$ DA7 with the current calibration circuit. MSB is a 3-bit unary weighted segment formed by the current cells, DA8 $\sim$ DA10 with the current calibration circuit. By using the binary weighted cells for the less significant bit segments, LLSB and ULSB Segs, the design area is miniaturized. Contrarily, the unary weighted segment is utilized for the more significant bit segment, MSB Seg, to improve the nonlinearity caused by the mismatch among the current cells. Besides, the ULSB and MSB Segs include the current calibration circuits to compensate the nonlinearity caused by the process variation. Furthermore, the Process detector generates 3-bit signals, p[2:0], to detect the process corners.

A. Nonlinearity Caused by Process Variation

Fig. 2 (a) shows the transfer curve of the current-steering DAC. With the increased digital input code, the analog output voltage increases linearly for the ideal case, as the gray line in Fig. 2. However, the output voltage increase slowly at the cycle 2^4 at the SS corner, as the black line for the real case in Fig. 2. It causes the nonlinearity of the current-steering DAC. Referring to Fig. 2 (b), when the digital input code increase linearly, the output voltages of the current cells, DA1 $\sim$ DA5, look like frequency divided period square functions, which consist of the increased analog output voltage of the DAC. At cycle 2^4, the rise of the output of the current cell DA5 slow down due to the SS corner. Thus, the summation of the output currents of DA1 $\sim$ DA5 induce the current error, resulted in the nonlinearity in Fig. 2 (a). This situation occurs easily at the switching of the most significant bits, i.e., bit 5 $\sim$ 10 in our case. In order to resolve this problem, a current calibration circuit is included in the current cells for ULSB and MSB Segs. The current calibration circuit provides the required additional current for the cycle 2^4, such that the current error at the cycle 2^4 is removed, as shown in Fig. 2 (c). However, at the next cycle, 2^4+1, the output of DA5 reaches its peak value and causes the current error due to the addition of the ideal output current of DA5 and the current calibration circuit, as shown in Fig. 2 (d). Thus, a delay circuit is included in ULSB and MSB Segs to generate a control signal, p[3], to remove the additional calibration current at cycle 2^4+1. Therefore, the nonlinearity due to the current calibration circuit is eliminated.

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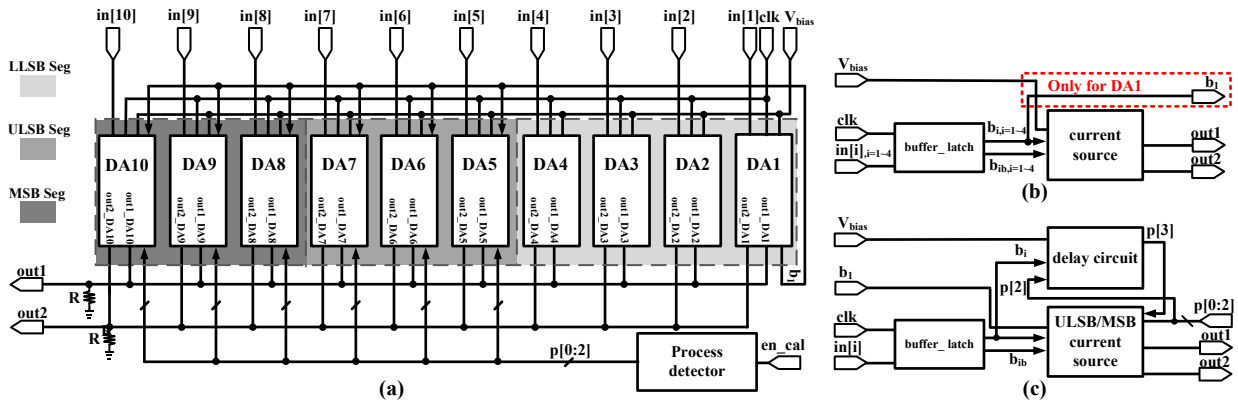

Fig. 1. Block diagram of (a) the proposed current-steering DAC, (b) the current cells, DA1 ∼ DA4, and (c) the current cells, DA5 ∼ DA10 (i = 5∼7/i = 8∼10 for ULSB/MSB Segs, respectively).

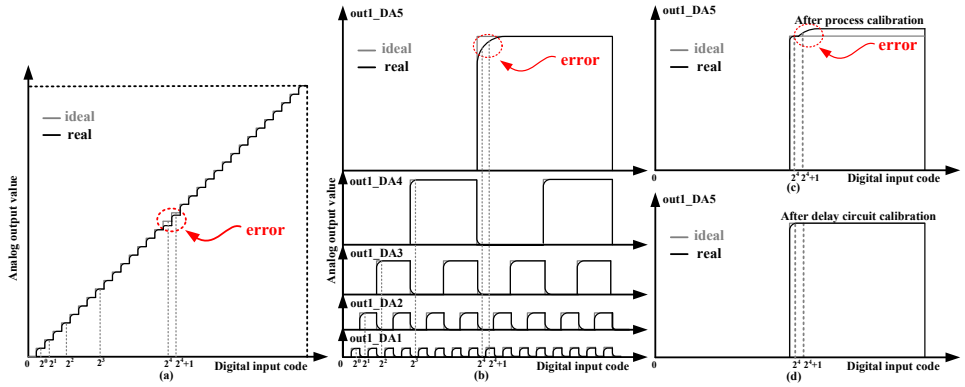

Fig. 2. Illustration error of analog output for individual bit

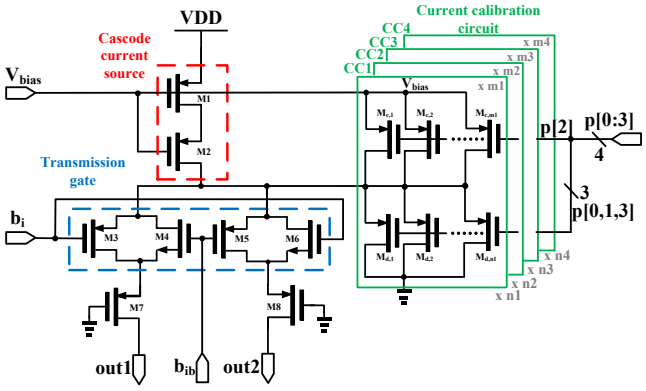

Fig. 3. Schematic of the current source with current calibration circuit

B. The Proposed Current Cells

Referring to Fig. 3, the MOS transistors, M1 ∼ M8 constitute the basic current cells for the LLSB, ULSB, and MSB Segs. M1 and M2 are the cascode current source, which receives the bias voltage, V_{bias}, and provides the output current with large output resistance. M3 ∼ M6 are two pairs of the transmission gates which are controlled by the input complementary signals, b_i and b_{ib}, for i = 1 ∼ 10. M7 and M8 are the always-turned-on transistors to remove the dynamic nonlinearity resulted from the binary switching. It also increases the output resistance for the differential output, out1 and out2.

As mentioned in the previous subsection, a current calibration circuit is included in ULSB and MSB Segs. $M_{c,1}$ ∼ $M_{c,m1}$ are the charging transistors to provide the additional compensation current for SS corner. $M_{d,1}$ ∼ $M_{d,n1}$ are the discharging transistors to sink the current from the output current for FF corner. CC1 ∼ CC4 are the four duplicates with various number of transistors to provide (or sink) different current for the current cell. The control signals, p[0] ∼ p[3], are generated by the Process detector and the delay circuit to determine the activation of the calibration current.

C. Process Detector

The Process detector consists of three duplicates of process sensors, PS1 ∼ PS3, and an encoder, as shown in Fig. 4 (a)

and (b). The process sensor is composed of a PMOS transistor, a pnp transistor, and a current comparator. With the process variation, the charging ability of the PMOS changed more severely than that of the pnp transistor. Thus, the process related current, $I_{sense} = I_{PMOS} - I_{pnp}$, is obtained. By tuning the aspect ratio of the PMOS transistors and β of the pnp transistor, the output of the current comparators, pin[0:2], become the thermometer code according to different process corners, as shown in Table I. The thermometer code, pin[0:2], is encoded to the one-shot code, p[0:2], by the encoder, as shown in Table I.

Fig. 4 (c) shows the schematic of the current comparator in the process sensor. M1 $\sim$ M4 operate the current comparison by the positive feedback inverter. With the input node biased at the source terminals of M1 and M2, the low input resistance is obtained. Besides, M5 and M6 are the output buffer to provide the driving ability.

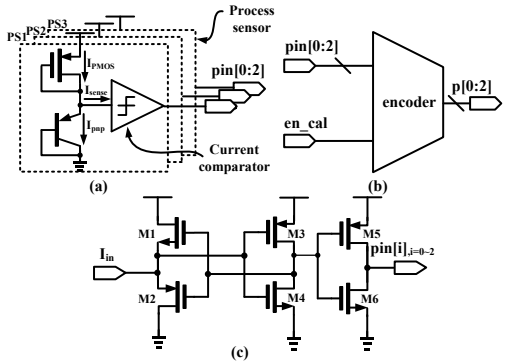

Fig. 4. Schematic of the process detector composed of (a) the current sensors, (b) the encoder and (c) the current comparator.

TABLE I
THE TRUTH TABLE FOR THE PROCESS DETECTOR

Process	pin[0]	pin[1]	pin[2]	p[0]	p[1]	p[2]
SS	1	0	0	1	1	0
TT	1	1	0	1	0	1
FF	1	1	1	0	1	1

D. Buffer Latch

The buffer latch is composed of 11 inverters, inv1 $\sim$ inv11, and 2 MOS transistors, M1 and M2. M1 and M2 are the switches triggered by the input clock signal, clk. The inverters, inv1 $\sim$ inv4 and inv11, generate the complementary signals for the output signals, b_i and b_{ib}. Notably, b_i is complementary to the input control signal, in[i]. Besides, b_i is low level activated to turn on the PMOS in the current calibration circuit. The inverters, inv9 $\sim$ inv10, constitute a simple latch to synchronize the complementary signals. The inverters, inv5 $\sim$ inv8, are the output buffer to provide the driving ability and reduce the output glitch.

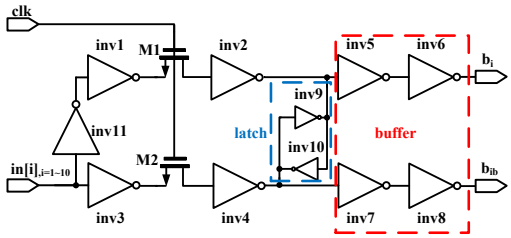

Fig. 5. Schematic of the buffer latch circuit.

E. Delay Circuit

The delay circuit is composed of a D Latch and a 3-input OR gate. The D Latch receives the LSB signal, b1, and the control signals, b_i, for i = 5 $\sim$ 10, respectively, and generates a output voltage for the OR gate. With the output OR gate, the output signal, p[3], is the low level activated signal to turn on the sink PMOS transistors in the current calibration circuit according to the control signals, b_i, b1 and p[2]. Notably, b_i is delayed for one cycle by the LSB, b1. Moreover, p[2] refers to the process corner.

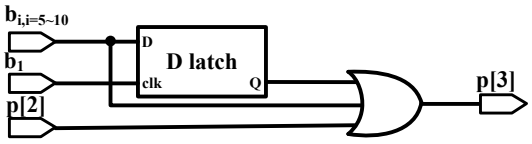

Fig. 6. Schematic of the delay circuit.

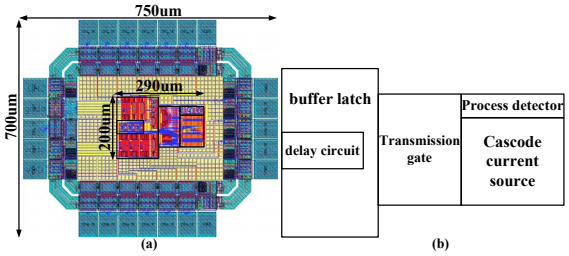

Fig. 7. Layout of the proposed current-steering DAC.

III. Implementation and Simulation Results

The proposed current-steering DAC is implemented using a typical 1P6M 0.18 μm CMOS process. With the proposed miniaturized calibration circuits, the core area is only 0.29 $\times$ 0.20 mm^2, as shown in Fig. 7. Fig. 8 (a) and (b) show the simulated DNL at the SS corner before and after calibration, respectively. The DNL is reduced from 2.04 LSB to 0.18 LSB by the process calibration. Fig. 9 (a) and (b) reveal the simulated INL at the SS corner before and after calibration, respectively. The worst case INL is reduced from -0.33 LSB to -0.32 LSB by the process calibration. Table II reveals the comparison of the specifications with that of several prior works.

A FOM (figure of merit) is given to show the performance among these works. With the given FOM, the proposed work possesses the best performance by considering the resolution, sample rate, power consumption and the normalized core area.

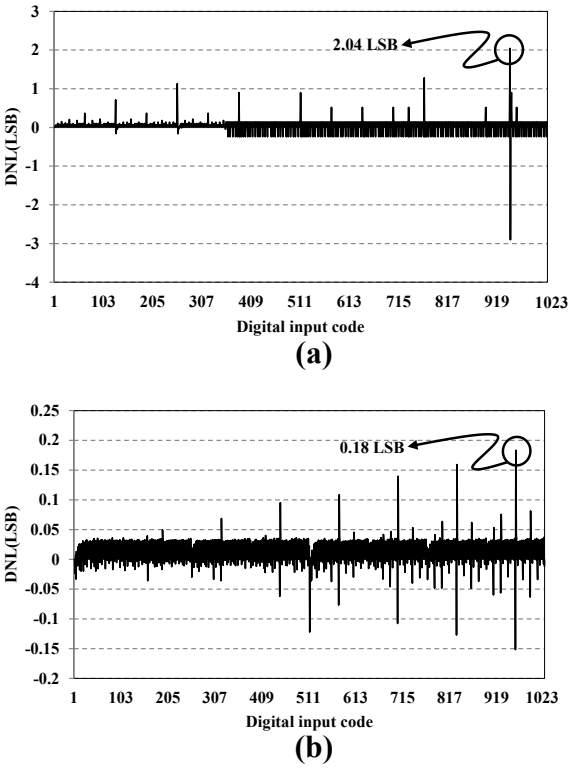

Fig. 8. Simulated DNL at the SS corner (a) before and (b) after calibration.

TABLE II
COMPARISON WITH SEVERAL PRIOR WORKS

	This work	[6]	[1]	[2]
Year	2013	2011	2008	2010
Process	0.18 μm	0.5 μm	65 nm	0.18 μm
Resolution(Bits)	10	8	10	10
Power supply (V)	1.8	5	2.5/1.2	1.8
Sample rate (MS/s)	400	200	300	200
Core area (mm^2)	0.058	0.282	0.1	0.2
$\|$DNL$\|$ (LSB)	0.18	0.16	0.23	0.07
$\|$INL$\|$ (LSB)	0.32	0.4	0.4	0.15
Power (mW)	3.7	113	6.24	65
FOM†	61.84	0.40	2.08	0.51

Note: † FOM = $\frac{2^N \times \text{Sample rate}}{\text{Power} \times \frac{\text{Core area}}{\text{Process}^2} \times 1000}$.

IV. CONCLUSION

This paper proposes a process calibrated current-steering DAC with 10-bit resolution and 400 MS/s sampling rate. Because of the proposed process detector, the current calibration circuit and the delay circuit, the DNL and INL are reduced to 0.18 LSB and 0.32 LSB, respectively, for the worst case. Besides, the calibration circuit is area-saving such that the core area is only 0.29 $\times$ 0.20 mm^2.

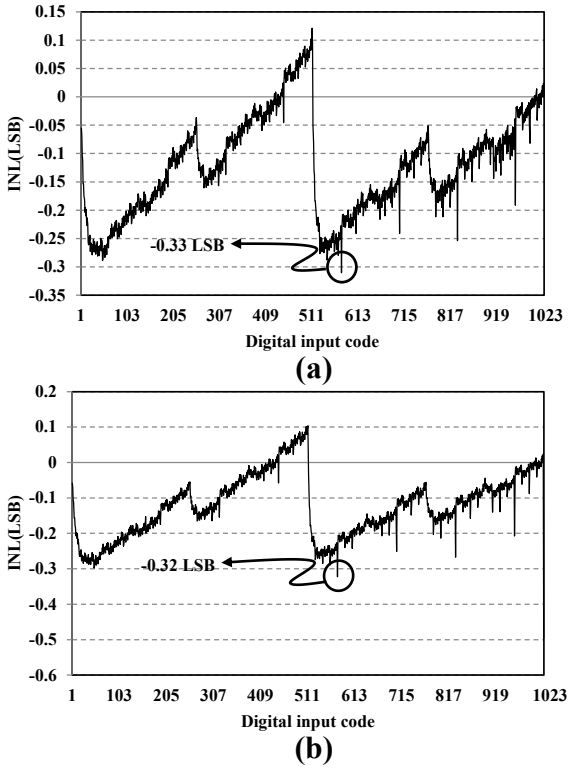

Fig. 9. Simulated INL at the SS corner (a) before and (b) after calibration.

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