High Voltage Operational Amplifier and High Voltage Transceiver Using 0.25 μm 60V BCD Process for Battery Management Systems

Chih-Lin Chen, Yi-Lun Wu, Chun-Ying Juan, and Chua-Chin Wang, *Senior Member, IEEE*

***Abstract*—This work presents a high voltage operational amplifier (HVOPA) and a high voltage transceiver (HVT) for Battery Management Systems (BMS). Battery Interconnect Modules (BIM) in BMS must be able to accommodate input voltage up to tens of volts, perhaps even hundreds of volts, which is difficult to be realized using a logic-based process. To realize a possible solution on silicon, BIM shall be fabricated using HV semiconductor processes, which usually are constrained by the voltage drop limitation between gate and source of HV devices. To overcome such a limitation, a HVOPA and a HVT are proposed in this work to carry out high voltage analog circuit design and data transmission. An experimental prototype is implemented using a typical 0.25 μm 1-poly 3-metal 60V BCD process. The post-layout-extracted simulation results proved the functional correctness of our proposed design.**

***Index Terms*—high voltage, operational amplifier, high voltage transceiver**

I. Introduction

High voltage (HV) Battery Management System (BMS) is widely needed in many applications, e.g., EV and HEV, where many Battery Modules are assembled and integrated, as shown in Fig. 1 [1]. These modules are composed of many battery strings to generate a high supply voltage. If Battery Module consists of series batteries, they will be unavoidably unbalanced among battery cells in voltage and capacity after a few times of charging and discharging cycles. Notably, the above hazard is always happened regardless that Battery Module is charging and discharging. If either over-charge or over-discharge occurs to any battery cell, the efficiency and health of the battery as well as the module will be degraded. What even worse is that the Li-ion battery might be burned out and exploded. Therefore, BMS with charge equalization is critically required in battery-operated applications.

A distributed BMS is composed of at least five blocks, including Battery Interconnect Modules (BIM), Main Controller, Analysis, Communication, and Logging & Telemetry, as shown in Fig. 1 [2], [3]. Notably, besides BIMs, the other 4 blocks are operated in low voltage (LV) domain. BIM is in charge of sensing the battery information, e.g., voltage, current, temperature, etc, and transmiting/receiving battery information between adjacent BIM by high voltage transceiver (HVT). Take a series of 8 batteries as an example. The highest voltage of Battery Module will reach 29.2 V (A Li-ion battery voltage is assumed to be 3.65 V). Therefore, HVT with HV tolerance is required in BIM to provide the communication capability between HV domain and LV domain.

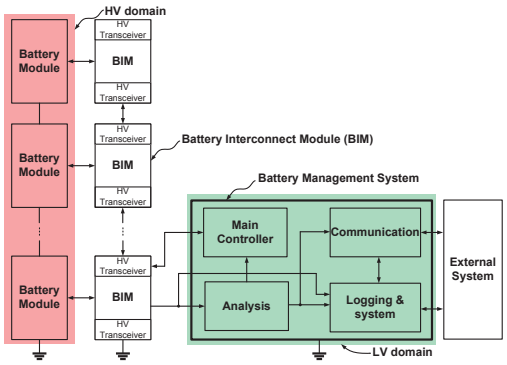

Fig. 1. The explosive view of a typical distributed Battery Management System (BMS).

Prior voltage measurement approaches are categorized into three types [1], as shown in Fig. 2. Referring to Fig. 2 (a), each battery cell is parallelly coupled to a corresponding ADC such that no HV multiplexer is needed. However, too many ADCs in such a scenario shall result in high power consumption and large area. Meanwhile, matching among ADCs is another problem. Fig. 2 (b) and (c) are more popular methods for BMS to save power and area, where Fig. 2 (c) is deemed as better solution using a differential approach to auto-cancelling the common noise. The multiplexer in Fig. 2 (c) is in charge of down-converting high voltage of each battery into the input range of HV Subtractor, which is composed of high voltage operational amplifier (HVOPA) and resistors. The bottom line of such a design is that the voltage distortion caused by the multiplexer and HV Subtractor must be as small as possible.

Several HVOPAs using multiple processes were reported

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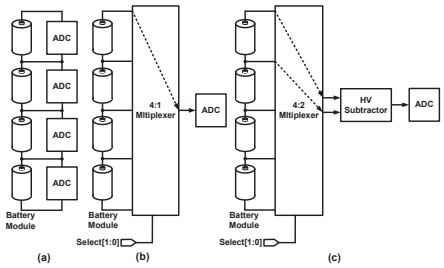

Fig. 2. Three prior architectures of voltage measurement.

[4]-[6]. A HV amplifier with complementary HV transistors was proposed using a 10-V trench-isolated CMOS process [4], where a parasitic field-oxide transistor is included. Due to the gain magnitude smaller than 30 dB, the gain error is very significant. A 36-V JFET-input bipolar OPA was implemented using a SOI SiGe bipolar process [5]. The power consumption is larger than 72 mW, and the cost of using the SOI process is more expensive than standard high voltage CMOS process. A single-ended HV amplifier was proposed using combination of different processes (BCD6/SOI) [6]. However, the input range is limited in low voltage such that it needs a resistive feedback network to provide a dc-stabilized voltage gain. Meanwhile, the output stage must provide a large quiescent current to drive the feedback resistors, which causes serious power dissipation.

Recently, many advanced semiconductor processes have been provided to fabricate HV devices on silicon, e.g., TSMC 0.25 μm 1-poly 3-metal 60V BCD process [2], [3]. For example, a low input-range HV amplifier was revealed using the mentioned process [7], where 0∼5 V digital signal could be amplified to 0∼60 V signal. This particular process offers digital cell library, including low voltage (LV) transistors driven by 2.5 V/5 V, and 60 V power MOS. The most critical limitation therewith is that the gate to source voltage of HV transistors must be limited under a low voltage $\approx$ 5 V. Therefore, the mentioned works are not easy to be directly implemented using this HV BCD process to be used in BIMs.

To resolve the above problems, novel HVT with HVOPA is disclosed in this paper. The proposed HVOPA design is equipped with wide input and output voltage range. Notably, the Vgs of all transistors is smaller than 5 V to comply with the voltage drop limitation. Besides, the proposed HV transceiver can receive digital signals with different dc level (0∼30 V), and then transmit them to either low voltage domain (0∼2.5 V) or high voltage domain (27.5∼30 V).

II. The Architecture of The Proposed HVT and HVOPA Designs

Referring to Fig. 1, a Battery Interconnect Modules (BIM) is proposed in this paper, including Battery Monitor, Regulator, multiplexers (MUX1 and MUX2), High Voltage Transceivers (HVT), as shown in Fig. 3. Battery Monitor is in charge of reading battery information, e.g., voltage, current, and temperature. Battery Monitor is composed of HVMUX and HV Subtractor, where HVMUX is a multiplexer with high voltage tolerant. HVMUX selects a pair of top voltage and bottom voltage of each battery into HV Subtractor consisting of HVOPA and resistors. Therefore, HV Subtractor derives the difference, which is the voltage information, into ADC to convert the voltage information into digital code. Regulator supplies stable voltages to every block. The multiplexers are driven to select the direction of the data flow. HVTs are responsible for delivering battery information among adjacent BIMs. Notably, the output voltage of an upper BIM is high voltage such that HVT must be able to receive data from high voltage domain, and then convert them into low voltage domain. On the other hand, HVT is also needed to transmit data to the upper BIM in high voltage domain.

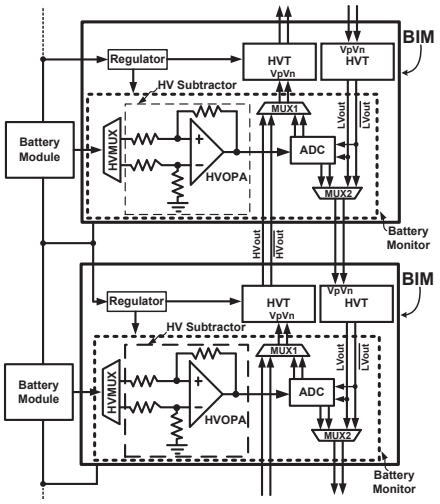

Fig. 3. The architecture of Battery Interconnect Modules

A. HV Transceiver

The HVT is composed of 4 amplifiers, i.e., A11, A12, A21, and A22, as shown in Fig. 4. Each amplifier is described in Table I. Firstly, A11 and A12 are in charge of converting GND∼VDD signals into GND∼5 V and VDD-5V∼VDD signals, respectively, to ensure Vgs <5 V and prevent over-voltage problem, because the input range of A21 and A22 must be smaller than GND∼5 V and VDD-5V∼VDD, respectively. Notably, the LVout and HVout are converted signals to transmit in low voltage domain and high voltage domain, respectively.

TABLE I
Description of each stage in HVT

A11	N-type input stage
A12	P-type input stage
A21	Low level gain stage
A22	High level gain stage

Fig. 5 shows the schematic of the proposed HVT. The P-type input stage and N-type input stage are realized using classical common source amplifiers, consisting of HV transistors, resistors, and zener diodes. The zener diodes limit the Vgs

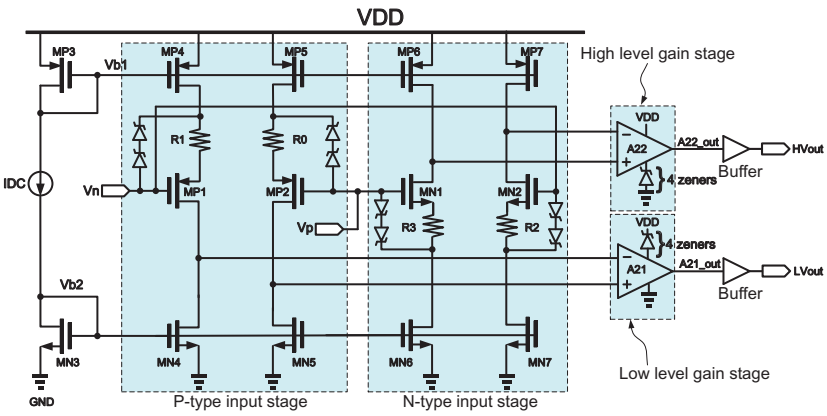

Fig. 5. HVT schematic.

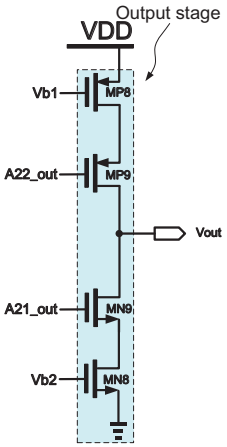

Fig. 6. The Output stage of HVOPA schematic.

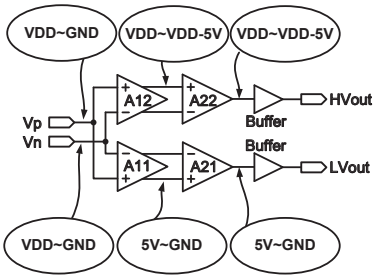

Fig. 4. The architecture of the proposed HVT.

of the transistors (MP1, Mp2, MN1, and MN2) to be smaller than 5 V. Besides, the resistors (R0 to R3) are meant to adjust the offset voltage. Finally, the small signal analysis of P-type input stage is defined in Eqn. (1)-(2), while the analysis of N-type input stage is similar.

$$\omega_{z1} = \frac{1}{\mathrm{ro}_{\mathrm{MP1}} \times \mathrm{Cgd}_{\mathrm{MP1}}} \tag{1}$$

$$\omega_{p1} = \frac{\mathrm{ro}_{\mathrm{MN4}} || \mathrm{ro}_{\mathrm{MP1}}}{\mathrm{Ctot1} \times \mathrm{Cgd}_{\mathrm{MP1}}} \tag{2}$$

where $\mathrm{ro}_{\mathrm{MP1}}$ is the output resistance of MP1, $\mathrm{Cgd}_{\mathrm{MP1}}$ is the capacitor between gate and drain of MP1, and Ctot1 is the overall output capacitance of P-type input stage.

High level gain stage and Low level gain stage are implemented using traditional differential amplifiers. Besides, the supply voltage of Low level gain stage is coupled via 4 zener diodes with VDD. To fine tune the current of amplifier and numbers of zener diodes, the supply voltage of Low level gain stage could be close to 5 V. On the contrary, the ground voltage of High level gain stage is coupled via 4 zener diodes with GND such that the ground voltage is close to VDD-5V. Over-voltage problem is then prevented. The small signal analysis of Low level gain stage is defined in Eqn. (3), while the analysis of High level gain stage is similar.

$$\omega_{p2} = \frac{1}{\mathrm{Rtot2} \times \mathrm{Ctot2}} \tag{3}$$

where Rtot2 and Ctot2 are the overall output resistance and capacitance of Low level gain stage, respectively.

Finally, the output of A21 and A22 is coupled with two Buffers to supply large currents for LVout and HVout, respectively. Notably, the supply voltage of Buffers is the same as that of digital circuits in low voltage domain or high voltage domain. Therefore, HVT can receive digital signals with different dc levels, and then convert them into low voltage domain or high voltage domain. Notably, LVout is used to transmit data to lower BIM in a BMS. By contrast, HVout is coupled with an upper BIM.

B. HV Operational Amplifier

Referring to Fig. 3, a high voltage operational amplifier (HVOPA) is proposed to realize the HV Subtractor in a BIM. The HVOPA is composed of HVT and Output stage, which is shown in Fig. 6. The Output stage is realized using a class-AB amplifier, consisting of MP8, MP9, MN8, and MN9. The outputs of A21 and A22, A21_out and A22_out, are coupled with Output stage. Therefore, the Output stage magnifies the different between A21_out and A22_out. For the sake of protecting HV transistors, the foundry strongly recommends that the slew rate must be limited. The current mirrors, i.e., MP8 and MN8, clamp the maximum output current for such a slew rate requirement. Notably, the output impedance can be enhanced to provide high gain. Finally, the small signal analysis of Output stage is defined in Eqn. (4).

$$\omega_{p3} = \frac{1}{\mathrm{Rtot3} \times \mathrm{Ctot3}} \tag{4}$$

where $\mathrm{Rtot3} \approx (\mathrm{gm}_{\mathrm{MN9}} \times \mathrm{ro}_{\mathrm{MN9}} \times \mathrm{ro}_{\mathrm{MN8}}) || (\mathrm{gm}_{\mathrm{MP9}} \times \mathrm{ro}_{\mathrm{MP9}} \times \mathrm{ro}_{\mathrm{MP8}})$, $\mathrm{gm}_{\mathrm{MX}}$ is the transconductance of MX, $\mathrm{ro}_{\mathrm{MX}}$ is the output resistance of MX, and Ctot3 is the overall output capacitance of Output stage.

III. Implementation and Simulation

The proposed designs are implemented using the 0.25μm 1-poly 3-metal 60V BCD process to justify the performance. Fig. 7 shows the layout of the proposed designs. The chip area is 1.18×1.9 mm^2, where the active areas are 0.339×0.667 mm^2 for HVT and 0.303×0.809 mm^2 for HVOPA, respectively. Fig. 8 shows the simulation results of HVT given digital signals with different dc levels, which is sweeping from 0 to 30 V. Notably, Vn is the inverted signal of Vp. The fastest data rate is 2 Mbps. The proposed HVT can receive any digital signals between 0 and 30 V, and then transmit them to high voltage domain or low voltage domain via HVout or LVout. The gain-bandwidth and phase margin (PM) of HVOPA is 0.443 MHz and 89.75 degrees, respectively, proven in Fig. 9. Table II shows the comparison between the proposed HVOPA design and prior works. Our proposed design attains the smallest power dissipation and wide input/output range compared with [6] and [7].

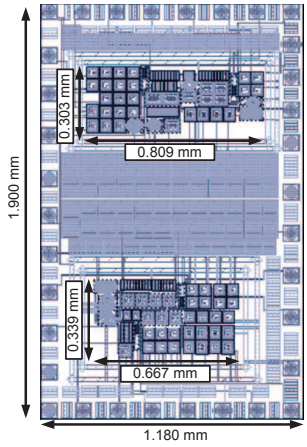

Fig. 7. The layout of the proposed designs.

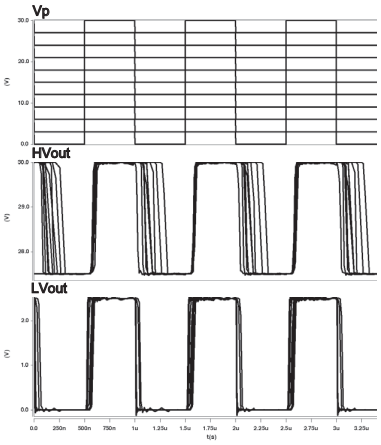

Fig. 8. The simulation results of the proposed HVT given digital signals with different dc levels.

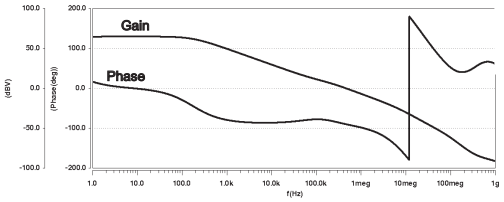

Fig. 9. The Bode plot of the proposed HVOPA.

TABLE II
Comparison between the proposed design and prior works

	This work	[5]	[6]	[7]
Year	2013	2011	2012	2011
Process	0.25μm BCD	SOI SiGe bipolar	BCD6 SOI	0.25μm BCD
DC Gain (dB)	64.6	N/A	40.9	133
PM(°)	89.75	N/A	N/A	85
GBW (MHz)	0.443	11	6.5	2.6
PSRR (dB)	106.9	140	N/A	N/A
CMRR (dB)	55.78	140	N/A	N/A
SR(V/μs)	7.18	20	1800	3.6
Offset (mV)	6.8	0.12	N/A	N/A
Avg. Power (mW)	24.74	72	37	127.7
ICMR (V)	3∼27	36	±3.5	0∼5
Output swing (V)	0∼29.6	N/A	±90	0 or 60

IV. Conclusion

In this paper, we propose a HVOPA and a HVT to realize the HV Subtractor and data transmission between high voltage domain and low voltage domain. The proposed design is implemented using a typical 0.25μm 1-poly 3-metal 60V BCD process such that is can be easily integrated in a possible SOC (system-on-chip) solution for high voltage BMS. The simulation results justify our design to be a high voltage operational amplifier and transceiver without using expensive SOI process. Notably, our design attains low power dissipation compared with the prior works.

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