A Battery Interconnect Module with High Voltage Transceiver Using 0.25 μm 60V BCD Process for Battery Management Systems

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***Abstract*—This work presents a Battery Interconnect Module (BIM) with high voltage (HV) transceiver for Battery Management Systems (BMS). BIM in BMS must be able to accommodate input voltage up to tens of volts, perhaps even hundreds of volts, which is difficult to be realized using a logic-based solution. To realize a possible solution on silicon, BIM shall be fabricated using an advanced HV semiconductor process, which usually is constrained by the voltage drop limitation between gate and source of HV devices. To overcome such a limitation, a HV switch is proposed in this work, including a HV Gate Voltage Driver (HVGVD) driving the HV MOS without any over-voltage hazard. An experimental prototype is implemented using a typical 0.25 μm 1-poly 3-metal 60V BCD process. The post-layout-extracted simulation results reveal that the worst-case error is less than 9 mV and the isolation between adjcent channels is -157 dB@10 MHz.**

***Index Terms*—high voltage, analog multiplexer, Battery Management System, high voltage transceiver**

I. Introduction

High voltage (HV) Battery Management System (BMS) is widely needed in many applications, e.g., EV and HEV, where many Battery Modules are assembled and integrated, as shown in Fig. 1 [1]. These modules are composed of many series of batteries to generate a high supply voltage. If the Battery Module is made of series batteries, they will be unavoidably unbalanced among battery cells in voltage and capacity after a few times of charging and discharging cycles. Notably, the above hazard is always happened regardless that the Battery Module is charging and discharging. If either over-charge or over-discharge occurs to any battery cell, the efficiency and health of the battery as well as the module will be degraded. What even worse is that the Li-ion battery might be burned out and exploded. Therefore, BMS with charge equalization is critically required in battery-operated applications.

A distributed BMS is composed of at least five blocks, including Battery Interconnect Modules (BIM), Main Controller, Analysis, Communication, and Logging & Telemetry, as shown in Fig. 1. Notably, besides BIMs, the other 4 blocks are operated in low voltage (LV) domain. BIM is in charge of sensing the battery information, e.g., voltage, current, temperature, etc. Take a series of 8 batteries as an example. The highest voltage of Battery Module will reach 29.2 V (A Li-ion battery voltage is assumed to be 3.65 V). Therefore, HV transceivers with HV tolerance are required in BIM to provide the communication capability between HV domain and LV domain.

Prior voltage measurement approaches are categorized into three types [1], as shown in Fig. 2. Referring to Fig. 2 (a), each battery cell is parallelly coupled to a corresponding ADC such that no HV multiplexer is needed. However, too many ADCs in such a scenario shall result in high power consumption and large area. Meanwhile, matching among ADCs is another problem. Fig. 2 (b) and (c) are more popular methods for BMS to save power and area. The multiplexer is in charge of converting high voltage of each battery into the input range of the sole ADC. The critical thing is that the voltage distortion caused by the multiplexer must be as small as possible.

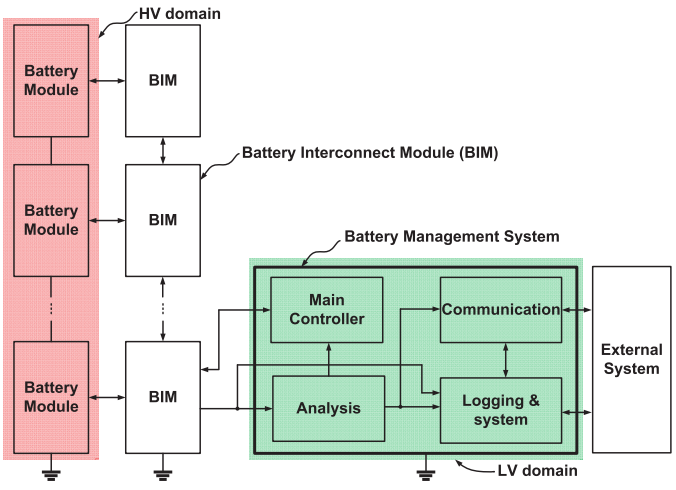

Fig. 1. The explosive view of a typical distributed Battery Management System (BMS).

Several HV multiplexers using multi-process technique have been reported [2]-[3]. An 8-channel HV multiplexer was

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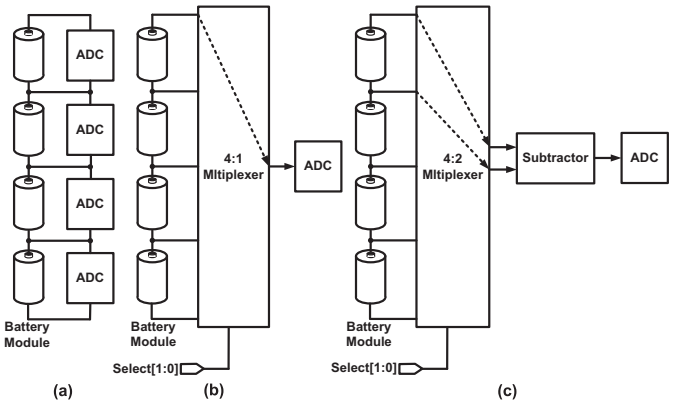

Fig. 2. Three architectures of voltage measurement methods.

proposed using both junction-isolated (JI) and dielectrically isolated (DI) D/CMOS process technologies [2], including a HV level-shift circuit to drive a switching MOS. A 16:1 analog multiplexer was revealed using a combination of process (CMOS/SOI) techniques [3], where 5 V CMOS logic circuits are shifted up to ±15 V to drive HV analog switches. HV drivers and analog switches are also widely used in LCDs, imaging system, and one-time programmable (OTP) memory [4]-[7].

Recently, many advanced semiconductor processes have been provided to fabricate HV devices on silicon, e.g., TSMC 0.25 μm 1-poly 3-metal 60V BCD process [8]. This particular process offers digital cell library, low voltage (LV) MOSs driven by 2.5 V/5 V, and 60 V power MOS. The most critical limitation is that the gate to source voltage of the HV MOS must be limited under a low voltage ≈ 5 V. Therefore, those mentioned prior works are not easy to be directly implemented using this HV BCD process.

To resolve the above problem, a novel HV analog multiplexer with digital calibration is disclosed in this paper. The proposed design converts the voltage drop of every battery in the same string into a low voltage level between 1.9 V and 3.7 V, which is the input range of an ADC. Therefore, the proposed design can be accommodated in BIM.

II. The Architecture of the Proposed Design

Battery Interconnect Module (BIM) is composed of an 8:1 HV analog multiplexer (HVMUX), a HV Transceiver, and a 3rd order Σ-Δ ADC, as shown in Fig. 3. The HVMUX selects a pair of input voltages, namely V_{bat_inX}, X=0, 2,$\cdots$8, and passes to the 3rd order Σ-Δ ADC, namely ADC_in. The HV Transceiver is in charge of communicating about battery information among adjacent BIMs. The 3rd order Σ-Δ ADC converts ADC_in into digital codes, ADCOUT[13:0]. Switch[2:0] selects one battery in Battery Module to be sensed. Enable is used to turn on or off the HVMUX for saving power.

The proposed HVMUX is shown in Fig. 4, including HV switches, HV subtractors & divider, LV multiplexer, LV multiplier. Notably, the Decoder in Fig. 3 converts Switch[2:0] into HV_S[0]∼HV_S[8] and LV_S[0]∼LV_S[1] to drive the

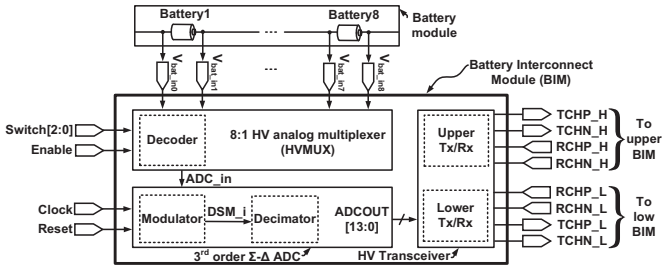

Fig. 3. Block diagrams of Battery Interconnect Module (BIM).

HV switches and LV Multiplexer, respectively. The function description of each block of HVMUX is given in the following text.

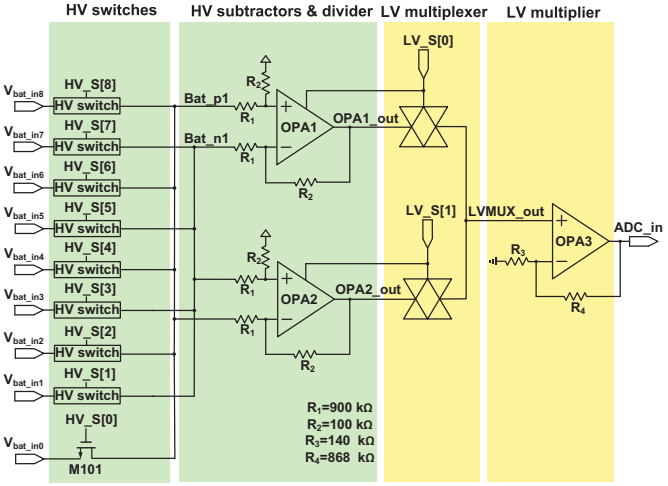

Fig. 4. Schematic of 8:1 HV analog multiplexer (HVMUX).

A. HV switches

The HV switches are composed of eight HV switch cells, where each HV switch cell comprises M201, M202, Buck Converter, HV Gate Voltage Driver (HVGVD), and an inverter, as shown in Fig. 5. M201 and M202 are HV devices. Notably, Vgs of the HV devices must be smaller than 5 V. In other words, the voltage difference between V_X and V_{gate} must be smaller than 5 V. When V_{gate} is equal to V_X, M201 and M202 are turned off. By contrast, when V_{gate} is equal to '$V_X - 5V$', M201 and M202 are turned on. The Buck Converter is used to generate '$V_X - 5V$', namely V_{X-5}. Referring to Fig. 5, the HV switch is driven by HV_S[i], i=1∼8, which chooses '$V_{gate} = V_X$' or '$V_{gate} = V_{X-5}$' by HVGVD. Therefore, M201 and M202 are ensured without any over-voltage hazard.

B. HV Gate Voltage Driver (HVGVD)

Fig. 6 shows the schematic of HV Gate Voltage Driver (HVGVD), including two resistors, M301, M302, seven diodes, which are all HV devices. The Vgs of M302 is driven by HV_S[i], i=1∼8, which is a digital signal with a swing 0 to 2.5 V. Therefore, M302 is ensured without any over-voltage hazard. To prevent the over-voltage damage of M301,

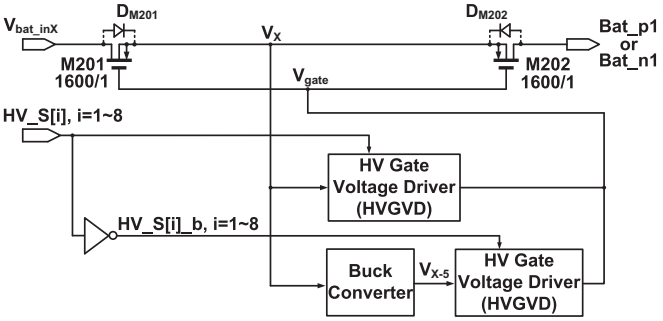

Fig. 5. Schematic of HV Switches.

the seven diodes is used to clamp the Vgs of M301 under 5 V. Notably, When V_X is smaller than 5 V, the gate voltage of M301 is generated by the two same resistors, R_a. For instance, if HV_S[i] is logic '1', V_a is half of V_X to turn on M301.

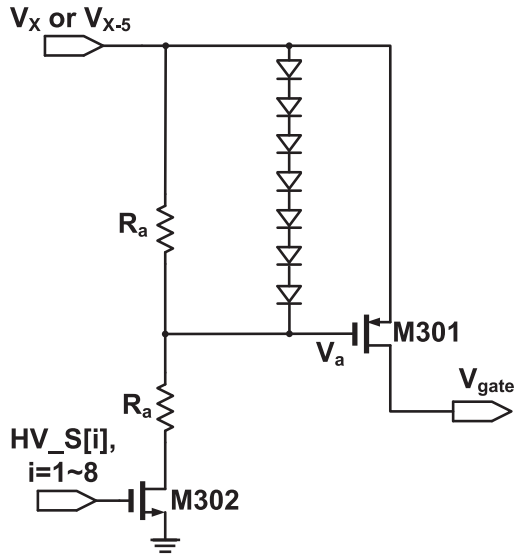

Fig. 6. Schematic of HV Gate Voltage Driver (HVGVD).

C. Buck Converter

Buck Converter is composed of a current source, I_{bias}, two current mirrors, M601∼M604, and a load resistor, R601, as shown in Fig. 7. Current source, I_{bias}, and M601 and M602 are LV devices. M603, M604, and R601 are HV devices. The Buck Converter generates '$V_X - 5V$', namely 'V_{X-5}', where V_{X-5} can be constrained by the following equation:

$$V_{X-5} = V_X - R601 \times I_3 \quad (1)$$

where I_3 is the current through R601. Assume the voltage difference between V_X and V_{X-5} is equal to 5 V, R601 can be written as

$$R601 = \frac{5}{I_3} = \frac{5}{I_1 + I_2} \quad (2)$$

where I_1 is the drain current of M604, which is supplied by the I_{bias}, I_2 is the input current of HVGVD. Referring to Fig. 6, I_2 can be derived as

$$I_2 = \frac{V_X}{2 \times R_a + Ro_{M302}} \quad (3)$$

where Ro_{M302} is the output resistor of M302. Substituting Eqn. (3) into Eqn. (2), R601 can be found as

$$R601 = \frac{5}{I_1 + \frac{V_X}{2 \times R_a + Ro_{M302}}} \quad (4)$$

Eqn. (4) shows how to calculate the device parameter of R601, where I_1, R_a, and Ro_{M302} can be determined based on the limitation of power dissipation. For instance, low I_1 and high R_a shall reduce dc current to save power.

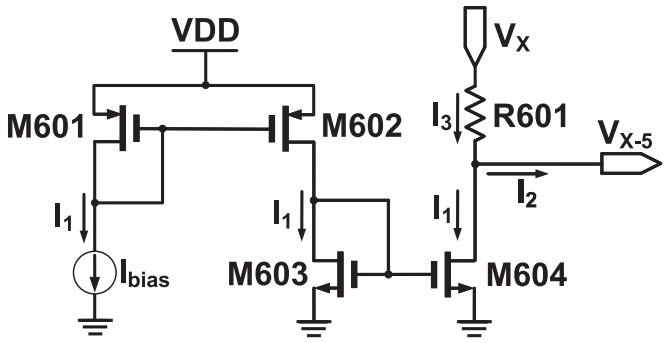

Fig. 7. Schematic of Buck Converter.

D. LV multiplexer & multiplier

LV multiplexer in Fig. 4 is composed of 2 transmission gates, which are respectively driven by LV_S[0] and LV_S[1]. LV multiplexer selects one of OPA1_out or OPA2_out to be LVMUX_out.

LV multiplier multiplies the voltage at LVMUX_out with R_4/R_3 to generate a corresponding ADC_in for the following 3^{rd} order Σ-Δ ADC.

$$ADC\_in = (1 + \frac{R_4}{R_3}) \times LVMUX\_out \quad (5)$$

where R_4 and R_3 are used to adjust the LVMUX_out into the voltage range of ADC, and LVMUX_out is the output voltage of LV multiplexer.

III. Implementation and Simulation

The proposed design is implemented using the 0.25 μm 1-poly 3-metal 60V BCD process to justify the performance. Fig. 8 shows the layout the proposed design. The chip area is 3.239 $\times$ 2.467 mm^2, where the core area is 2.619 $\times$ 1.757 mm^2. Fig. 9 shows the error distribution with calibration given 3 different battery voltages, namely Vbattery, which are the lower bound, typical, and upper bound voltage of a Li-ion battery. Table I shows the comparison of the proposed design with several prior works. Our design attains the smallest power dissipation and the best isolation, -157 dB@10 MHz.

TABLE I
COMPARISON BETWEEN THE PROPOSED DESIGN AND PRIOR WORKS

	This work	[5]	[3]	[7]	[8]
Year	2012	2005	2008	2011	2012
Process (μm)	0.25 μm 60 V BCD	0.35 μm SOI	30 V CMOS/SOI	0.35 μm 50 V	0.25 μm 60 V BCD
Number of switches	8	32×32	16	4	8
Analog input range	2.5∼29.2 V	-40∼40 V	-5∼25 V	0∼40 V	2∼29.2 V
On resistance	30 Ω	N/A	<1500 Ω	26 Ω	16.8 Ω
Isolation	-157 dB@10 MHz	-53 dB@4 MHz	-45 dB@0.2 MHz	-90dB@10 MHz	-79.4 dB@10 MHz
Power dissipation	14.24 mW (only HVMUX)	10 mW/switch	<15 mW	N/A	17.79 mW

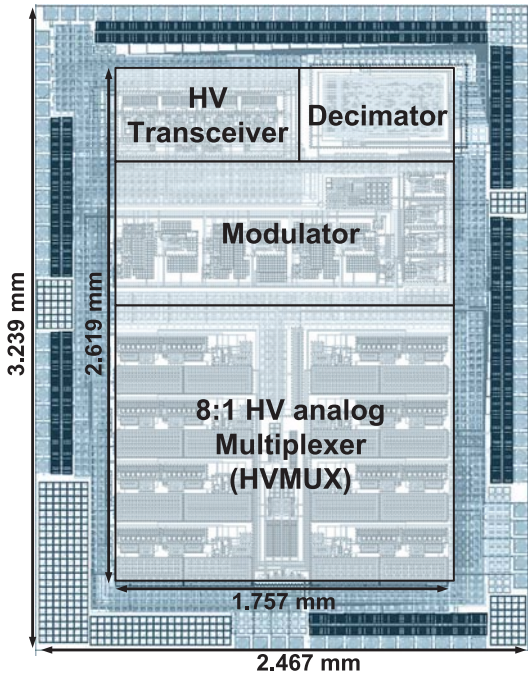

Fig. 8. The layout of the proposed design.

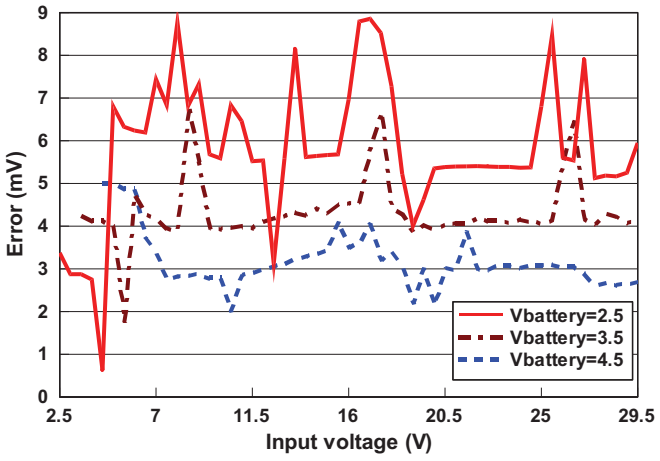

Fig. 9. Error distribution given 3 different battery voltages (Vbattery).

IV. CONCLUSION

In this paper, we propose a total solution for BIM. The proposed design is implemented using a typical 0.25 μm 1-poly 3-metal 60V BCD process such that it can be easily integrated in a possible SOC (system-on-chip) solution for high voltage BMS. The simulation results justify our design to be a multi-channel HV analog multiplexer with HV transceiver. Finally, the error of the proposed design is smaller than 9 mV from 2.5 V to 29.5 V, as shown in Fig. 9.

V. ACKNOWLEDGEMENT

This investigation was partially supported by Metal Industries Research Development Centre (MIRDC) and Ministry of Economic Affairs, Taiwan, under grant 100-EC-17-A-01-1010, 99-EC-17-A-01-S1-104, and 99-EC-17-A-19-S1-133. It was also partially supported by National Science Council, Taiwan, under grant NSC99-2221-E-110-082-MY3, NSC99-2923-E-110-002-MY2, NSC-99-2221-E-110-081-MY3, NSC-99-2220-E-110-001. This research was partially supported by the Southern Taiwan Science Park Administration (STSPA), Taiwan, R.O.C. under contract no. EZ-10-09-44-98. The authors would like to express their deepest gratefulness to CIC (Chip Implementation Center) of NARL (Nation Applied Research Laboratories), Taiwan, for their thoughtful chip fabrication service.

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