On-Chip MOS PVT Variation Monitor for Slew Rate Self-Adjusting 2×VDD Output Buffers

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***Abstract*—A novel PVT (Process, Voltage, Temperature) detection and compensation technique is proposed to automatically adjust the slew rate of a 2×VDD output buffer. The threshold voltage (Vth) of PMOSs and NMOSs varying with process, voltage, and temperature deviation could be detected, respectively. The proposed design is implemented using a typical 90 nm CMOS process to justify the performance. By adjusting output currents, the slew rate of output signal could be compensated over 26% and the maximum data rate is 330 MHz.**

***Index Terms*—PVT variation, threshold voltage detection, mixed-voltage tolerant, I/O buffer, floating N-well circuit, gate-oxide reliability**

I. Introduction

THE sensitivity of modern VLSI circuits to the process, voltage, and temperature (PVT) variation severely degrades performance and yield, especially when the technology is evolved toward nano-scale. The performance of VLSI circuits on silicon can be interpreted as a function of PVT variation, as shown in Fig. 1 [1]. Lately, many prior works have proposed different techniques to enhance the capability against PVT variation and enlarge the acceptable envelop as much as possible to increase the yield. Though the logic delay method has been widely utilized to detect PVT variation [2]-[7], it can only recognize three corners, TT, FF, and SS. Therefore, from a perspective view of transistor level, a novel corner detection technique is needed to detect all process corners, i.e., TT, FF, SS, SF, and FS. That is, the process variation of PMOS and NMOS should be examined, respectively.

In past several years, many mixed-voltage I/O buffers were reported to deal with the chip interface problems of different voltage levels [8]. However, the transmitting and receiving frequency of most previous works are not high enough to meet certain required specification, e.g., PCI-express, which is up to 266 MHz. Therefore, a wide range I/O buffer able to simultaneously transmit and receive signal from VDD to 2×VDD is deemed as a total solution for these scenarios. To communicate the signal with 2×VDD swing, double stacked transistors are used in the output stage to avoid the gate-oxide overstress. Moreover, for the high-speed interface circuits, the specification of slew rate is definitely required by communication system protocols. Hence, a compensation mechanism integrated with the NMOS and PMOS process corner detectors is needed to self-adjust the slew rate of output buffers, as shown in Fig. 2.

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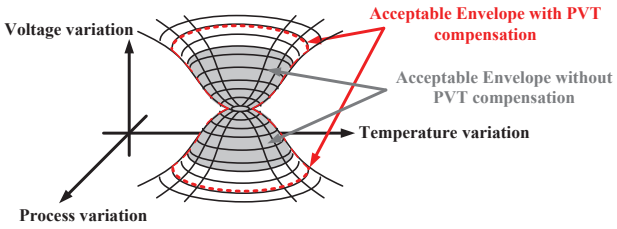

Fig. 1. Performance envelop as a function of process and temperature varitaion.

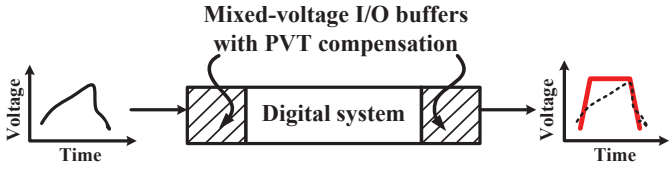

Fig. 2. The slew rate is compensated through our system

II. 2×VDD Output Buffer with PVT Compensation

Fig. 3 shows the block diagram of the proposed buffer design for mixed-voltage circuits. The proposed design is composed of PVT sensors, PVT decider, and a 2×VDD output buffer. The PVT sensors consist of PMOS Process sensor, NMOS Process sensor, and Voltage & Temperature sensor. Notably, the PVT decider comprises three comparators, a V_{Bias} generator, and a Digital circuit.

A. PMOS Process sensor

Fig. 4 shows the schematic of a PMOS process sensor. The PMOS process sensor comprises 2 cascaded PMOS source followers, which are composed of MP901 ∼ MP904. In the first cycle, if reset is activated, then V_vthp1 is pulled high to VDD (=1.2 V). In the second cycle, when reset is pulled low, V_vthp1 is discharged till Vthp, which is the threshold voltage of MP901. By a similarly operation, pout will be discharged till 2×Vthp in the second cycle. In other words, the variation of PMOS threshold voltage is "magnified" twice at the output, pout. Finally, the voltage of pout is transmitted to the following PVT decider to detect the PMOS corner.

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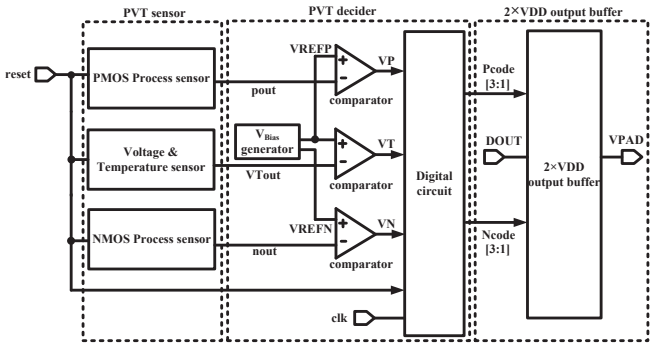

Fig. 3. The block diagram of the proposed output buffer

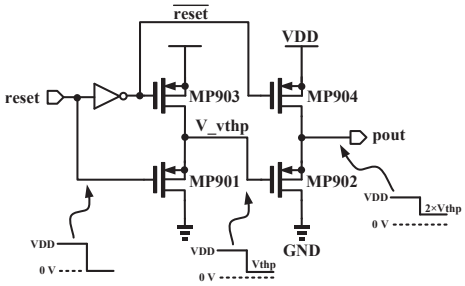

Fig. 4. Schematic of PMOS process sensor

B. NMOS Process sensor

Fig. 5 shows the schematic of an NMOS process sensor. Similarly, the NMOS process sensor also uses 2 cascaded NMOS source followers, which are composed of MN901 $\sim$ MN904, to detect the NMOS threshold voltage deviation. In the first cycle, when reset is activated, V_vthn is pulled low to GND (= 0V). In the second cycle, after reset is pulled low, V_vthn is charged till VDD-Vthn, where Vthn is the threshold voltage of MN904. By a similarly operation, nout will be charged till VDD-2$\times$Vthn in the second cycle. Therefore, the 2 cascaded NMOS source followers generate a VDD-2$\times$Vthn voltage, which is nout, to transmit to PVT decider. Again, the cascaded source follower again "magnify" the NMOS threshold voltage and the variation herewith.

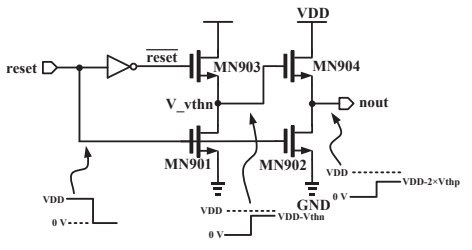

Fig. 5. Schematic of NMOS process sensor

C. Voltage & Temperature sensor

Fig. 6 shows the schematic of Voltage & Temperature sensor. This sub-circuit employs cascaded source followers to generate 2$\times$Vthp, which is similar to the PMOS Process sensor. The difference is that all bulks are coupled to VDD to generate the body effect in each PMOS. By monitoring the variation of PMOS transistor's Vthp, the voltage and temperature variations can be derived as long as the bulk of the PMOS transistor is coupled to VDD.

1) According to Eqn. (1), the Vthp of MOS with body effect will drift at different Vbs, which is the voltage difference between VDD and source voltage of MOS. Notably, Vthp0 is the no body effect threshold voltage, γ_p is the body effect coefficient, Vfn is the bulk surface potential, Vbs is the voltage difference between bulk and source of MOS. In short, supply voltage variation disturbs Vbs, and Vbs then disturbs Vthp.

$$\mathrm{Vthp} = \mathrm{Vthp0} + \gamma_p(\sqrt{2|\mathrm{Vfn}| + \mathrm{Vbs}} - \sqrt{2|\mathrm{Vfn}|}) \quad (1)$$

2) Referring to threshold voltage's characteristic, the Vthp voltage has a negative temperature coefficient around -1mV/°C, which indicates that it is also affected by temperature.

Thus, the 2 cascaded source followers generate 2$\times$Vthp voltage, VTout, with VDD and temperature variation.

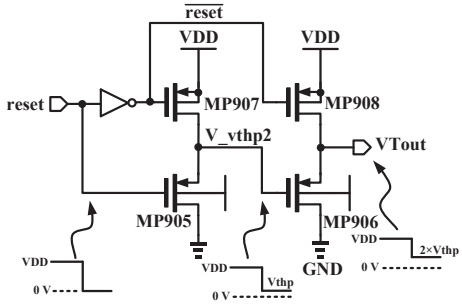

Fig. 6. Schematic of Voltage & Temperature sensor

D. PVT decider

Depending on the above sensors output voltages, PVT decider has to derive two digital codes, Pcode [3:1] and Ncode [3:1], to compensate the 2$\times$VDD output buffer. PVT decider consists of a V_{Bias} generator, three comparators, and a Digital circuit, as shown in Fig. 3. Fig. 7 illustrates the block diagram of Digital circuits, where a 6-bit counter, an Encoder, and D flip-flops are included. When pout, TVout, and nout reach the reference voltage VREFP and VREFN, respectively, comparators deliver, VP, VT, and VN, respectively, to latch D flip-flops (DFFs). According to various corners, the Encoder will create two codes, Pcode [3:1] and Ncode [3:1]. The codes indicates the required compensation status to control the output currents in 2$\times$VDD output buffer.

E. 2$\times$VDD Output Buffer

The 2$\times$VDD output buffer is composed of a Pre-driver, a Vg1 generator, a VDDIO detector, and an output stage, as shown in Fig. 8. Pre-driver is used to encode three control signals, DOUT, Pcode [3:1], and Ncode [3:1], to adjust output currents for slew rate compensation. VDDIO detector and Vg1 generator can generate appropriate gate drive voltages in

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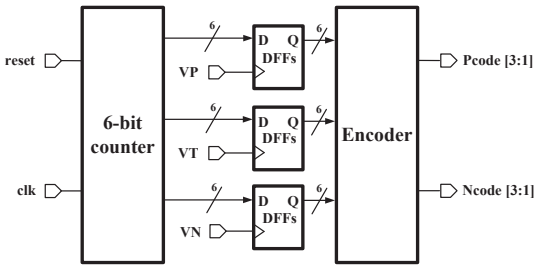

Fig. 7. Architecture of Digital circuit

different voltage modes without leakage currents and overstress problems [7].

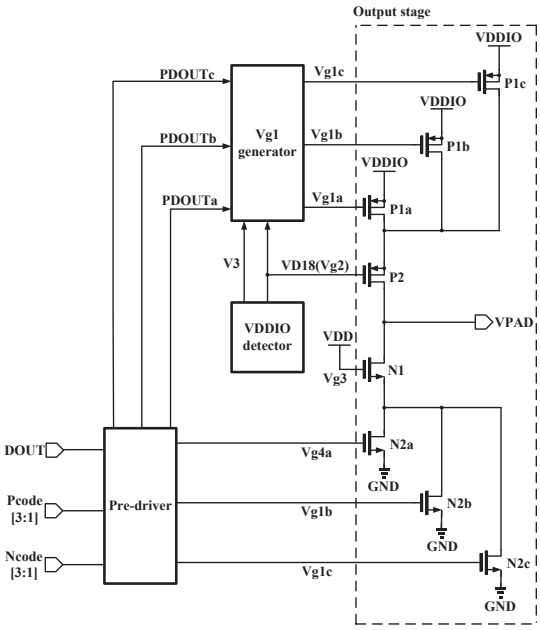

Fig. 8. Schematic of 2×VDD mixed-voltage tolerant output buffer

F. Output stage

Since the supply voltage (VDD) of the core circuits is 1.2 V in 90 nm CMOS process, the output stage must be realized using two groups of stacked PMOS and NMOS transistors, respectively, for transmitting 2×VDD (≈ 2.5 V) signals, as depicted in Fig. 8. PMOSs P1a∼ P1c are in parallel such that the slew rate of the output signal can be selected by turning on or off the currents flowing through P1a∼P1c individually. According to the detected different process and temperature status, Pcode [3:1] and Ncode [3:1] will select the number of turned on PMOSs of output stage. The switching status of N1a∼N1c are corresponding to PMOSs mentioned above. P1a∼P1c and N1a∼N1c are designed with different sizes to generate different currents, which could successfully achieve the required coarse and fine adjustment.

III. Implementation and Measurement Results

The proposed design is implemented using TSMC 90 nm CMOS technology without any thick-oxide device. Fig. 9 shows the die photo of the proposed design, where the overall chip

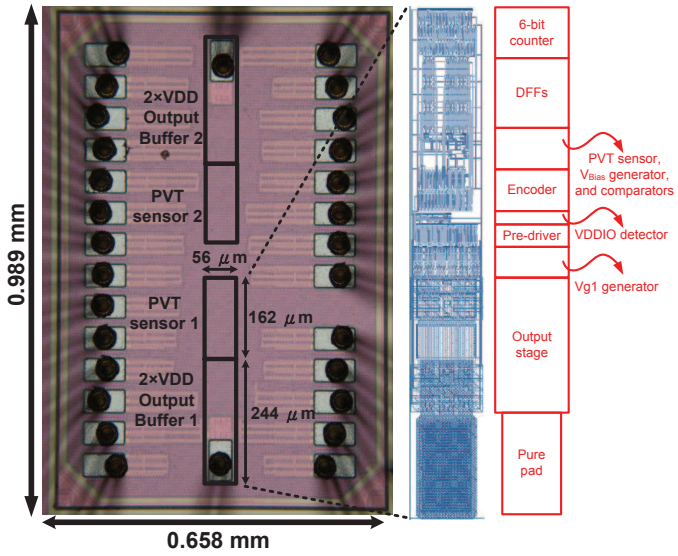

Fig. 9. Die photo of the proposed design

size is only 0.658 × 0.989 mm^2 and the compensation circuit is only 0.056 × 0.162 mm^2. That is, the area overhead is less than 1.4%. Fig. 10 shows the uncompensated and compensated VPAD given VDDIO = 0.9 V in Tx mode. After compensation, the slew rate is enhanced to 809.45 V/μs from 653.47 V/μs. The uncompensated and compensated eye diagrams of VPAD are shown in Fig. 11 and Fig. 12, respectively. The performance of the proposed design is summarized in the Table I. Apparently, the best improvement occurs when VDDIO = 0.9 V, and the fastest data rate is 330 MHz when VDDIO = 0.9 V. Table II shows the comparison between our design and several prior works. Our design attains the edge of all corners process detection, including TT, FF, SS, FS, and SF, and smallest power consumption.

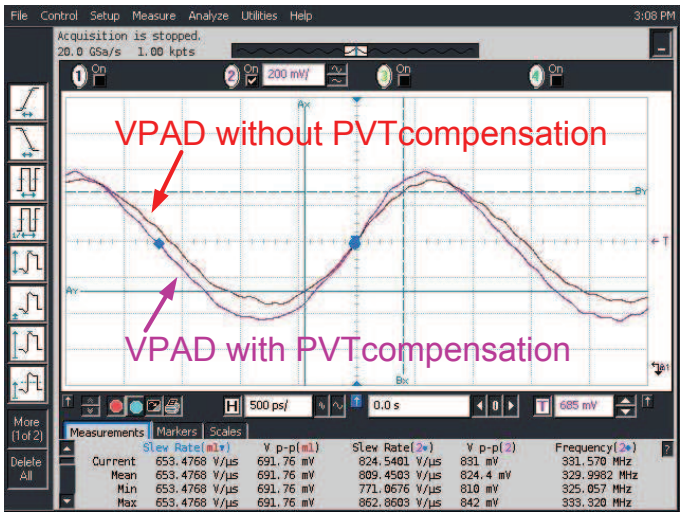

Fig. 10. The uncompensated and compensated VPAD with VDDIO = 0.9 V

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TABLE I
COMPENSATION RESULTS AT DIFFERENT VDDIOS

VDDIO	2.5 V	1.8 V	1.2 V	0.9 V
Data rate (MHz)	300	300	330	330
Eye jitter (ps)	18.2	18.8	18	16.9
Eye width (ns)	1.55	1.55	1.41	1.27
Eye height (V)	1.91	1.82	1.08	0.65
Slew rate improvement (V/μs)	26% (1.31→1.65)	16% (1.4→1.63)	18% (0.85→1)	26% (0.65→0.82)

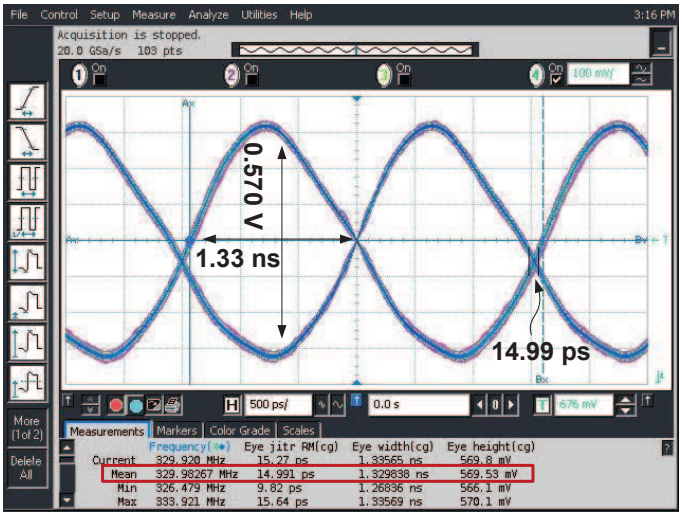

Fig. 11. The uncompensated eyes diagram of VPAD with VDDIO = 0.9 V in Tx mode

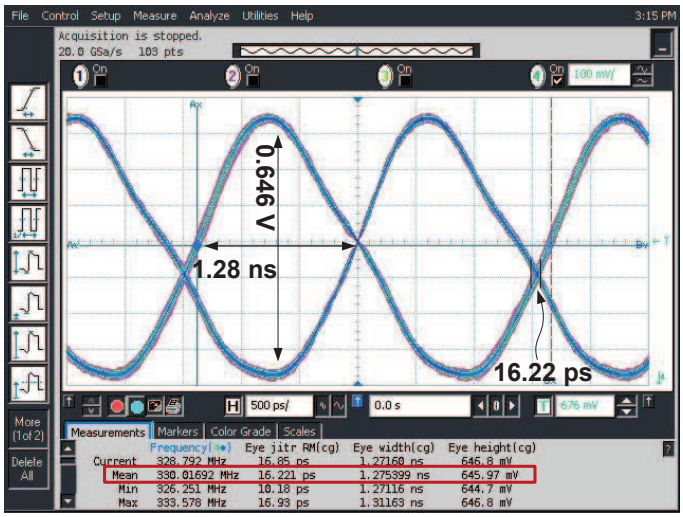

Fig. 12. The compensated eyes diagram of VPAD with VDDIO = 0.9 V in Tx mode

IV. CONCLUSION

A robust compensation circuit is proposed in this paper, where the compensation circuit is implemented using a typical 90 nm CMOS process to self-adjust the slew rate of 2×VDD output buffer. The maximum slew rare improvement can be achieved over 26%. Notably, the PVT sensor and PVT decider are implemented on silicon, therefore, they are easy to real-time detect the PVT corners of PMOS and NMOS, respectively.

TABLE II
PERFORMANCE COMPARISON OF OUTPUT BUFFER

	Ours	[2] *ISSCC*	[3] *JSSC*	[4] *JSSC*
Year	2011	2007	2003	2003
Process (μm)	0.09	0.18	0.35	0.18
Results	Measured	Post-sim	Measured	Measured
Slew rate (V/ns)	0.65-1.65	2.10-3.58	1.60-2.20	0.40-0.99
Process corners detected	TT, FF, SS FS, SF	TT, FF, SS	TT, FF, SS	TT, FF, SS
Power (mW)	2.2	13.7	N/A	N/A
Slew rate improvement	26%	N/A	N/A	32%

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