A High Voltage Analog Multiplexer with Digital Calibration for Battery Management Systems

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***Abstract*—This work presents a multi-channel high voltage analog multiplexer with digital calibration for battery management systems (BMS). For a high voltage battery management systems, the front end circuit must be able to accommodate input voltage up to tens of volts, perhaps even hundreds of volts. To realize a possible solution on silicon, the front end of BMS shall be fabricated using an advanced HV (high voltage) semiconductor process, which usually is constrained by the voltage limitation between gate and source of HV devices. To overcome such a limitation, a high voltage gate control circuit is proposed in this work, including digital calibration that can compensate the output voltage loss of the multiplexer. An experimental prototype is implemented using a typical 0.25 μm 1-poly 3-metal 60V BCD process. The post-layout-extracted simulation results reveal that the worst-case error is less than 2 mV with calibration, which is 91% improvement compared with the state of art based on thorough simulations.**

***Index Terms*—high voltage, analog multiplexer, battery management system, digital calibration**

I. Introduction

High voltage (HV) BMS is widely needed in many applications, e.g., EV and HEV, where many battery modules are assembled and integrated. These modules are composed of many series of batteries to generate a high supply voltage. If the battery module is made of series batteries, they will be unavoidably unbalanced among battery cells in voltage and capacity after a few times of charging and discharging cycles. Notably, the above hazard is always happened no matter when the battery module is charging and discharging. If either over-charge or over-discharge occurs to any battery cell, the efficiency and health of the battery will be degraded. What even worse is that the Li-lon battery might be burned out and exploded. Therefore, BMS with charge equalization is critically required in battery-operated applications.

A typical custom BMS is composed of five blocks, including Measurement, Management, Analysis, Communication, and Logging & Telemetry, as shown in Fig. 1 [1]. The front end of BMS is namely Measurement, which senses the battery information, e.g., voltage, current, temperature, etc. For a series of 8 batteries, the highest voltage of battery module will reach 29.2 V (A Li-lon battery voltage is assumed to be 3.65 V). Therefore, high voltage tolerance is required in the front end of BMS. Prior voltage measurement approaches are categorized into three types [1], as shown in Fig. 2. Referring to Fig. 2 (a), each battery cell is parallelly coupled to an ADC such that no HV multiplexer is needed. However, too many ADCs in such a scenario shall result in high power consumption and large area. Fig. 2 (b) and (c) are more popular methods for BMS to save power and area. The multiplexer is in charge of converting high voltage of each battery into the input range of the sole ADC. Consequently, the voltage distortion caused by the multiplexer must be as small as possible.

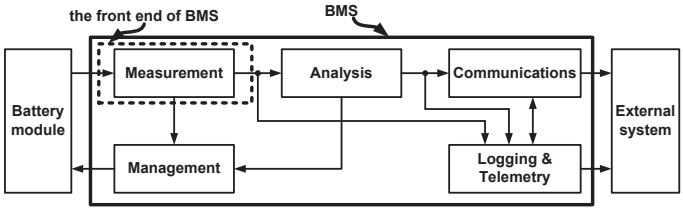

Fig. 1. The explosive view of a typical custom battery management system (BMS)

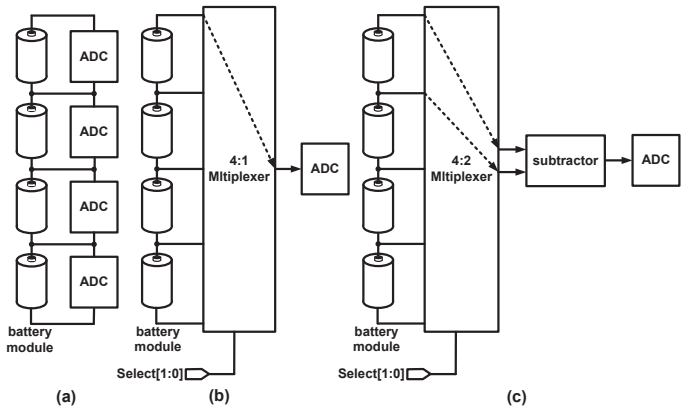

Fig. 2. Three architectures of voltage measurement methods

Several HV multiplexers using multi-process technique have been reported [2]-[3]. An 8-channel HV multiplexer was proposed using both junction-isolated (JI) and dielectrically isolated (DI) D/CMOS process technologies [2], including a HV level-shift circuit to drive a switching MOS. A 16:1

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analog multiplexer was revealed using a combination of process (CMOS/SOI) techniques [3], where 5 V CMOS logic circuits are shifted up to ±15 V to drive HV analog switches. HV drivers and analog switches are also widely used in LCDs, imaging system, and one-time programmable (OTP) memory [4]-[7].

Recently, many advanced semiconductor processes have been provided to fabricate HV devices on silicon, e.g., TSMC 0.25 μm 1-poly 3-metal 60V BCD process. This particular process offers digital cell library, low voltage (LV) MOSs driven by 2.5 V/5 V, and 60 V power MOS. The most critical limitation is that the gate to source voltage of the HV MOS must be limited under a low voltage ≈ 5 V. Therefore, those mentioned prior works are not easy to be directly implemented using such HV BCD process.

To resolve the above problem, a novel HV analog multiplexer with digital calibration is disclosed in this paper. The proposed design converts the voltage drop of every battery in the same string into a low voltage level between 1 V and 2 V, which is the input range of an ADC. Therefore, the proposed design can be accommodated in the front end of an BMS. The rest of this paper is organized as follows. In Section II, the HV analog multiplexer is analyzed, where the digital calibration scheme is included. Particularly, a current DAC is in charge of calibrating the output of HV multiplexer to ensure the conversion accuracy. In Section III, we demonstrate the all-PVT-corner post-layout simulation results of the proposed design by HSPICE. The performance comparison between our design and prior works is also discussed. Finally, a brief conclusion is given in Section IV.

II. The Architecture of the Proposed Design

The front end of BMS is composed of an 8:1 HV analog multiplexer (HVMUX), a Digital Calibration, an Oscillator, and a 2^{nd} order ΣΔ ADC, as shown in Fig. 3. The HVMUX selects a pair of input voltages, namely VinXn∼VinXp, X=1, 2,$\cdots$8, and passes to the 2^{nd} order ΣΔ ADC. The Oscillator generates a CLK signal, which is about 512 KHz frequency, to serve as the clock of the 2^{nd} order ΣΔ ADC. The 2^{nd} order ΣΔ ADC converts ADC_in into digital codes, ADCOUT[11:0]. Switch[2:0] selects one battery in Battery module to be sensed. Calibration[3:0] triggers the Digital Calibration to compensate the input voltage loss of ADC_in. C_compensation and R_compensation are, respectively, coupled to an off-chip resistor and a capacitor to fine tune the frequency of CLK to be exactly 512 KHz.

The proposed HVMUX is shown in Fig. 4, including HV switches, HV subtractors, Low voltage multiplexer (LVMUX), Voltage multiplier, Digital Calibration, and Decoder. The Decoder converts Switch[2:0] into S[0]∼S[7] to drive the HV switches. The function description of each block of HVMUX is given in the following text.

A. HV switches & HV subtractors

An HV switch is composed of eight HV switch cells, where each HV switch cell comprises M_{HVP}, R_{HV}, and M_{HVN}, as shown in Fig. 5. M_{HVP}, R_{HV}, and M_{HVN} are HV devices. Notably, Vgs of the HV devices must be smaller than 5 V.

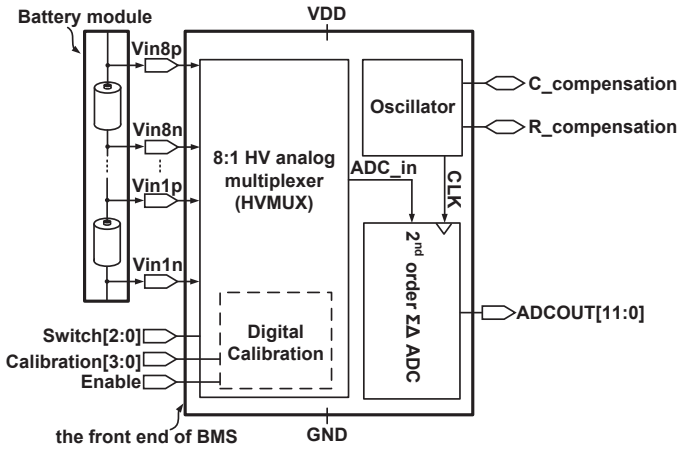

Fig. 3. Block diagrams of the front end of BMS

The Vgs of M_{HVN} is driven by S[0], which is a digital signal with a swing 0 to 2.5 V. Therefore, M_{HVN} is ensured without any over-voltage hazard. To prevent the over-voltage damage of M_{HVP}, the voltage drop of R_{HV}, namely V_{RHV}, must be smaller than 5 V. In other words, V_{RHV} must be constrained by the following equation:

$$\mathrm{V_{RHV}} = \mathrm{I_{RHV}} \times \mathrm{R_{HV}} < 5\,\mathrm{V} \tag{1}$$

where I_{RHV} is the current of R_{HV}. Assumed M_{HVN} is biased in the saturation region, the drain current of M_{HVN}, namely I_{RHV}, can be written as

$$\mathrm{I_{RHV}} = \frac{\beta_{\mathrm{MHVN}}}{2}(\mathrm{V_{S[0]}} - \mathrm{Vth_{MHVN}})^2 \tag{2}$$

where β_{MHVN} represent the device parameter of M_{HVN}, and Vth_{MHVN} is the threshold voltage thereof. Substituting Eqn. (2) into Eqn. (1), β_{MHVN} can be derived as

$$\beta_{\mathrm{MHVN}} < \frac{2 \times 5\,\mathrm{V}}{(\mathrm{V_{S[0]}} - \mathrm{Vth_{MHVN}})^2 \times \mathrm{R_{HV}}} \tag{3}$$

Eqn. (3) shows how to calculate the device parameter of M_{HVN}, where R_{HV} can be determined based on the limitation of power dissipation. For instance, high R_{HV} shall decrease dc current of I_{RHV} to save power.

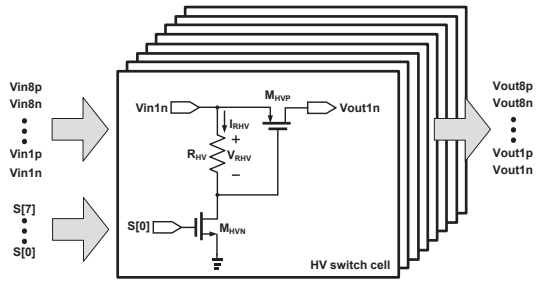

Fig. 5. Schematic of HV Switches

Fig. 6 shows the schematic of HV subtractors composed of an operational transconductance amplifiers (OTA), R1, and R2. R1 and R2 are HV resistors with 60 V tolerance. Take Vbattery1 as an example, it can be derived as follows.

$$\mathrm{Vbattery1} = \frac{\mathrm{R_2}}{\mathrm{R_1}} \times (\mathrm{Vout1p} - \mathrm{Vou1n}) \tag{4}$$

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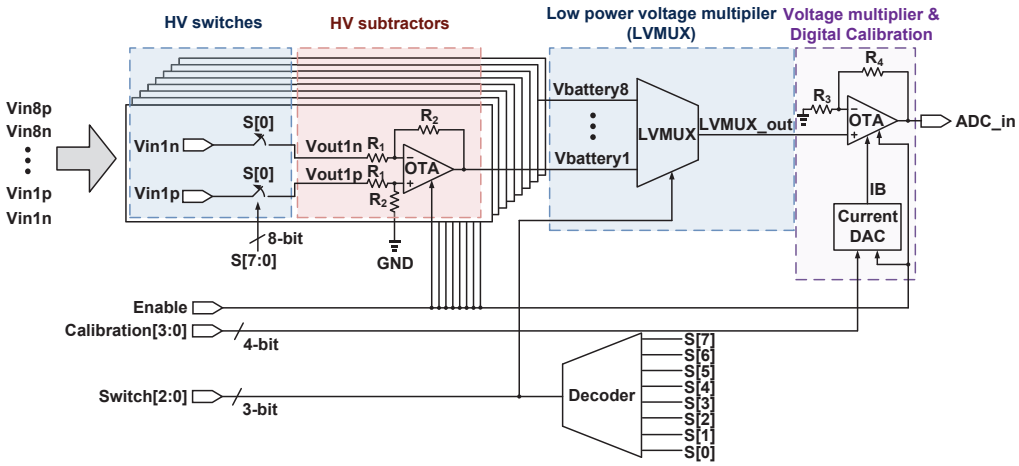

Fig. 4. Schematic of 8:1 HV analog mutiplexer (HVMUX)

where (Vout1p-Vou1n) is the voltage drop of the first battery, while the ratio of R_2 and R_1 is utilized to shift the voltage of battery into a lower voltage range.

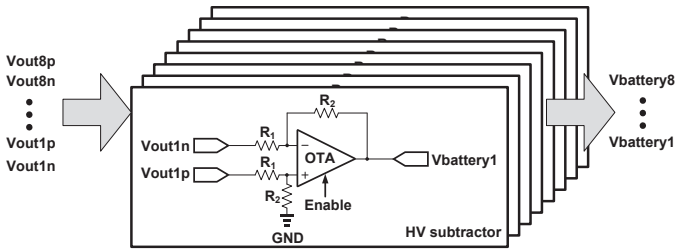

Fig. 6. Schematic of HV subtractors

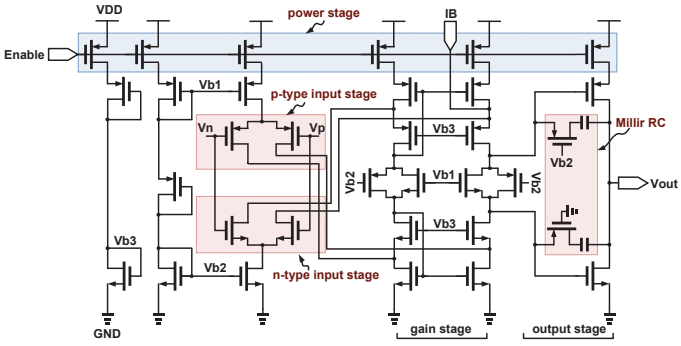

Fig. 7. Schematic of OTA

B. Low voltage multiplexer & Voltage multiplier

Low voltage multiplexer (LVMUX) in Fig. 4 is composed of 8 transmission gates, which are respectively driven by S[0]∼S[7]. LVMUX selects one of Vbattery1∼Vbattery8 to LVMUX_out.

Voltage multiplier multiplies the voltage at LVMUX_out with the ratio of R_4 and R_3 to generate a corresponding ADC_in for the following ADC.

$$\text{ADC\_in} = (1 + \frac{R_4}{R_3}) \times \text{LVMUX\_out} \tag{5}$$

where R_4 and R_3 are used to adjust the LVMUX_out into the voltage range of ADC, and LVMUX_out is the output voltage of LVMUX.

C. Digital Calibration

Digital Calibration [9] compensate the voltage loss of ADC_in by Current DAC tuning IB of OTA according to Calibration[3:0]. A rail-to-rail amplifier topology [8] is adopted to implement OTA in Fig. 4. The detailed schematic of the OTA is shown in Fig. 7. Enable is used to power gate the entire OTA for the sake of power saving if the OTA is not used.

Current DAC in Fig. 4 uses simple current mirrors to generate a set of binary weighted currents. The matching accuracy of MOS transistors depends on size and the ratio of W/L. The magnitude of IB is expressed as follows.

$$\begin{aligned}\text{IB} = [&\text{Calibration}[0] \times 2^0 + \text{Calibration}[1] \times 2^1 + \\ &\text{Calibration}[2] \times 2^2 + \text{Calibration}[3] \times 2^3] \times \text{IREF}\end{aligned} \tag{6}$$

where IREF is the reference current. IREF is replicated in each of the transistor arrays. Calibration[3:0] determine the magnitude of IB flowing into OTA to compensate the voltage loss of ADC_in.

III. Implementation and Simulation

The proposed design is implemented using the 0.25 μm 1-poly 3-metal 60V BCD process to justify the performance. Fig. 8 shows the layout the the proposed design. The chip area is 1.985×1.9 mm^2, where the core area is 1.608×1.6 mm^2. Fig. 9 shows the error distribution comparison of the proposed HV analog multiplexer with and without calibration. The worst-case error is reduced from 22 mV to 2 mV. Fig. 10 shows the error distribution with calibration given 3 different battery voltages, which are the lower bound, typical, and upper bound voltage of a Li-ion battery. Table I shows the comparison of the proposed design with several prior works. Our design attains the smallest On resistance and the second best isolation, -79.4 dB@10 MHz.

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TABLE I
COMPARISON BETWEEN THE PROPOSED DESIGN AND PRIOR WORKS

	This work	[5]	[3]	[7]
Year	2012	2005	2008	2011
Process (μm)	0.25 μm 60 V BCD	0.35 μm SOI	30 V CMOS/SOI	0.35 μm 50 V
Number of switches	8	32×32	16	4
Analog input range	2∼29.2 V	-40∼40 V	-5∼25 V	0∼40 V
On resistance	16.8 Ω	N/A	<1500 Ω	26 Ω
Isolation	-79.4 dB@10 MHz	-53 dB@4 MHz	-45 dB@0.2 MHz	-90dB@10 MHz
Power dissipation	17.79 mW	10 mW/switch	<15 mW	N/A

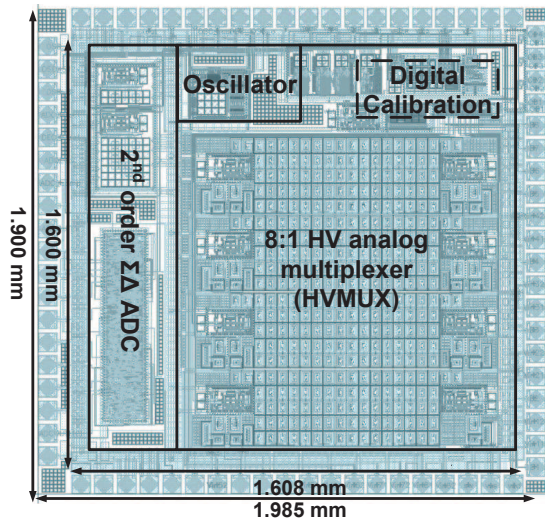

Fig. 8. The layout of the proposed design

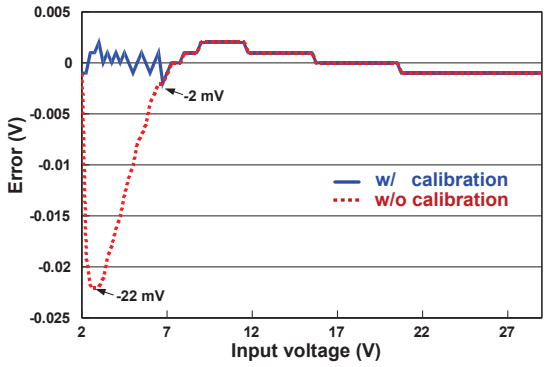

Fig. 9. Error distribution of the proposed HV analog multiplexer with and without calibration

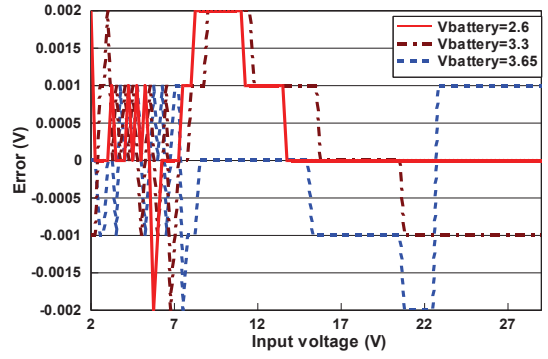

Fig. 10. Error distribution given 3 different battery voltages

IV. CONCLUSION

In this paper, we propose a total solution in the front end for BMS. The proposed design is implemented using a typical 0.25 μm 1-poly 3-metal 60V BCD process such that it can be easily integrated in a possible SOC (system-on-chip) solution for high voltage BMS. The simulation results justify our design to be a multi-channel HV analog multiplexer with obscure distortion. Finally, the digital calibration method is proved to compensate the voltage loss of HV analog multiplexer over 90% improvement.

V. ACKNOWLEDGEMENT

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