Single-ended Disturb-free 5T Loadless SRAM Cell Using 90 nm CMOS Process

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***Abstract*— A novel single-ended load SRAM cell is proposed in this study, where a loadless SRAM cell with write assistant loop and an isolated wordline-controlled transistor (WLC) is revealed. A shared bitline inverter is included to boost the read access speed at the minimal expense of area cost. The energy dissipation per write/read operation is found to be 0.479/0.091 fJ provided that the SRAM cells is supplied a 0.6 V VDD region using a typical 90 nm CMOS technology. The proposed cell is proved to attain the smallest area, PDP (power-delay product) and disturb-free during the memory access.**

***Keywords*—single-ended SRAM cell, loadless, power-delay product (PDP), subthresold region, disturb-free**

I. INTRODUCTION

Owing to the demand of long operation time of personal data devices, e.g., smart phones, and tablets, the low power design requirement has become very much overwhelming in every aspect of a electronic system. As well noted, memory devices have long been the core of digital systems next to CPUs. They have undoubtfully consumed a great portion of the battery power. When the performance at low power supply voltage of the memory is able to meet the system demand, voltage scaling is considered the most effective method to reduce the power dissipation therewith [7]. The 4-T loadless SRAM was proposed to be a possible solution for the lower power demanding SRAM [1], where low-V_{th} transistors are used as bit line drivers and high-V_{th} transistors are the data latch components. Not only can the access time be shortened, the data retention is also enhanced. Although the P-latch N-drive 4-T SRAM cell with a built-in self-refreshing data retention path to eliminate the WLC and ehnace the accessing speed of the SRAM was proposed , the read/write disturbance is queationable in such a cell due to lack of bitline isloation mechanism. The degration of the SNM (static noise margin) pointed out in [2] has verified such a potential hazard. Though the negative WLC scheme reported in [2] was proved to be funcational, the overhead using multiple VDD supplies are required but costly. Another possible approach is to employ vriable bulk bias [3]. However, the latch-up problem might be introduced as well. The asymmetrical W/R-assist approach proposed in [4], [5], and [6] has drawn a great attention. These works highlight the necessity of disturb-free design at the low voltage supply scenarios, particulary when the SRAM is asked to carry out R/W in the subthrehsold region using a nano-scale CMOS process. However, the area and power overhead caused by those auxiliary circuits and transistors are very significant. It is unacceptable in low power or low cost applications.

In this investigation, a loadless SRAM with a write-assist loop to isolate the WLC such that the write disturbance free is feasible. On the othe other hand, a shared read inverter is used to reject the potential bitline voltage variation so as to guarantee the disturb-free. Notably, the SRAM cell itself is a 5-T design with a pair of high-V_{th} PMOS transistors to serve as the latch-like storage. According to the all-PVT-corner post-layout simulations, the proposed SRAM cell outperforms the existing SRAM cells given the same 90-nm CMOS process. The write/read operation consumes 0.479/0.091 fJ, respectively, with VDD = 0.6 V in the worst PVT corner.

II. LOAD-LESS SRAM CELL WITH DISTURB-FREE

The theory of the loadless SRAM cells will be revealed in this section. Then, the W/R-assist circuits will be introduced and analyzed.

A. Analysis of hidden self-refreshing path

Referring to Fig. 1, the data bits kept in the back-to-back high-V_{th} PMOS pair, i.e., P1 and P2. N1 and N2 are respectively meant to be the bit lines (BL, BLB) drivers which are controlled by word line (WL). If the threshold voltage of N1 and N2 is lower, the switching time of N1 and N2 will be reduced which will in turn shortens the access time of the SRAM cell. Besides, larger driving currents will be supplied to drive the bitlines.

It is also well known that such a pseudo-latch still possesses the leakage problem which leads to the loss of the stored data. The leakage can be neutralized by "hidden self-recharging path". Referring to Fig. 2, assume that N1, N2 are off given that WL = 0. A total of 4 currents affect the voltage level of node Q when the data node Q is floating.

$$\text{subthreshold current : } I_{P1} \text{ and } I_{N2}$$
$$\text{reverse bias current : } I_{D1} \text{ and } I_{D2}$$

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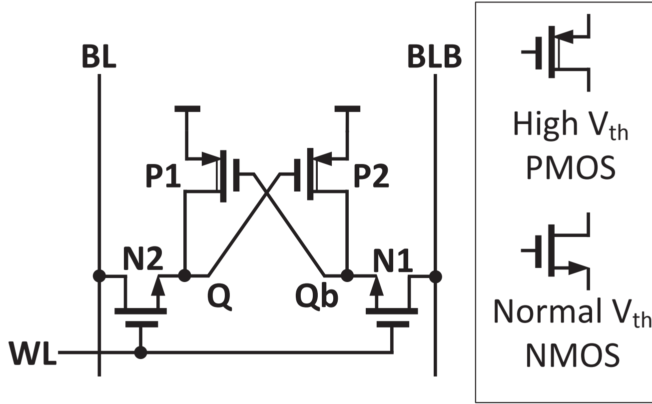

Fig. 1. Schematic of the loadless SRAM cell

The requirement of the data retention for the possible weak "0" at node Q is (I_{P1}+I_{D1}) $<$ (I_{N2}+I_{D2}). Notably, the magnitude of the subthreshold currents are adjustable according to the following equations.

$$I_{sub} = \frac{W}{L} e^{\frac{V_{gs}-V_t}{nV_T}} (1 - e^{\frac{-V_{ds}}{V_T}}) \quad (1)$$

$$I_D = WL^{'} \cdot I_S(e^{\frac{V}{V_T}} - 1) = I_{leakage} \quad (2)$$

where L and $L^{'}$ denote the widthes of the gate and the parasitic diode, respectively. Thus, the data retention problem can be resolved by solving the W/L ratios to meet the requirement of $(I_{P1} + I_{D1}) < (I_{N2} + I_{D2})$. Apparently, the loadless SRAM cell attains the edge of area efficient based on the above analysis.

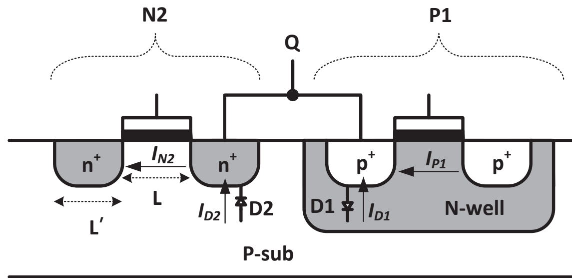

Fig. 2. Side view of the loadless SRAM cell

B. Disturb-free loadless 5T SRAM cell

Alougth the prior loadless SRAM has been proven to be high speed and small area, the price to pay is the reduction of the noise margins, particularly SNM [8]. The reason, obviously, is caused by the bitline disturbance during the R/W operation. Such a disadvantage will become even worse if the SRAM is implemented using nano-scale technologies, where the leakage current, including the subthreshold current, tends to dominate the power dissipation and even compromise the stored data bits. We, then, propose a novel loadless SRAM cell in this study to resolve the above predicament. Referring to Fig. 3, a single-ended disturbance-free load-free 5T SRAM cell is revealed.

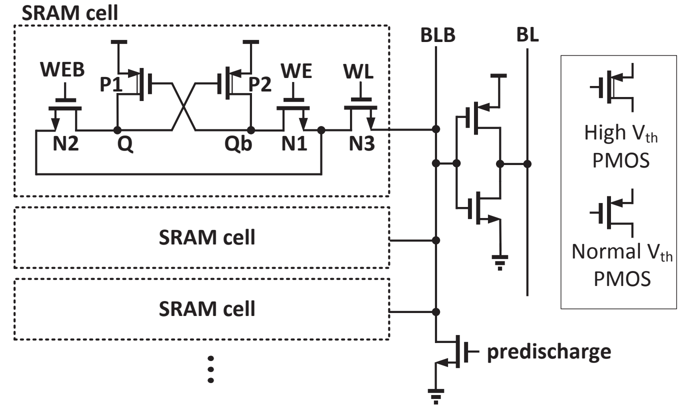

Fig. 3. Proposed disturb-free loadless SRAM cell

Referring to Fig. 3, to reject the potential disturbance from the bitlines, we propose to insert one WL-controlled transistor ($\approx$ WLC), namely N3, between BLB and the cell. Besides, the sources of N1 and N2 are coupled to become the "write-assist loop", where the common mode noise coupled from GND will likely be rejected. Notably, N1 and N2 are driven by WE (write enable) and WEB (write enable bar), respectively.

• **Read access** : The read operation timing diagrams are shown in Fig. 4. As soon as the address lines are valid, WL is asserted to turn on N3. Meanwhile, WE is high and WEB is low. The state at Qb will be passed to BLB via N1 and N3. Notably, a shared inverter is inserted between BLB and BL to reject the nose coupled in BL. Besides, the shutoff N2 will ensure Q is free from the disturbance of BLB.

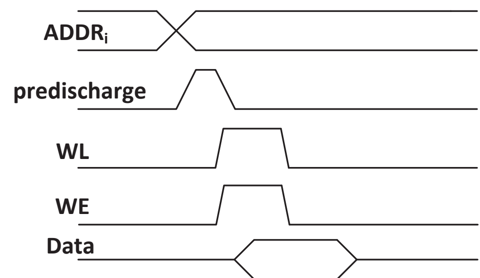

Fig. 4. Read timing diagram of the proposed loadless SRAM cell

• **Write access** : By contrast, the write operation timing diagrams are shown in Fig. 5. When the address lines are valid, WL is asserted to turn on N3. Meanwhile, WE is high and WEB is low. The state of Qb will be coupled to BLB via N3 and N1 to either flip or stay the same. As stated earlier, the state of Q might become the complementary of Qb via the latch-like PMOS pair. Most important of all, the shutoff N2 prevents Q from the disturbance of BLB.

Therefore, the proposed loadless 5T SRAM cell is a single-ended disturb-free design. Besides the R/W noise margins can

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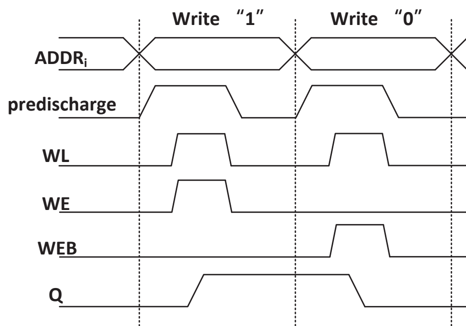

Fig. 5. Write timing diagram of the proposed loadless SRAM cell

be enhanced, the area cost is also drastically reduced compared with the known disturb-free design approaches. Notably, the inverter bewteen BLB and BL is shared by many SRAM cells, since only one cell in a single column is allowed to access the bitline pair in any single R/W cycle. The area overhead is obscure.

C. Various disturbance-free SRAM cells

Certainly, many disturb-free SRAM cells have been reported or evovled from conventional 6T cells, including Type 1 (8T, Fig. 6) [4], Type 2 (9T, Fig. 7) [5], loadless Type 1 (7T, Fig. 8), and loadless Type 2 (7T, Fig. 9). Apparently, these deisgn might also attain the disturb-free performance at the expense of large cell area and power dissipation due to complicated auxillary circuits therewith.

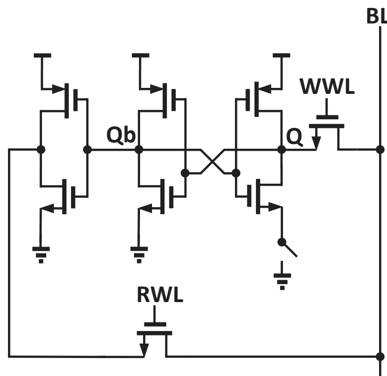

Fig. 6. Disturb-free SRAM cell in [4]

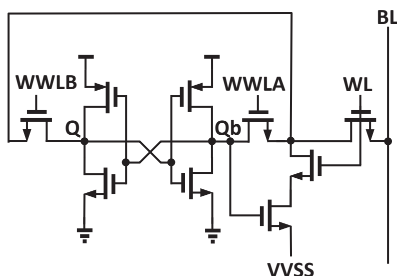

Fig. 7. Disturb-free SRAM cell in [5]

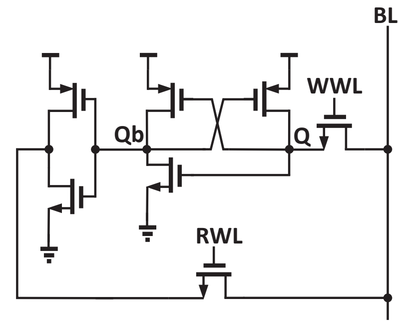

Fig. 8. Loadless SRAM cell type 1

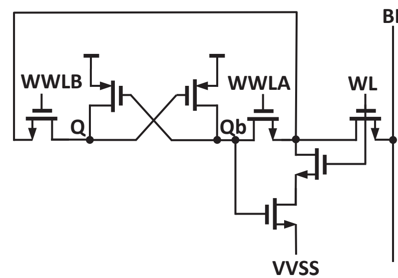

Fig. 9. Loadless SRAM cell type 2

III. Implementation and Simulation

Thorough all-PVT-corner simulations are a must to justify the performance of the proposed 5T loadless SRAM cells. Referring to Fig. 10, the area of the proposed cell is 2.05×1.12 μm^2 using a typical 90 nm CMOS process (TSMC). Compared with the cell in Fig. [4], i.e., 0.8×3.96 μm^2 using the same process, our area saving is 28% per cell.

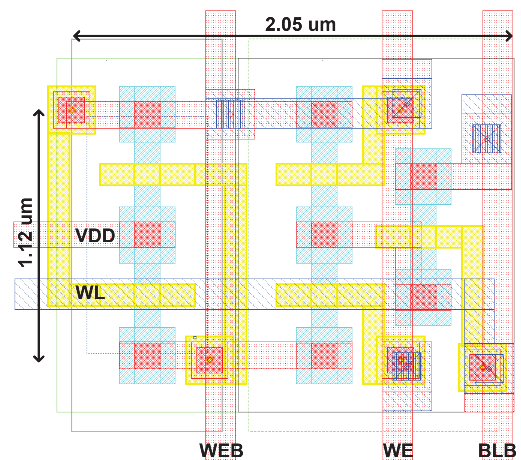

Fig. 10. Layout of the proposed SRAM cell

The read SNM of the proposed cell are shown in Fig. 11. Since one of the WEB and WE will be low to shut off one of the access NMOS, either Q or Qb will remain the same during the read operation, which is different from the conventional

6T-based SRAM cells. The read SNM is 326.90 mV, which is far better than the other single-ended SRAM update date. Most important of all, the write operation of the proposed cell is disturb-free in any case. The comparison with prior works using the same 90 nm CMOS process based on all-PVT-corner psot-layout simulations with VDD=0.6 V is tabulated in Table I.

Notably, the PDP in Table I stands for power-delay product, which is also the enerfy dissipation in every single read/write. Meanwhile, FOM is estimated by the following equation,

$$\text{FOM} = \frac{\text{SNM}}{\text{Write PDP} \times \text{Read PDP} \times \text{normalized CA}}, \quad (3)$$

where CA denotes cell area. The proposed design outperforms the others with respect to the SNM, cell area, and write disturb-free. Besides, our design also attains the edge of quite balanced PDP in read/write operations. The FOM summarizes the overall performance that our cell is recognized as the best of all.

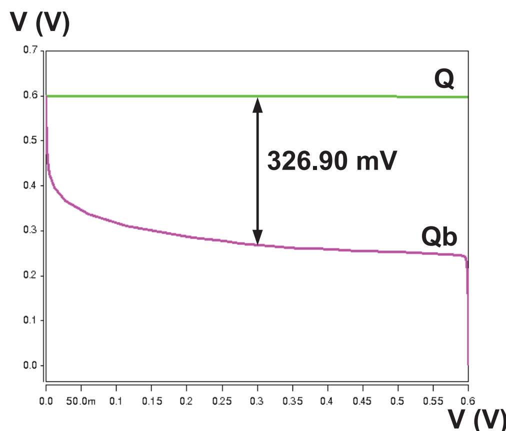

Fig. 11. Read SNM of the proposed SRAM cell

TABLE I
COMPARISON WITH PRIOR WORKS

	[4]	[5]	loadless-I	loadless-II	this work
Transistors	8T	9T	7T	7T	5T
SNM (mv)	283.54	267.85	291.87	313.00	326.90
WM (mV)	281.90	N/A	282.30	N/A	N/A
Write PDP (fJ)	1.08	4.37	0.727	5.72	0.187
Read PDP (fJ)	0.248	0.039	0.194	0.0419	0.130
Cell Area (μm^2)	3.96 $\times$0.8	3.625 $\times$1.18	2.835 $\times$1.12	2.955 $\times$1.18	2.05 $\times$1.12
FOM	2.7005	5.2712	2.9821	3.0305	47.4349
Year	2010	2011	2011	2011	2012

IV. CONCLUSION

This paper presents a low-power single-ended loadless 5T SRAM cell with disturb-free write access. By inserting a WL-controlled NMOS between the cell and BLB, the pontential interference from bitlines is de-coupled during the access. Besides, the shared inverter to drive BL attains the high driving current and noise rejection at a relatively small area cost. Thorough post-layout simulaitons have justified the outstanding performance of the proposed SRAM cell in terms of SNM, area and power-delay product.

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