A Digital Over-temperature Protector for FlexRay Systems

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***Abstract*—This work presents a digital over-temperature protector for FlexRay systems. A temperature sensor with a negative coefficient with respect to frequency is realized on silicon. A frequency to digital converter (FDC) is used to convert the frequency into a digital code to represent the sensed temperature. An experimental prototype was implemented using a typical 0.35 μm CMOS process. The post-layout-extracted simulation results reveal that the worst error is less than $\pm 6^{\circ}\mathrm{C}$ at all PVT (Process, voltage, and temperature) corners. Notably, the error is less then $\pm 1.8^{\circ}\mathrm{C}$ in the range from $0^{\circ}\mathrm{C}$ to $100^{\circ}\mathrm{C}$.**

***Index Terms*—temperature sensor, temperature detector, over-temperature protector, FlexRay system**

I. Introduction

Recently, FlexRay [1] is considered as a total solution to govern different in-car communication networks, e.g., CAN or MOST, since it is mainly aimed at safety and reliability. According to FlexRay specifications, a FlexRay system must be operated in $-40^{\circ}\mathrm{C} \sim +125^{\circ}\mathrm{C}$, which means a over-temperature protector is required to ensure that no hazards would be caused by temperature problems. The over-temperature protector shall provide a means to monitor the junction temperature on silicon. If a pre-defined threshold is exceeded, the over-temperature protector must disable the transmitter, which usually demands the largest power consumption in a FlexRay system, to prevent further heating of the chip. Therefore, the over-temperature protector plays an important role in a FlexRay system.

Traditionally, temperature detectors are categorized into two different types, i.e., voltage detection and digital detection. The voltage detection scheme basically comprises a temperature sensor and an analog to digital converter (ADC). The temperature sensor at least possesses a temperature-sensitive feature or measure to generate a temperature-sensitive voltage. Then, the ADC converts the temperature-sensitive voltage into a digital code. Notably, the conversion between voltage and temperature is expected to be linear to attain high precision. Usually, the range of temperature-sensitive voltage is close to 100 mV from $0^{\circ}\mathrm{C}$ to $+100^{\circ}\mathrm{C}$ such that a high precision ADC is required to distinguish the difference in such a small voltage window. Thus, a sigma-delta ADC is widely used in this kind of temperature detectors [2]. Notably, a high precision sigma-delta ADC is not easy to design in a full digital circuit.

Recently, many researchers turn their attention to the digital detection type. There are two kinds of temperature sensors in the digital detection type, i.e., oscillator [3], and delay cells [4]. In [3], the frequency of oscillator shall be increased or decreased varying with the temperature. Depending on the sensitivity between temperature and oscillator, a frequency to temperature converter (FTC) is used to convert the frequency into digital codes. The other way is to detect the temperature variation by the delay time of delay cells [4]. When the temperature is increased, the delay time of delay cell is increased, and vice versa. Therefore, delay cells are as good as the oscillator in a temperature detector. The temperature detector with digital detection is very welcomed in a system-on-chip (SoC) design. The reason is that the oscillator and delay cells are digital circuits, which are easily implemented and integrated by Verilog code. That is, a temperature detector with digital detection are easily migrated among different CMOS processes, e.g., 0.35 μm, 0.18 μm, and other advanced CMOS processes. Therefore, it is also easy to be integrated in a FlexRay system.

This work proposes a digital over-temperature protector for FlexRay systems, which is deemed as the digital detection type. The proposed digital over-temperature protector is used to detect the temperature variation form $-40^{\circ}\mathrm{C}$ to $+125^{\circ}\mathrm{C}$. In Section II, we propose a temperature sensor and a frequency to digital converter. The temperature sensor generates a frequency depending upon temperature variation. The following frequency to digital converter approximates a linear equation to describe the slope between temperature and frequency based on interpolation of sampled data. A data flow of the frequency to digital converter is also shown in Section II. In Section III, we demonstrate the simulation results of the proposed digital over-temperature protector by HSPICE, Model-Sim, and an FPGA board. The performance comparison between our digital over-temperature protector circuit and the prior works is given as well A brief conclusion is given in Section IV.

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II. Protector Architecture

The proposed digital over-temperature protector is composed of a Bandgap, a temperature sensor and a frequency to digital converter (FDC), as shown in Fig. 1. The Bandgap circuit generate the Vbias = 2.8 V to the temperature sensor (TS). TS then generates a temperature-sensitive clock (Fout). Then, FDC converts Fout into digital codes. The Clk is the main clock of FDC. The reset resets all digital circuits and activate the temperature sensor. The retest will clear the previous temperature's value and sense new temperature. The mode[1:0] and next_mode are in charge of calibrating the derived equation between temperature and frequency. Finally, if the temperature detection is done, the EOC is pulled high to notify the user or any following circuit. The function of each block of the proposed design is given in the following text.

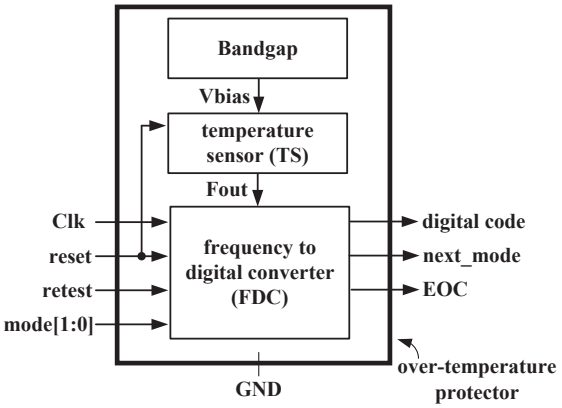

Fig. 1. The proposed over-temperature protector

A. Temperature sensor (TS)

The TS consists of a $3\times V_{BE}$ generator, three Delay Stages, a Buffer Stage, and two Dummy Stages, as shown in Fig. 2. The $3\times V_{BE}$ generator generates a temperature-sensitive voltage, Vcs, which is 3 times of the V_{BE} voltage of BJTs (Q_1, Q_2, and Q_3). By Eqn. (1), V_{BE} is the voltage difference between the base and emitter of BJT ($V_{BE} \approx 0.7$ V), Is is the BJT scale current (Is $\approx 1\times e^{-18}$ A), V_T is the thermal voltage ($V_T \approx 26$ mV at room temperature), and n is the emission coefficient (n = 1). R0 can be derived as follows.

$$I_{R0} = \frac{VDD - 3 \times V_{BE}}{R0} = Is \times e^{\frac{V_{BE}}{nV_T}} \quad (1)$$

Three Delay Stages are cascaded to serve as a ring oscillator. Referring to [5], the V_{BE} voltage has a negative temperature coefficient about -1.5 mV/°C. Take the rightmost Delay Stage in Fig. 2 as an illustrative example. The gate of M6 is driven by Vcs, which is 3 times of V_{BE} voltage. That means the tail current via M6, Ics, also attains a negative temperature coefficient. Notably, the output clock frequency of the ring oscillator is proportional to Ics. Therefore, a clock with negative temperature-sensitive frequency is generated. The Buffer Stage is in charge of driving logic circuits in FDC, namely Fout. Meanwhile, Dummy Stages mimic the delay of each Delay Stage to force the duty cycle of Fout as close to 50% as possible.

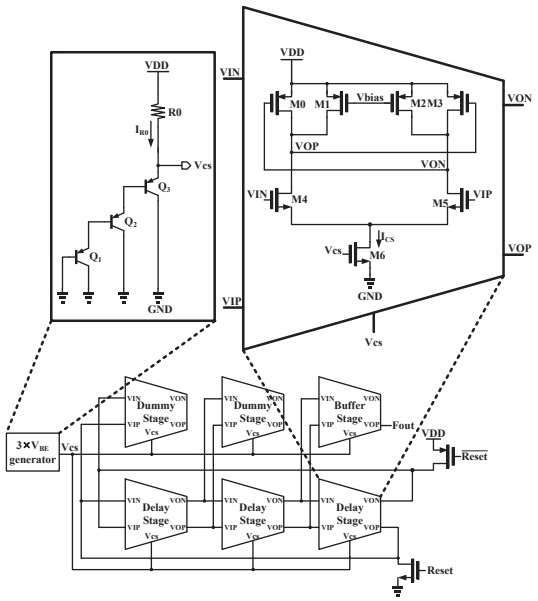

Fig. 2. The schematic of TS

B. Frequency to digital converter (FDC)

The function of FDC is dedicated to derive a linear equation between frequency and temperature. The FDC is composed of a Counter_1, a Counter_2, and a Temperature Decision (TD), as shown in Fig. 3. C1_C and C2_C control the

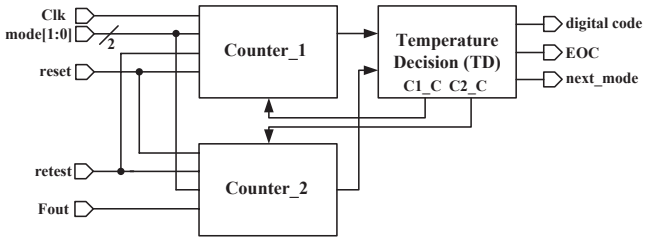

Fig. 3. Block diagram of FDC

Counter_1 and Counter_2 separately. If C1_C (or C2_C) is pulled high, Counter_1 (or Counter_2) counts up. By contrast, if C1_C (or C2_C) is pulled low, Counter_1 (or Counter_2) stays still. After counting up the Clk pulses, Counter_1 sends final count to TD in Fig. 3. By contrast, Counter_2 counts up the Fout pulses, and send the final count as well. Finally, TD receives the two final counts from Counter_1 and Counter_2, respectively, to generate a frequency basing upon the algorithm described in the following section.

C. Temperature Decision (TD)

To derive the linear equation between frequency and temperature, TD firstly checks two reference frequencies at 20°C and 60°C, respectively. There are two ways to acquire the two reference frequencies either by simulation results or

measurement results. The simulation results are derived using HSPICE, which will be stored in the registers. The other relies on the measurement results. As soon as the silicon prototype is ready, the over-temperature protector is measured given $20°C$ and $60°C$ environmental temperatures, and then TD stores the measured frequencies of TS in the registers. By either way, the TD calculates a linear equation by the two reference frequencies, as shown in Eqn. (2), where y means the temperature, x is the frequency, $(x1, y1)$ is the sample of TS in $20°C$, and $(x2, y2)$ is the sample in $60°C$.

$$(y - y1) = \frac{y2 - y1}{x2 - x1} \times (x - x1) \tag{2}$$

Based on the above method, there are four operation modes in TD, which is driven by mode[1:0] as follows.

- mode[1:0]='00': TD calculates the linear equation by simulation results only.
- mode[1:0]='01': The over-temperature protector is selected and measured given a $20°C$ environmental temperature. TD stores the measured frequency of TS.
- mode[1:0]='10': The over-temperature protector is measured given $60°C$ environmental temperature. TD stores the measured frequency of TS.
- mode[1:0]='11': TD senses the current temperature. If retest is asserted, it re-senses the temperature.

Fig. 4 shows the data flow of TD.

1) In the beginning, if the reset is activated, all registers reset.
2) When mode[1:0]='00', TD stores the simulation results in CounterA and CounterB.
3) When mode[1:0]='01', TD counts up Counter_2 until Counter_1 counts up to 100. Then, copy Counter_2 to CounterA.
4) When mode[1:0]='10', TD counts up Counter_2 until Counter_1 counts up to 100. Then, copy Counter_2 to CounterB.
5) When mode[1:0]='11', TD counts up Counter_2 until Counter_1 counts up to 100. Then, copy Counter_2 to CounterC.
6) To calculate the slope, Count_quo, TD uses the Eqn. (3), where 60000 demotes $60.000°C$, 20000 denotes $20.000°C$.

$$\begin{aligned} \text{Count\_quo} &= \frac{y2 - y1}{x2 - x1} = \frac{\text{Delta\_Y}}{\text{Delta\_X}} \\ &= \frac{60000 - 20000}{\text{CounterA} - \text{CounterB}} \end{aligned} \tag{3}$$

7) To increase the resolution, TD is required to distinguish the Count_quo if the LSB of the converted code is higher than 0.5. In such a case, Count_quo pluses 1.
8) Finally, the linear equation is generated. CounterA, CounterB, and CounterC are plugged into Eqn. (2) to derive the y (temperature), as shown in Eqn. (4).

$$\begin{aligned} y = &\frac{(40000 - 20000) \times (\text{CounterC} - \text{CounterA})}{\text{CounterA} - \text{CounterB}} \\ &+ 20000 \end{aligned} \tag{4}$$

III. Implementation and Simulation Results

The proposed design is implemented using a typical 0.35 μm CMOS process to justify the performance. Fig. 5 shows the layout of the proposed design. The proposed design includes four temperature sensors, which are operated in different frequency ranges and one frequency to digital converter (FDC). The chip area is 1.8×1.6 mm^2, where the core area is 1.0×1.2 mm^2. Notably, all of the process corners: $[-40°C, +125°C]$ and [SS, SF, TT, FS, FF] models are simulated. Fig. 6 shows the linearity of TS, where the x-axis is CounterC. Apparently, the slope between the frequency of TS (CounterC) and temperature is linear at all different corners.

FDC is carried out by Verilog HDL code and verified by ALTERA DE2 Development and Education Board (EP2C35F672C6). Fig. 7 shows error distribution of the proposed over-temperature protector at all corners, where the worst error is $6°C$ at FS, $-40°C$. Notably, the worst error is less $\pm 1.8°C$ between $0°C$ and $100°C$ at all corners. Table I shows the comparison of the proposed design with several

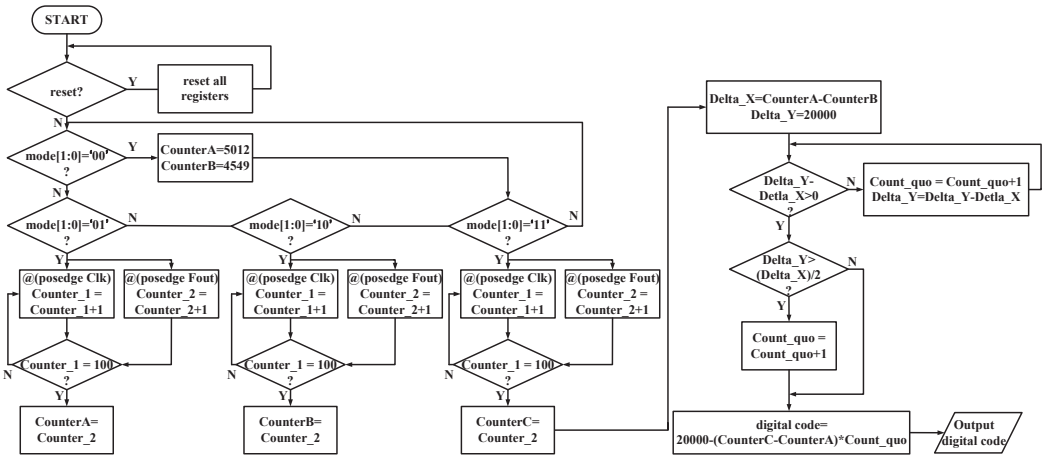

Fig. 4. Data flow of FDC

TABLE I
COMPARISON BETWEEN THE PROPOSED DESIGN AND PRIOR WORKS

	This work	[6]	[7]	[8]
Year	2011	2007	2009	2009
Process (μm)	0.35	0.18	0.35	0.13
Architecture type	Oscillator	Oscillator	Oscillator	Oscillator
Sampling rate	7.875 KHz	N/A	N/A	10 Hz
Resolution	0.001°C/LSB	N/A	N/A	0.4°C/LSB
Temp. range	$-40°C \sim 125°C$	$27°C \sim 47°C$	$10°C \sim 80°C$	$-20°C \sim 96°C$
Worst error @$0°C \sim 100°C$	$< \pm 1.8°C$	$\pm 1°C$	$\pm 1.8°C$	N/A

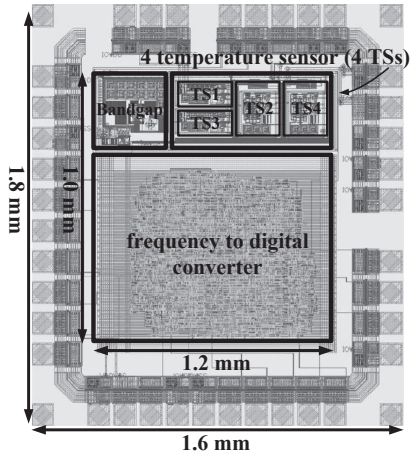

Fig. 5. The layout of the proposed design

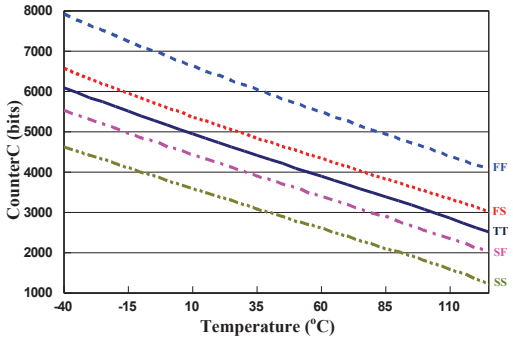

Fig. 6. Linearity of TS

latest works. Our design attains the fastest sampling rate, the lower worst error, and the widest sensing temperature range.

IV. CONCLUSION

In this paper, we propose a digital over-temperature protector for FlexRay systems. The proposed design is implemented using a typical 0.35 μm mixed-signal CMOS process such that it can easily be integrated in a possible SOC solution. The simulation results justify our design is totally compliant with the FlexRay standards, where the temperature range covers from $-40°C$ to $+125°C$. Notably, a digital over-temperature protector is good enough to detect temperature variation on chip.

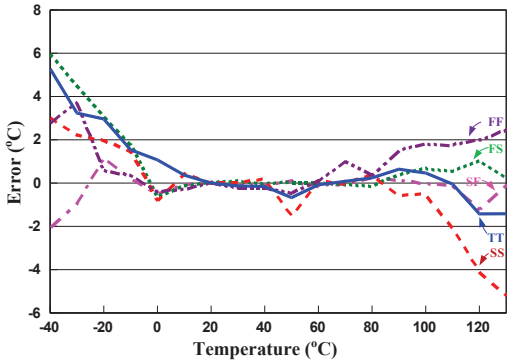

Fig. 7. Error distribution of the proposed over-temperature protector at all corners

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