2.45 GHz ZigBee Receiver Frontend for HAN With Smart Meter

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***Abstract*—This paper proposes a 2.45 GHz ZigBee receiver frontend for the communication in a HAN (Home Area Network) with the smart meter. By employing a cascode LNA, the gain is simulated to be 17.376 dB at 2.45 GHz. Besides, by using the double-balanced Gilbert mixer with a current bleeding MOS transistor, the NF and the IIP3 of the mixer are only 5.074 dB and -7.234 dB, respectively. In order to reduce the phase noise of the receiver, a fractional-N frequency synthesizer with a complementary cross-coupled VCO and a multi-modulus divider are utilized. Moreover, a delta-sigma modulator is included for the noise shaping. The phase noise of the fractional-N frequency synthesizer is 137.7 dBc/Hz. The proposed circuit is carried out using the standard 0.18 μm CMOS process. The core area is 3.57 mm^2.**

Keywords— ZigBee, HAN, smart meter, frontend

I. Introduction

In order to reduce the carbon footprint, an organic building becomes a popular research field recently. The smart meter is one of the important device in the organic building. The smart meter can monitor the power consumption of each electrical device and collect the information of the consuming electricity to the remote database. With a proper management methodology, the smart meter can even shut down the unnecessary electrical device to avoid the waste of energy. For the purpose of the communication in a organic building, the smart meter must operate in a home area network (HAN). With the features of low-cost and low-power, the ZigBee transceiver is suitable for the wireless communication in the HAN, as shown in Fig. 1 [1].

Besides, 2.45 GHz ZigBee possesses the high transmission bit rate of 250 Kbps owing to the O-QPSK (offset-quadrature phase shift keying) modulation [1]. It is sufficient for conveying the security information and is suitable for the HAN. In order to maintain the transmission quality in the RF band, the paper proposes a 2.45 GHz ZigBee receiver frontend which employs a double-balanced Gilbert mixer and a fractional-N frequency synthesizer (FNFS). Based on the worst-case simulation results, the phase noise is -137.7 dBc/Hz.

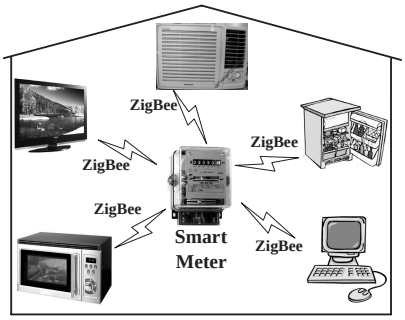

Fig. 1. The applications of ZigBee utilized in the HAN with the smart meter.

II. 2.45 GHz ZigBee Receiver Frontend

The proposed ZigBee receiver frontend is composed of a RF circuit and a baseband circuit, as shown in Fig. 2. The RF circuit receives the differential RF signals from the antenna by the low-noise amplifier (LNA). The amplified differential RF signals are then downconverted to the baseband I/Q signals by the Mixer, which operates with a polyphase filter (PP Filter) and a fractional-N frequency synthesizer (FNFS). The differential baseband I/Q signals are firstly converted to the single-ended I/Q signals by the differential-to-single amplifiers (DtoS AMP). The single-ended signals are then filtered and amplified by the the multiple-feedback filter (MFB Filter) and the programmable gain amplifier (PGA).

A. The Low-Noise Amplifier (LNA)

Fig. 3 (a) shows the schematic of the LNA. The LNA is based on a single-ended common-source amplifier. The MOS transistor M2 serves as a cascode MOS, which can increase the gain of the LNA, avoid the Miller effect, and resist the reflected signal from the output. The input capacitor, C1, is a coupling capacitor to protect the antenna from the DC LNA bias. Besides, the source-inductor, Ls, and the gate-inductor,

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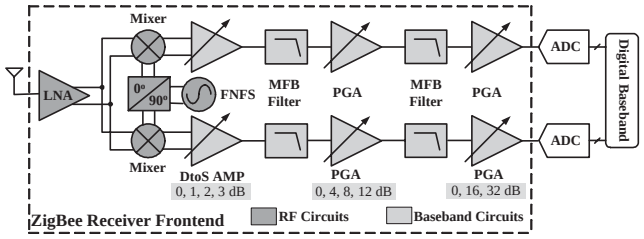

Fig. 2. Block diagram of the proposed ZigBee receiver.

Lg, the drain-inductor, Ld, and the output capacitor C2 are utilized for the impedance matching.

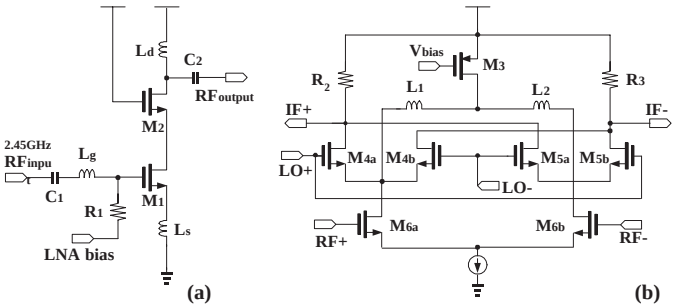

Fig. 3. Schematic of (a) the LNA and (b) the Mixer.

B. The Mixer

The Mixer is in the double-balanced Gilbert configuration, as shown in Fig. 3 (b). M6a and M6b provide the transconductance for the Mixer. By using the current bleeding MOS transistor, M3, and the resonate inductors, L1, and L2, the noise resulted from the bias current can be reduced such that a better noise figure (NF) can be resulted.

C. The Fractional-N Frequency Synthesizer (FNFS)

The LO is based on a fractional-N frequency synthesizer (FNFS). Referring to Fig. 4, the FNFS is composed of a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a fractional-N frequency divider (FNFD). The FNFD performs the integer division for the frequency of Fout. Until the loop is in the lock state, the MASH 1-1 DSM starts the non-integer frequency division for Fout. With the two step fractional-N frequency division, the phase noise and the locking time can be reduced. Besides, the unwanted unlock state is avoided.

1) The VCO: In order to reduce the phase noise, the VCO is in the complementary cross-coupled configuration, as shown in Fig. 5. By using the complementary configuration of M3, M4, M5, and M6, the VCO possesses a higher transconductance than that with only PMOS or NMOS configuration. Besides, the switching speed of the cross-coupled configuration is faster. Moreover, the rise time and the fall time of the VCO are symmetric, such that the phase noise can be reduced. Furthermore, the complementary cross-coupled MOS transistors, M3, M4, M5, and M6, provide the negative resistances, which

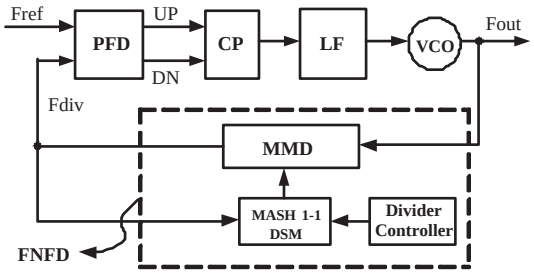

Fig. 4. Block diagram of the fractional-N frequency synthesizer.

compensate the equivalent resistance of the LC tank. Thus, the power consumption can be reduced.

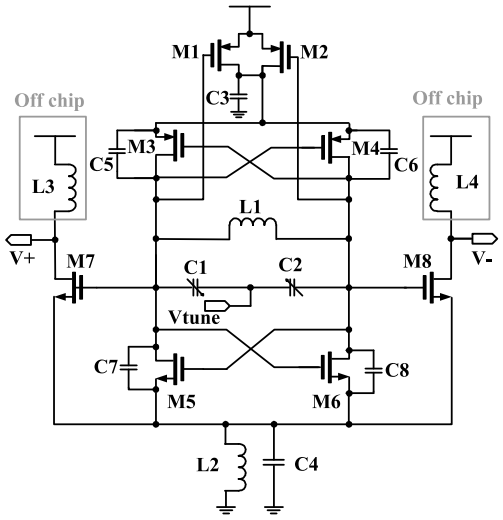

Fig. 5. Schematic of the VCO.

2) The Multi-Modulus Divider (MMD): Fig. 6 (a) shows the schematic of the multi-modulus divider (MMD), which is composed by foure NOR gates, five NAND gates and five 2/3 Dividers. The MMD provides a division ratio from 32 to 63. The division ratio is controlled by the control signals, B0 $\sim$ B4, which are generated by the MASH 1-1 delta-sigma modulator (DSM). Referring to Fig. 6 (b), the MASH 1-1 DSM is composed of five registers (REG), two 8bits CLA adders, and one Noise Cancellator. The MASH 1-1 DSM receives a control signal from the Divider Controller, and a reference clock signal, CK. The MASH 1-1 DSM provides the noise shaping for the MMD, thus, the phase noise can be reduced.

D. The Differential-to-Single-Ended Amplifier (DtoS AMP)

In order to reduce the physical cost, the baseband signal is converted to be single-ended by the differential-to-single-ended amplifier (DtoS AMP). Referring to Fig. 7, the DtoS AMP is composed of three operation amplifiers (OPA), 12 resistors, and 8 switches. Notably, because OP_{pos} and OP_{neg} are in the instrumentation amplifier configuration, the DtoS

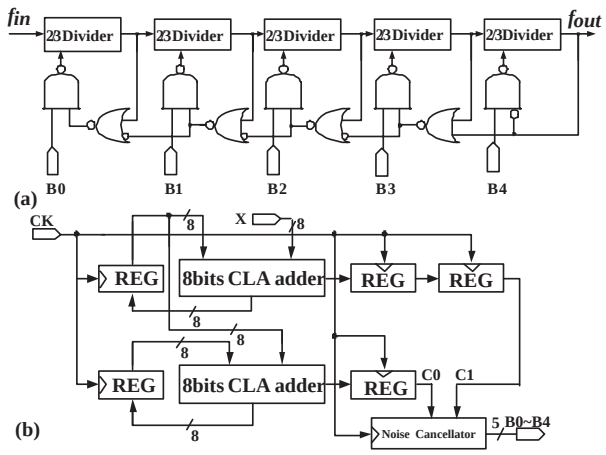

Fig. 6. Block diagram of (a) the multi-modulus divider (MMD) and (b) the MASH 1-1 DSM.

AMP possesses high CMRR. Thus, the DC offset resulted from the Mixer can be canceled. Besides, the DtoS AMP provides four selection for the gain of 0 dB, 1 dB, 2 dB, and 3 dB, by the 8 switches and the resistor array. Furthermore, the equivalent resistors of the turned-on switches can be ignored by connecting the switches to the negative input nodes of the OP_{pos} and OP_{neg} , which possess the infinite input resistance.

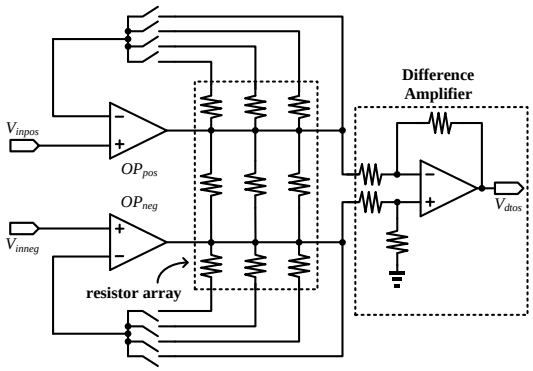

Fig. 7. Schematic of the differential-to-single-ended amplifier (DtoS AMP).

E. The Multiple Feedback (MFB) Filter

Fig. 8 (a) shows the schematic of the Multiple Feedback (MFB) Filter. Notably, the resistances should be determined by considering the loading effect. Besides, the ground symbol in Fig. 8 (a) refers to the AC ground, which are biased at the DC voltage of 1/2 $\times$ VDD.

F. The Programmable-Gain Amplifier (PGA)

The programmable-gain amplifier is composed of an operational amplifier and the feedback resistor array, as shown in Fig. 8 (b). The feedback resistor array is composed of 6 resistors and four switches, which can provide 4 selection for the voltage gain. Referring to Fig. 2, the first PGA provide 4 selection for the gain of 0 dB, 4 dB, 8 dB, and 12 dB. The

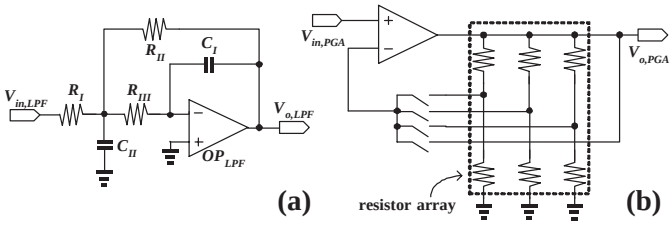

Fig. 8. Schematic of (a) the MFB filter and (b) the PGA.

second PGA provides the selectable gain of 0 dB, 16 dB, 32 dB. Thus, the gain of the baseband circuit is selectable from 0 dB to 47 dB with the gain step of 1 dB.

G. The Rail-to-Rail Operation Amplifier (OPA)

Fig. 9 show the schematic of the rail-to-rail operational amplifier, which is employed in the DtoS AMP, the MFB Filter, and the PGA. The rail-to-rail OPA is composed of the N-type and P-type input stages, the gain stage, and the output stage. By using the N-type and P-type input and the output stage, the rail-to-rail OPA can provide a full swing for the input and output signals. Besides, the cascode structure in the gain stage provides a large resistance at the output nodes of the gain stage. Thus, two MOS transistors, M_{M1} and M_{M2}, and 2 Miller capacitors C_{M1} and C_{M2} are employed for canceling the RHP zero. Therefore, the rail-to-rail OPA possesses the phase margin of 60^o, the open loop gain of 100 dB, and the unity gain frequency of 30 MHz.

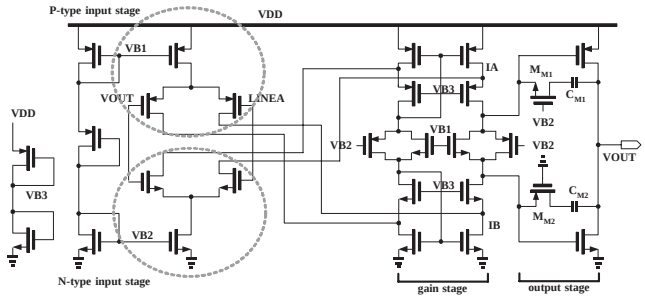

Fig. 9. Schematic of the rail-to-rail OTA.

III. Implementation and Simulation

The proposed 2.45 GHz ZigBee receiver is carried out using TSMC 0.18 μm CMOS process. Fig. 10 shows the layout of the proposed design. The core area is 1.325 $\times$ 2.697 mm^2. Fig. 11 shows the gain of the LNA to be 17.376 dB with the worst-case of SS, 70^oC. Fig. 12 shows that the gain of the baseband circuit is programmable from 0 dB to 47 dB with the gain step of 1 dB. Besides, the cutoff frequency is at 2 MHz determined by the MFB filter. Moreover, phase noise of the fractional-N frequency synthesizer is simulated to be -137.7 dBc/Hz. The specifications of the proposed design are shown in Table I. Moreover, the performances compared to the prior works are shown in Table II. A FOM (figure of merit) is given by considering the gain, IIP3, power consumption,

core area, and the phase noise. According to the FOM, the proposed design possesses the best performance.

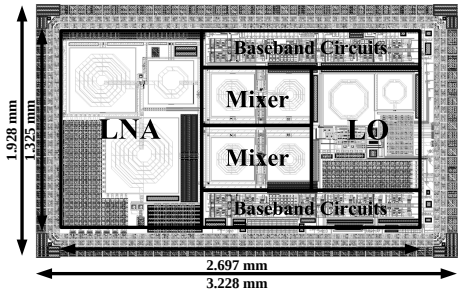

Fig. 10. Layout of the proposed ZigBee receiver.

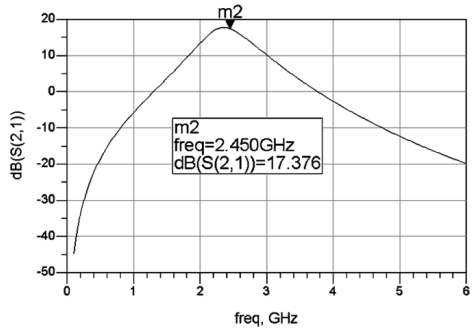

Fig. 11. Simulated waveform of the gain of the LNA at 2.45 GHz for the worst-case of SS, 70^{o}C.

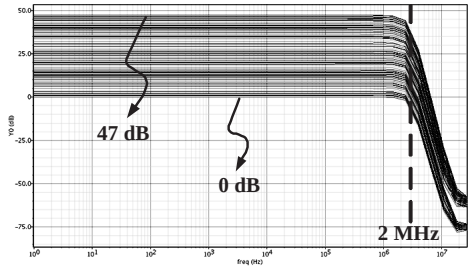

Fig. 12. Simulated waveform of the gain of the baseband circuit from 0 dB to 47 dB.

IV. Conclusion

A 2.45 GHz ZigBee receiver frontend is proposed for the HAN in this paper. The proposed ZigBee receiver employs the cascode LNA, the double-balanced Gilbert mixer, and the fractional-N frequency synthesizer to reduce the phase noise. The phase noise is -137.7 dBc/Hz at the frequency of 3 MHz.

Acknowledgment

This research was partially supported National Science Council under grant NSC99-2220-E-110-001 and NSC 100-2218-E-230-001. Besides, the authors would like to express their deepest gratefulness to CIC (Chip Implementation Center) of NARL (National Applied Research Laboratories), Taiwan, for their thoughtful chip fabrication service.

LNA	S_{11} @2.45 GHz	-43.688 dB
	S_{22} @2.45 GHz	-11.967 dB
	Gain @2.45 GHz	17.376 dB
	Noise Figure	2.712 dB
Mixer	Noise Figure	5.074 dB
	Gain	7.876 dB
	Out-of-channel IIP3	-7.234 dB
FNFS	Phase Noise @1 MHz	-127 dBc/Hz
	Phase Noise @3 MHz	-137.7 dBc/Hz
	Phase Noise @10 MHz	-148.2 dBc/Hz
	Lock time @ 2.45 GHz	$< 20\ \mu$s
	VCO Gain	130 MHz/V
	Bandwidth	200 KHz
Baseband Circuits	Max. Gain	47 dB
	Min. Gain	0 dB
	Filter Bandwidth	2 MHz
Power	Whole chip	88 mW
	LNA	53 mW
	Mixer	5 mW
	FNFS	21 mW
	Baseband circuits	9 mW
Core area		3.57 mm^2

TABLE I
Specifications of the proposed ZigBee receiver.

	This work	[2]	[3]	[4]
Gain	$>$ 73 dB	N/A	$>$ 75 dB	$>$ 67 dB
IF Bandwidth	2 MHz	2 MHz	2 MHz	2 MHz
Phase Noise (dBc/Hz)	-137.7 @3 MHz	N/A	-107.8 @3.5 MHz	-127 @3 MHz
IIP3	-7.234 dBm	-16 dBm	-12.5 dBm	-10.5 dBm
Core Area	3.57 mm^2	1.36 mm^2	0.35 mm^2	1.7 mm^2
VDD (V)	1.8	1.8 / -3.75	1.2	0.6
Power (mW)	88	30.8¶	4.8¶	22¶
Process	0.18μm	0.18μm	90 nm	90 nm
Publication	ISIC	ISSCC	ISSCC	JSSC
Year	2011	2006	2008	2010
FOM†	16.1	N/A	1.13	2.67

Note: ¶ The power includes the power consumption of the receiver and the analog circuits.

† $\text{FOM} = \frac{\text{Gain(in amplitude ratio)}\times\text{IIP3}}{\text{Power}\times\text{Core Area}\times\text{Phase Noise}\times 10^{13}}$.

TABLE II
Comparison with several prior works

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